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Interfacing SDRAM on High-Performance Microcontrollers Design Guide

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Design Resources

TIDM-TM4C129XSDRAM	Tool Folder Containing Design Files
TIDM-CONNECTED-ETHERNET	Tool Folder
TM4C129XNCZAD	Product Folder
TM4C123GH6PM	Product Folder
TPS2051B	Product Folder
LM4819	Product Folder
TPS62177	Product Folder
REF3230	Product Folder
TMP100	Product Folder

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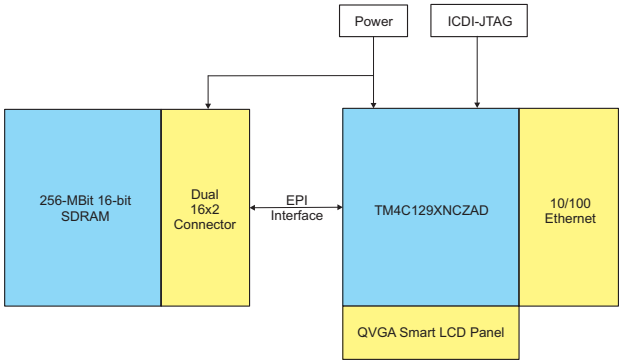
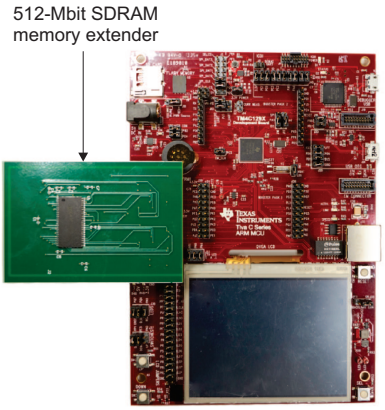
Design Features

- DK-TM4C129X EVM (formerly Tiva™ MCU) With Integrated Smart QVGA LCD Panel For Graphics Rendering
- 512-Mbit 16-bit SDRAM With 60-MHz EPI Interface For High-Memory Throughput And Footprint Applications
- Driver Library Components To Simplify Code Development
- Source Code With Project For Code Composer Studio™

Featured Applications

- Interactive Human Machine Interfaces
- IoT Solutions
- Industrial Automation





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1 System Description

The interfacing of the TM4C129x family of microcontrollers to an external memory can be used to download and execute code and data when the internal memory is not sufficient for a large user application. This application note describes the requirements for hardware interfacing and software example codes for TM4C129x microcontrollers from Texas Instruments for external 512-Mbit 16-bit access SDRAM.

The design files include Schematics, BOM, Layer plots, Altium files, Gerber, and reference example codes for easy-to-use SDRAM with the TM4C129XNCZAD EVM kit.

1.1 TM4C129XNCZAD

TM4C129XNCZAD is 120-MHz high-performance microcontroller with 1-MB on-chip Flash and 256-KB on-chip SRAM. This microcontroller features an integrated Ethernet MAC+PHY for connected applications. The device has high bandwidth interfaces like an LCD controller, memory controller, and a high-speed USB 2.0 digital interface. With integration of a number of low- to mid-speed serials, up to 4-MSPS 12-bit ADC, and motion control peripherals, the device makes for a unique solution for a variety of applications ranging from industrial communication equipments to smart energy and smart grid applications.

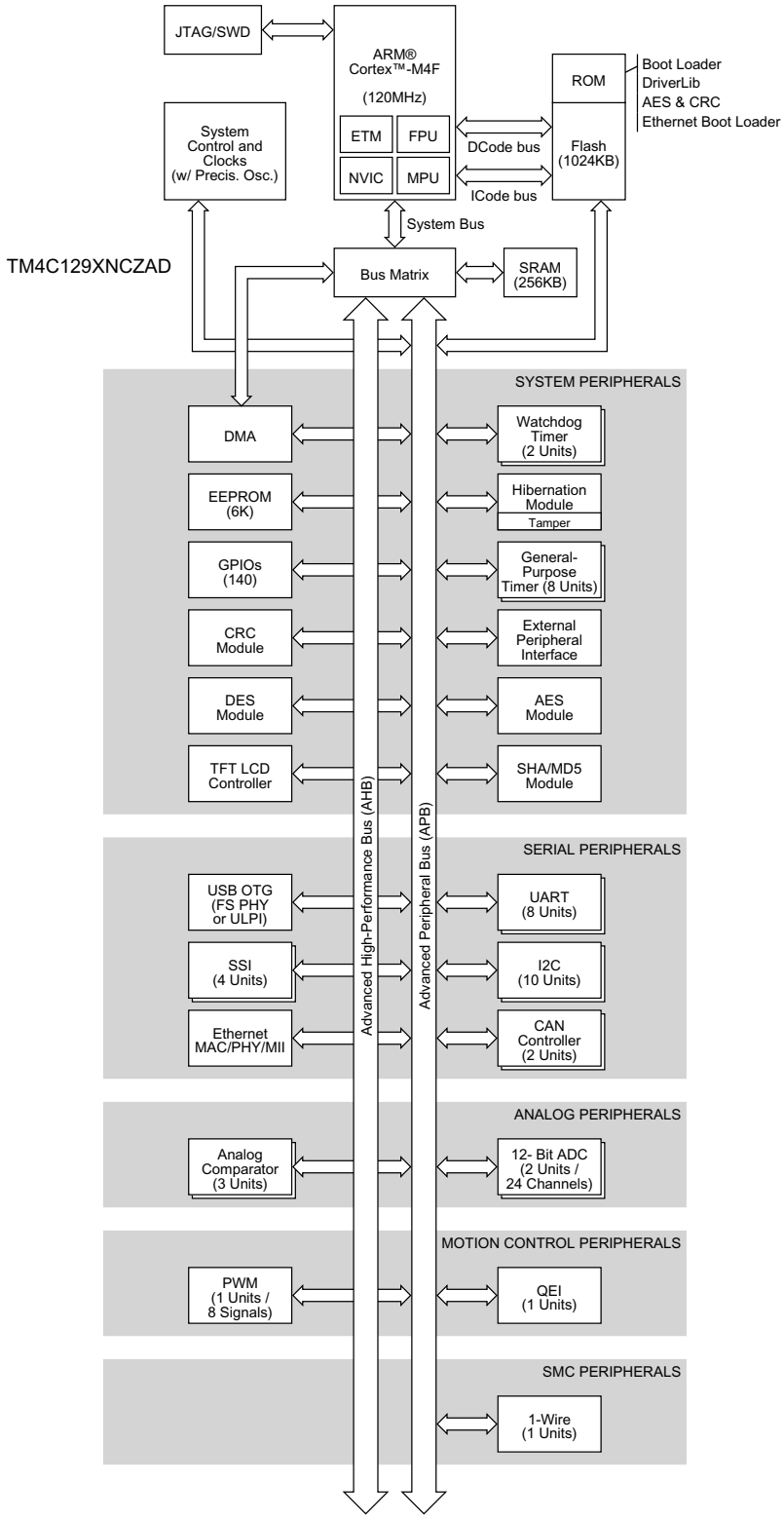

Figure 1. TM4C129XNCZAD Microcontroller High-Level Block Diagram

2 Block Diagram

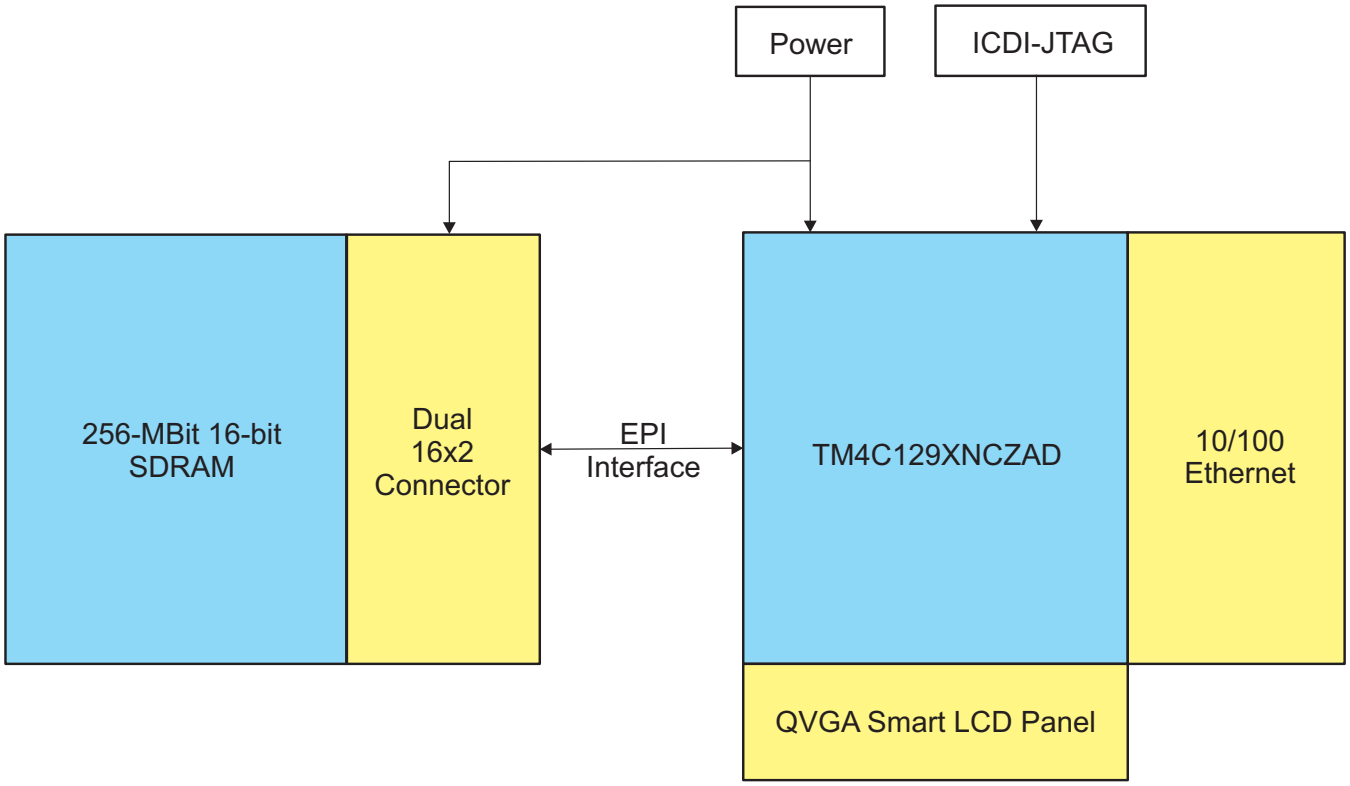

Figure 2. SDRAM Extender Block Diagram

3 Getting Started Hardware

The interfacing of the external SDRAM to the TM4C129XNCZAD device on the DK-TM4C129X requires a daughter board to be designed that can be connected to the evaluation kit on headers J27 and J28.

3.1 SDRAM Daughter Card

The SDRAM daughter card uses easily available dual 15×2 female receptacles that are connected to the dual 16×2 headers on the DK-TM4C129X EVM. To ensure that the receptacles mate correctly, connect pin-1 of the daughter card to pin-3 of the headers. This connection helps avoid the 5-volt J27.1 and J28.1 from connecting to the daughter card and prevents any damage to the SDRAM, while reducing the cost due to a lower-pin-count receptacle. The receptacles mount to the surface to allow for optimal routing and shorter trace lengths. Figure 3 illustrates the final connector mounting:

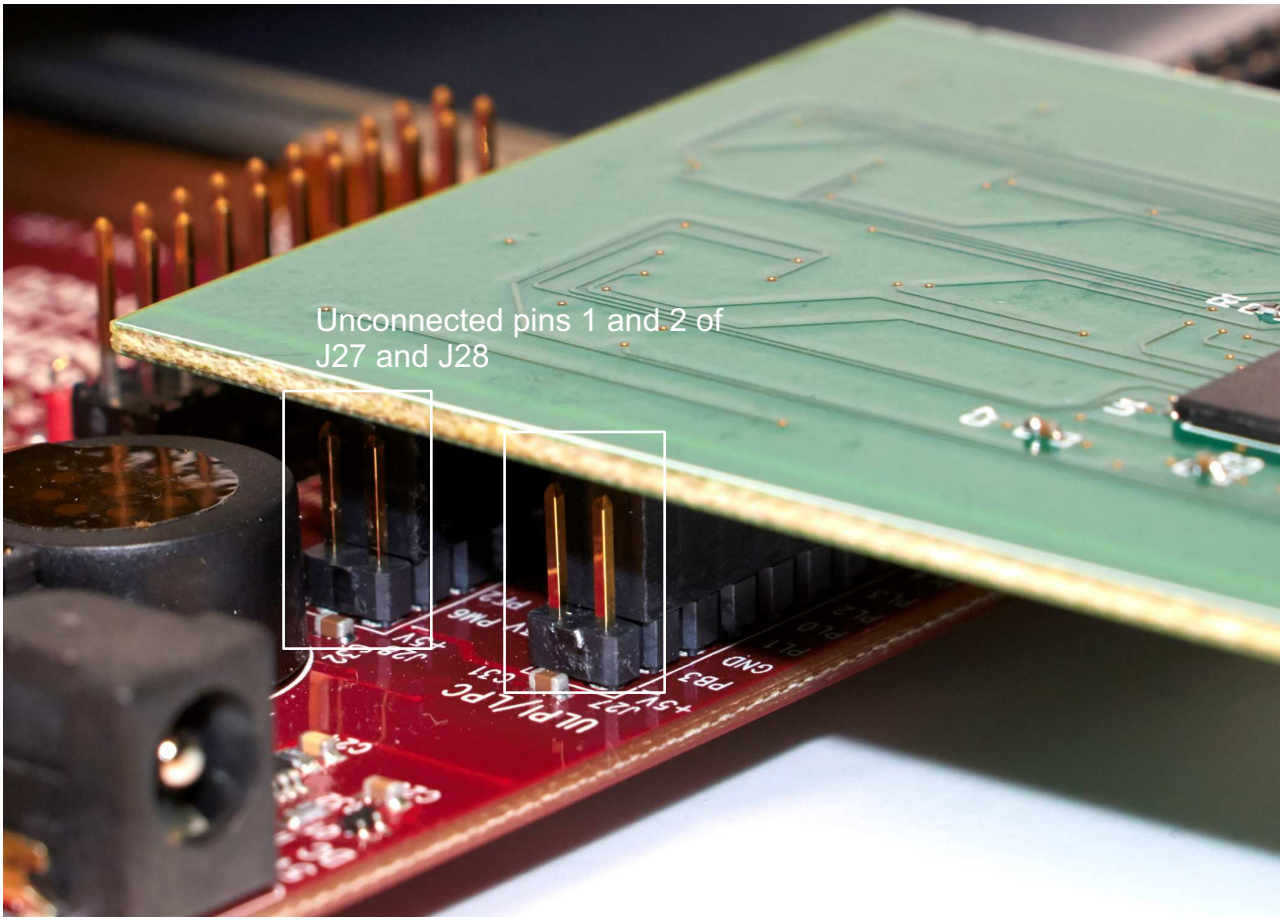

Figure 3. SDRAM Connector Mounting

4 Getting Started Software

The reference design comes with an example code that the user can import in Code Composer Studio™. The following subsections describe the example code that customers may use in their end application.

4.1 SDRAM Throughput Performance-Example Code

The SDRAM throughput performance-example code configures the I/O's of TM4C129XNCZAD to be controlled by the EPI module. This example then configures the EPI module for the 512-Mbit SDRAM with interface frequency of 60 MHz. On successful initialization, the SDRAM performs a write of 4-K bytes and measures the time taken using the SysTick timer to compute the bandwidth. After completing the write, the SDRAM performs a read of the 4-K bytes and measures the time taken using the SysTick timer to compute the bandwidth. The operations performed are with 16-bit, 32-bit, and 64-bit words.

5 Test Setup

The test setup involves importing the example code into Code Composer Studio, building the same, and executing the code on the DK-TM4C129X EVM. Section 6 shows the results of the example that a customer may expect and a scope view of the SDRAM clock.

NOTE: The use of the examples assumes that Serial Console Application (PuTTY, TeraTerm, and others), Code Composer Studio v6.0.1, and TivaWare Full Installation Software release 2.1.0-12573 have already been downloaded and installed on the PC.

5.1 Hardware Setup

Figure 4 shows the full setup. The USB cable that comes as a part of the DK-TM4C129X EVM (shown on the top right) provides power, JTAG for debug, and UART for the serial console to the EVM and the SDRAM memory extender. The SDRAM memory extender is connected on the left side of the image to the headers J27 and J28.

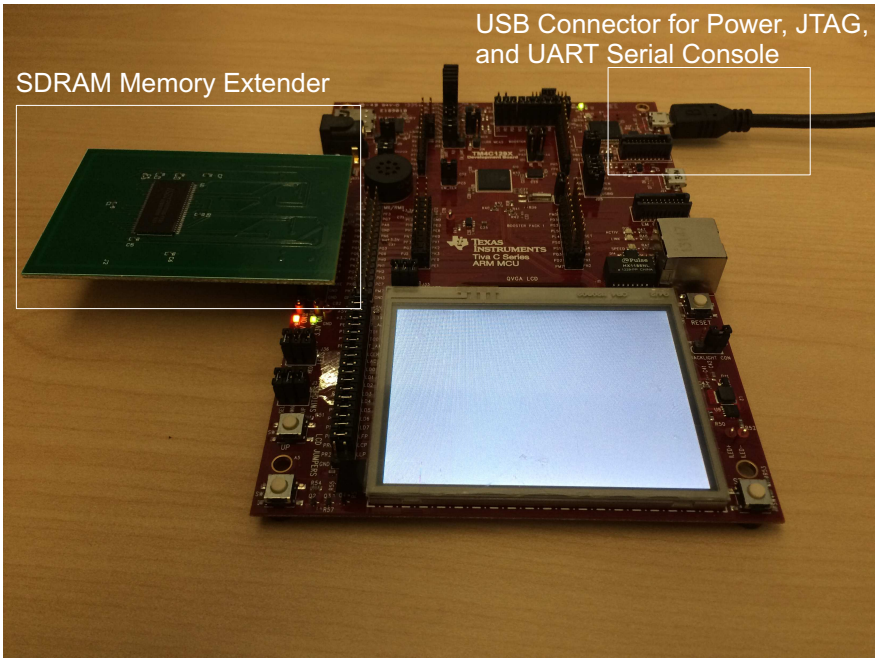

Figure 4. Full Test Assembly

5.2 Software Setup

Follow these steps to set up the software:

1. Download the software examples zip package from the TI Design web page and unzip the file on the local PC.
2. Launch Code Composer Studio v6.0.1 or later. To import the project, click File → Import → CCS Projects, then click “Next”. Browse to the directory where the software examples are kept. Select the project “dktm4c129_sdram_performance_example”, and click “Finish”.

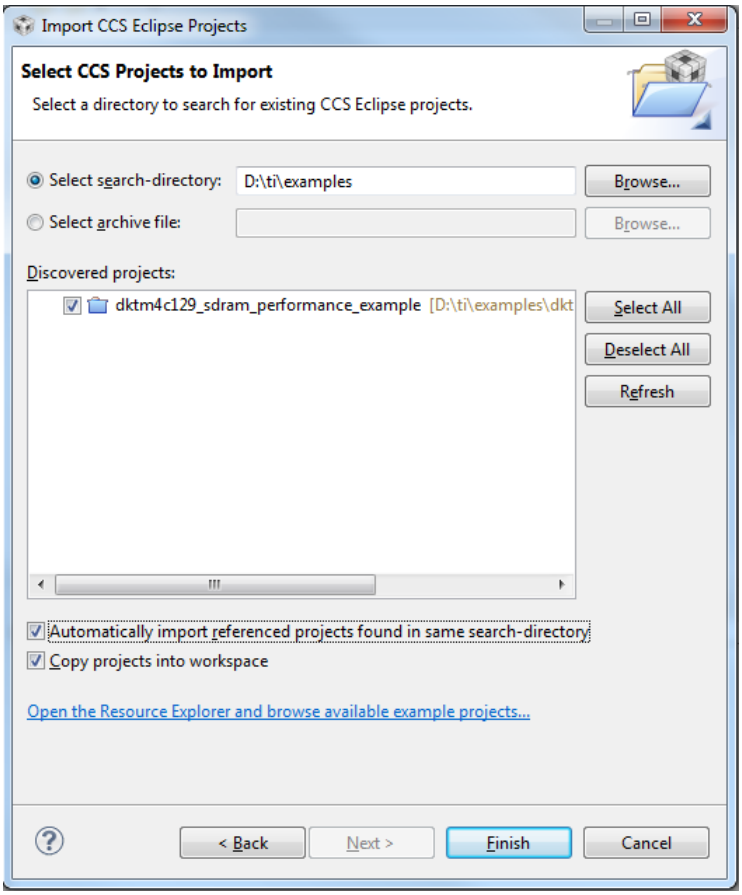

Figure 5. Importing the Software Example

3. Build the project by right clicking the project and then selecting “Rebuild Project”. The project must compile without any errors.

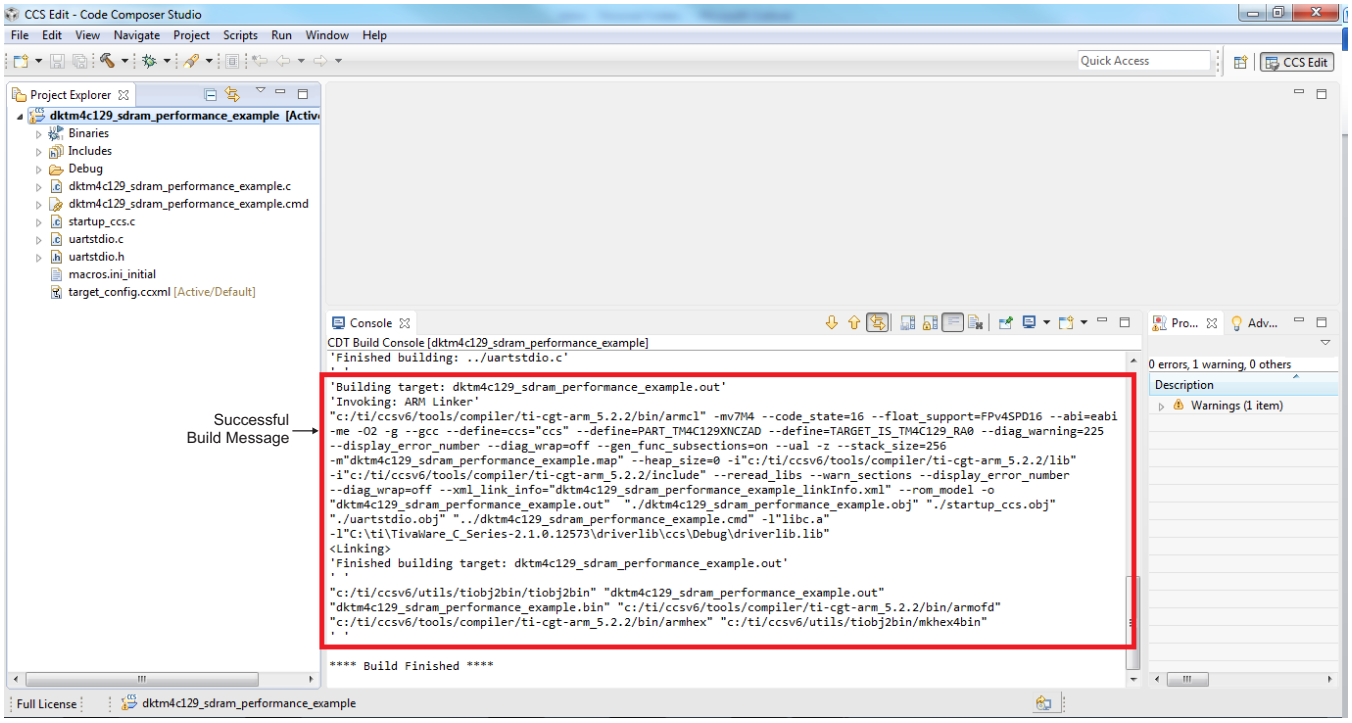

Figure 6. Compiling the Software Example

4. Run the example by pressing the Debug button, which will load the code into the TM4C129XNCZAD Flash. Press the Play button after the code has loaded. On a serial console, users must see the following message including the bandwidth computed for the write and read to the SDRAM.

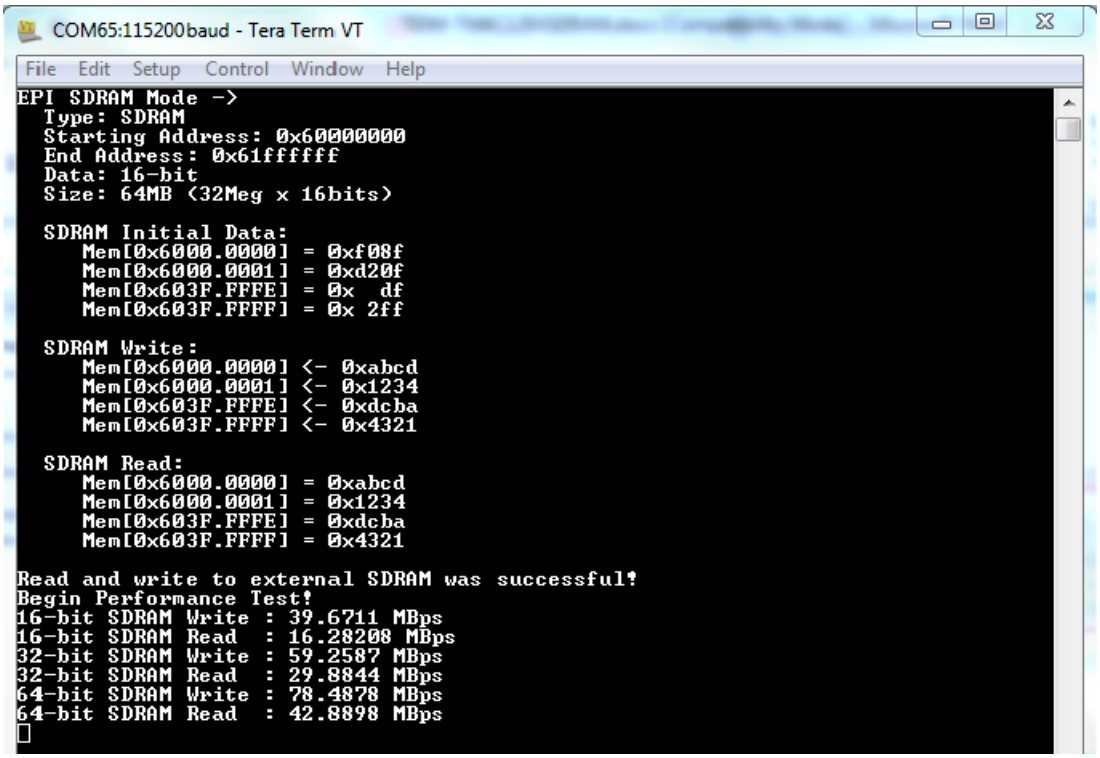

Figure 7. Expected Console Output for the Software Example

6 Test Data

The following section highlights the performance data and electrical signal integrity of the SDRAM clock pin during the transactions.

6.1 SDRAM Performance Data

The example code for the SDRAM performance test is a bare-metal example and may only be used as a reference when ensuring that all hardware connections are correct. Based on the DK-TM4C129X EVM and with a system frequency of 120 MHz, the maximum SDRAM clock achievable is 60 MHz. Table 1 computes the bandwidth for the different Write and Read operations via the Cortex-M4 CPU:

Table 1. Performance of SDRAM with EPI in Different Burst Modes

	SDRAM WRITE THROUGHPUT	SDRAM READ THROUGHPUT
16-BIT WORD	39.6711 MBps	16.282 MBps
32-BIT WORD (BURST SIZE OF 2)	59.2587 MBps	29.884 MBps
64-BIT WORD (BURST SIZE OF 4)	78.4878 MBps	42.889 MBps

6.2 SDRAM Electrical Signal Integrity

The waveform plot in Figure 8 shows the signal behavior of EPI0S31, which is the SDRAM clock from the TM4C129XNCZAD device to the SDRAM during active Write and Read transactions.

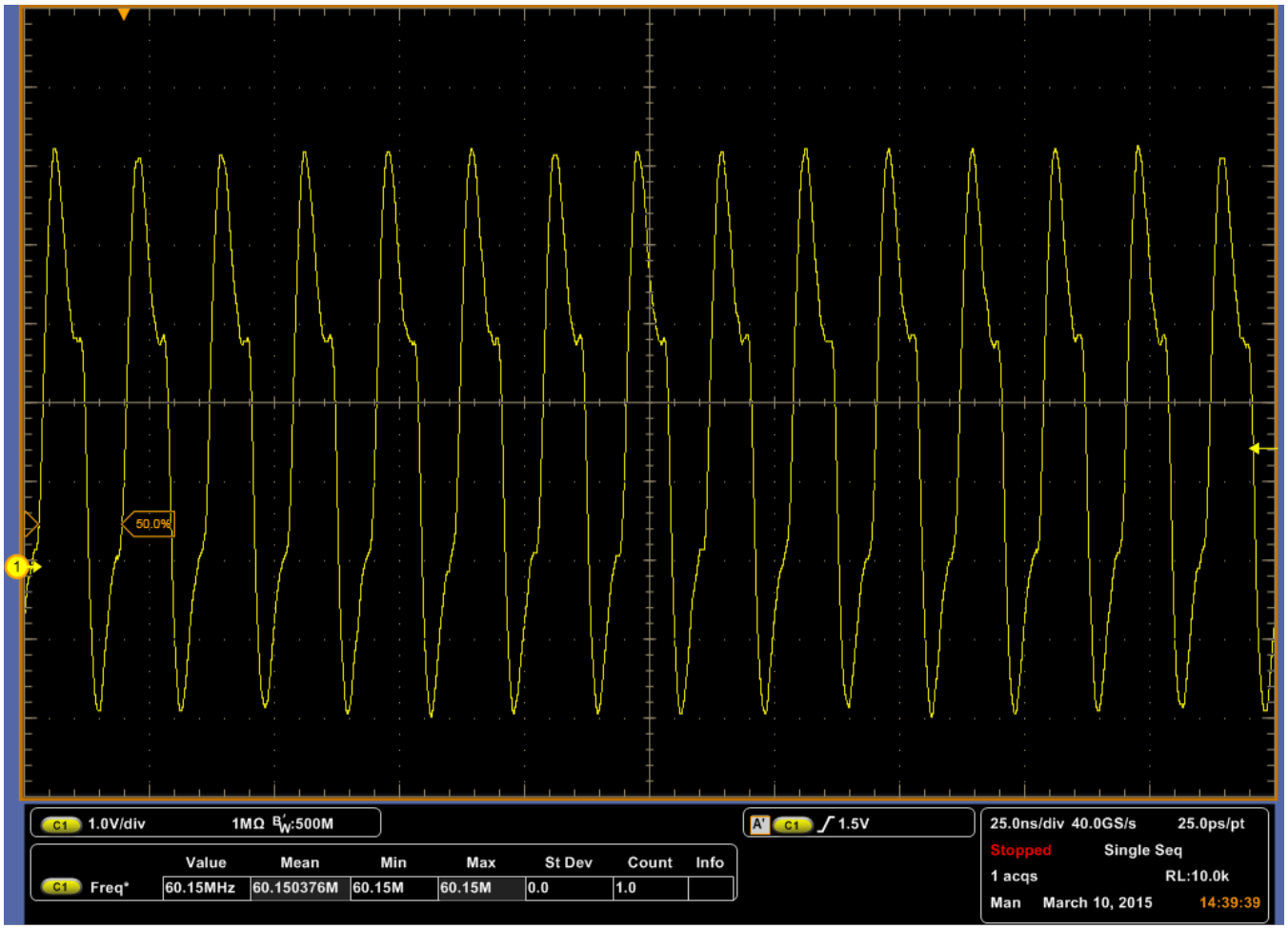

Figure 8. SDRAM Clock Signal Integrity

7 Design Files

7.1 Schematics

To download the Schematics for each board, see the design files at TIDM-TM4C129XSDRAM.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-TM4C129XSDRAM.

7.3 PCB Layout Recommendations

When performing the layout, ensure that the EPI0S31 (the SDRAM clock pin) has the shortest trace. Also, minimize reflections from the shared data and address pins, and use a single route from the connector pin to either the address or data pin without creating a stub. Please see Section 7.6.

7.4 Layer Plots

To download the layer plots, see the design files at TIDM-TM4C129XSDRAM.

7.5 Altium Project

To download the Altium project files, see the design files at TIDM-TM4C129XSDRAM.

7.6 Layout Guidelines

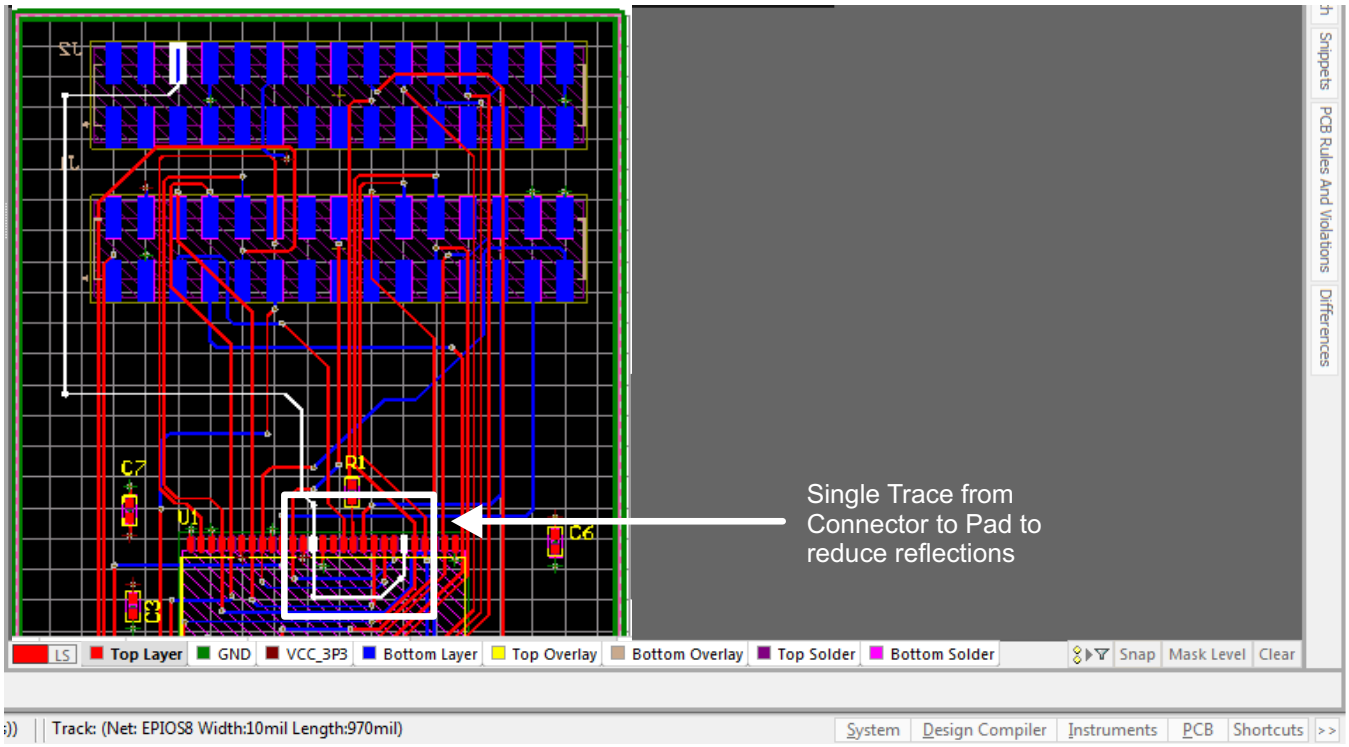

Figure 9. Layout Guidelines for Reducing Reflections

7.7 Gerber Files

To download the Gerber files, see the design files at TIDM-TM4C129XSDRAM.

7.8 Software Files

To download the software files, see the design files at TIDM-TM4C129XSDRAM.

8 References

1. ISSI 512Mbit SDRAM Memory (http://www.issi.com/WW/pdf/42-45R-S_86400D-16320D-32160D.pdf)

9 About the Author

AMIT ASHARA is an Application Engineer at Texas Instruments, where he is responsible for developing applications for the TM4C12x family of high-performance microcontrollers. Amit brings to this role his extensive experience in high-speed digital and microcontroller system-level design expertise. Amit earned his Bachelor of Engineering (BE) from University of Pune, India.

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