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Parallel Load Switches for Higher Output Current & Reduced ON-Resistance Design Guide

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Design Resources

TIDA-00513	Tool Folder Containing Design Files
TIDA-00514	Design Folder
TPS22966	Product Folder
TPS22959	Product Folder
TPS22966EVM-007	Product Folder

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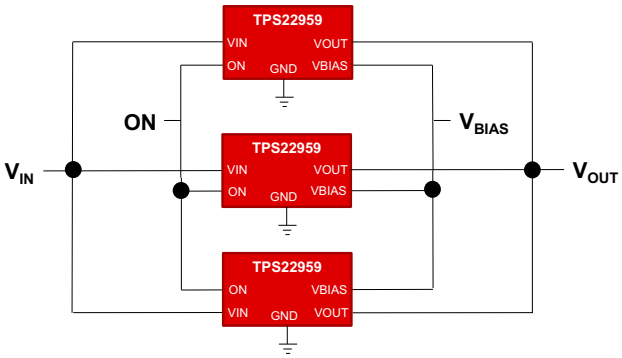
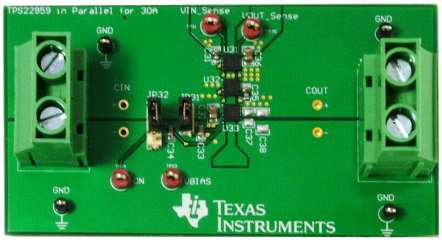
Design Features

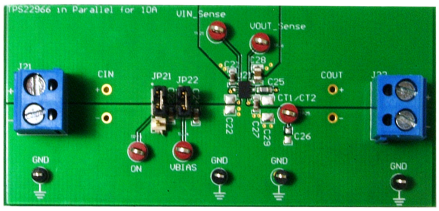
- Increased Maximum Output Current
- Reduced Total ON-Resistance (R_{ON})
- Faster Output Rise Time
- Lower Power Dissipation
- Reduced Quick Output Discharge (QOD) Resistance

Featured Applications

- Servers
- Enterprise Computing
- Industrial Systems
- High Current Voltage Rails







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1 System Description

Users can expand the functionality of existing load switches by placing multiple channels in a parallel configuration. This TI Design demonstrates two examples of paralleling load switches.

1.1 Dual TPS22966

The first example uses both channels of the dual-channel TPS22966 for a total output current of 10 A.

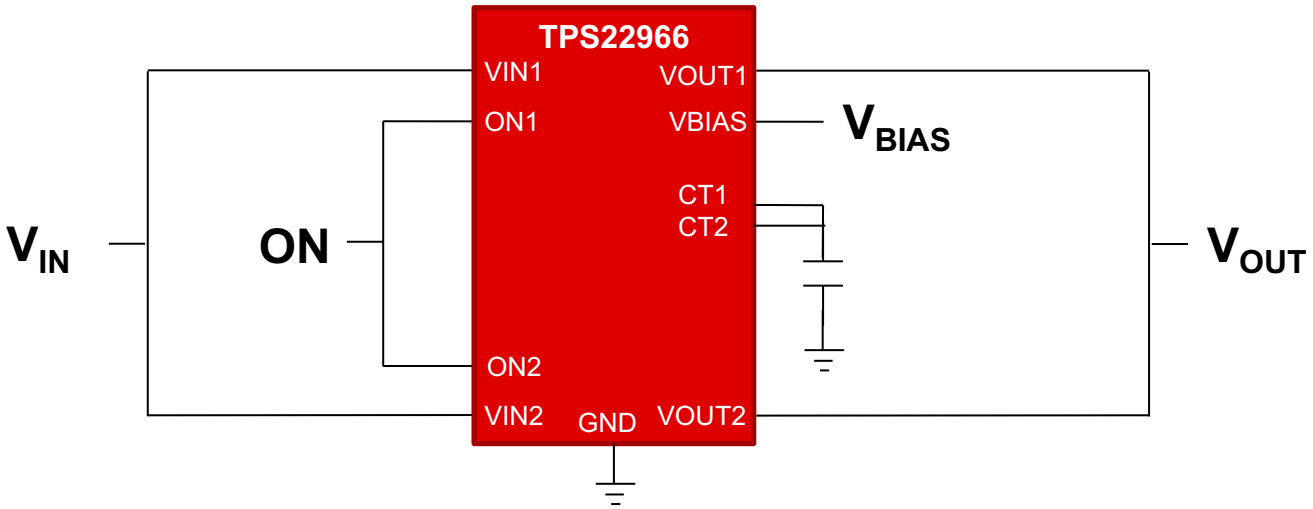

Figure 1. Dual TPS22966 Block Diagram

1.1.1 Key Specifications

Table 1. Key Specifications

PARAMETER	SPECIFICATION	DETAILS
Maximum Continuous Output Current	10 A	See Section 4.1
Typical ON Resistance	8 mΩ	See Section 7.1
Rise Time at 5 V	262 us	See Section 7.2

1.2 Triple TPS22959

The second uses three TPS22959 in parallel for a total output current of 30 A.

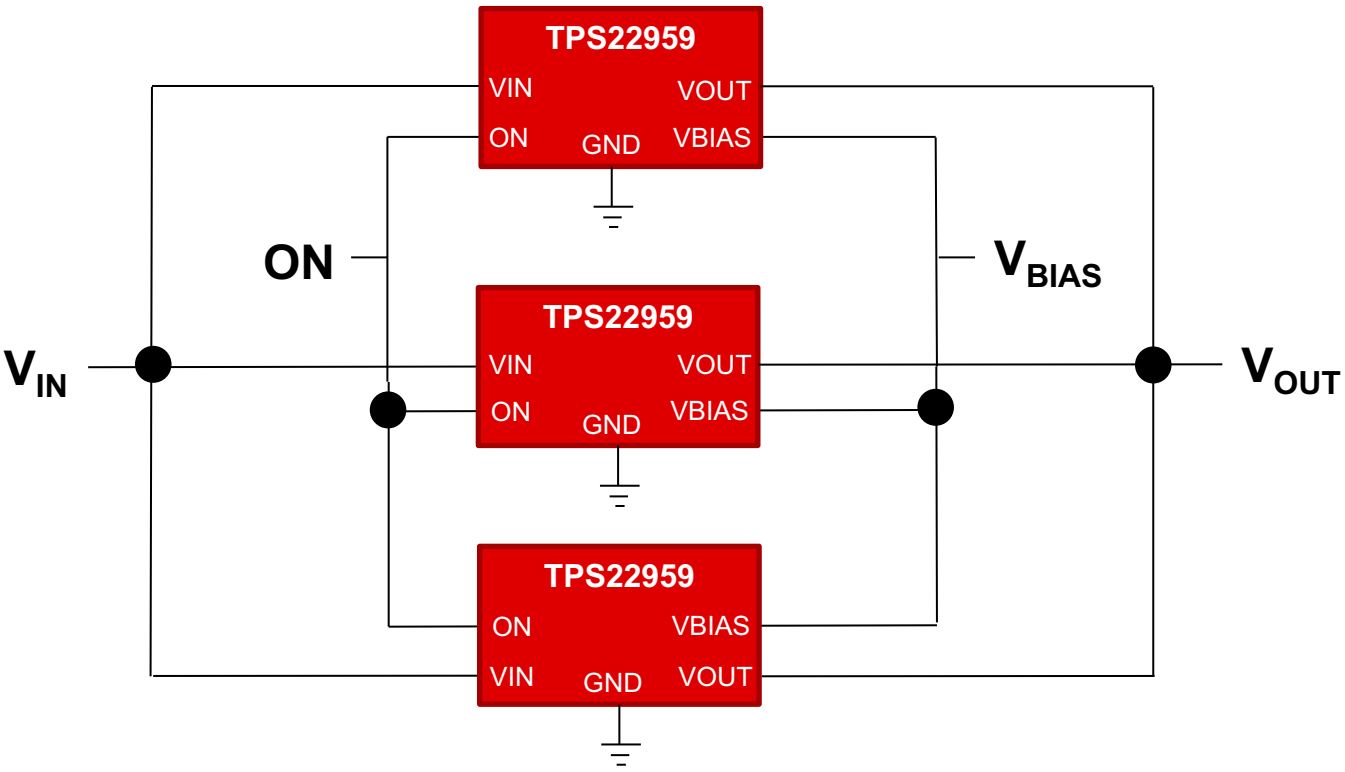

Figure 2. Triple TPS22966 Block Diagram

1.2.1 Key Specifications

Table 2. Key Specifications

PARAMETER	SPECIFICATION	DETAILS
Maximum Continuous Output Current	30 A	See Section 4.1
Typical ON Resistance	1.5 mΩ	See Section 8.1
Rise Time at 5 V	2.4 ms	See Section 8.2

2 Block Diagram

The block diagrams for the two parallel load switch circuits are shown in Figure 3 and Figure 4.

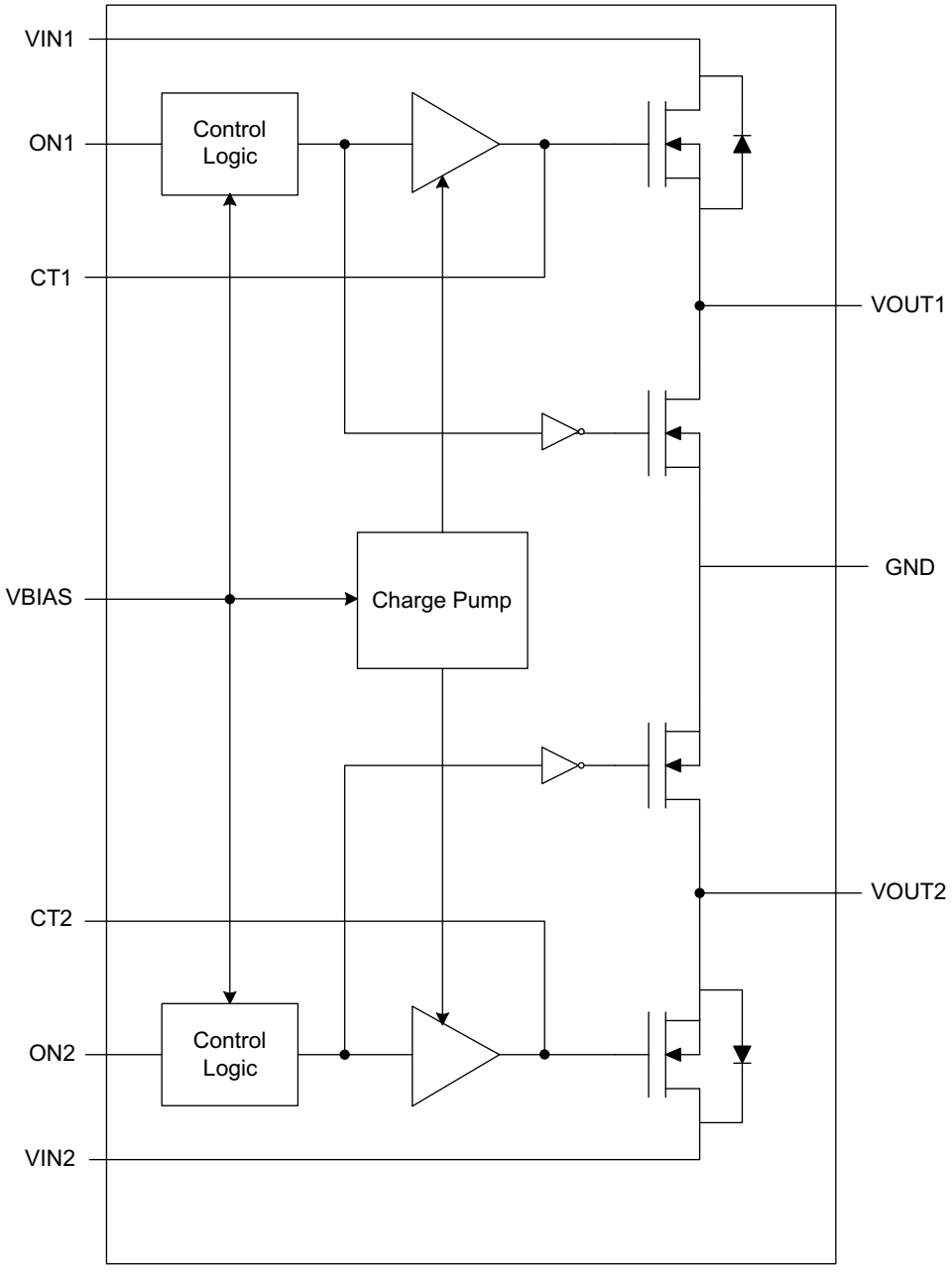

Figure 3. TPS22966 Functional Block Diagram

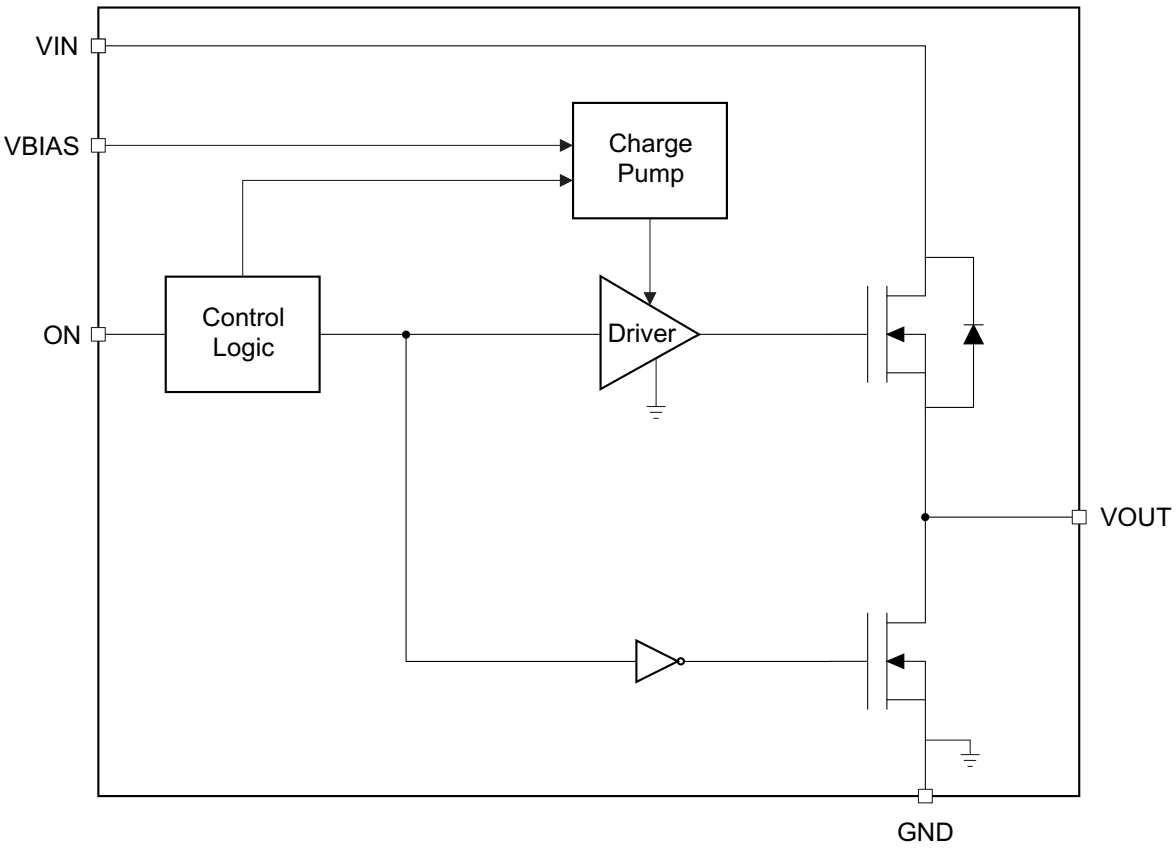

Figure 4. TPS22959 Functional Block Diagram

3 Highlighted Products

3.1 TPS22966

- Integrated Dual-Channel Load Switch
- Input Voltage Range: 0.8 V to 5.5 V
- ON-Resistance
  - R_{ON} = 16 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 16 mΩ at V_{IN} = 3.6 V (V_{BIAS} = 5 V)
  - R_{ON} = 16 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)
- 6-A Maximum Continuous Switch Current per Channel
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Configurable Rise Time
- Quick Output Discharge (QOD)
- SON 14-Pin Package With Thermal Pad

3.2 TPS22959

- Integrated Single Channel Load Switch
- V_{BIAS} Voltage Range: 2.5 V to 5.5 V
- V_{IN} Voltage Range: 0.8 V to 5.5 V
- Ultra Low R_{ON} Resistance
  - R_{ON} = 4.4 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
- 15 A Maximum Continuous Switch Current
- Low Quiescent Current (20 µA for V_{BIAS} = 5 V)
- Low Shutdown Current (1 µA for V_{BIAS} = 5 V)
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Quick Output Discharge (QOD)
- SON 8-Terminal Package with Thermal Pad

4 System Design Theory

This section will discuss how placing multiple load switch channels in parallel will effect functionality.

4.1 Increased Maximum Output Current

When multiple load switch channels are placed in the parallel, the maximum output current increases for two reasons:

1. The total ON Resistance is lower reducing the amount of V = IR voltage drop.
2. The power dissipation will be more distributed leading to better thermal performance.

4.2 Reduced Total ON-Resistance (R_{ON})

Placing multiple load switch channels in parallel will reduce the typical and maximum ON Resistance proportionately to the number of channels in parallel. For example, two channels will half the ON Resistance, and three channels will result in one third. This event is critical in systems with tight tolerances on the voltage rails.

4.3 Faster Output Rise Time

When a single-load switch channel is turned on, the inrush current is limited by a controlled slew rate. When multiple channels are in parallel, the total inrush will increase, allowing for a faster output rise time.

4.4 Reduced Quick Output Discharge (QOD) Resistance

For load switches that connect a quick output discharge resistance to the output when disabled, the total QOD resistance will be reduced because multiple QOD resistors will be in parallel. This lower QOD resistance will reduce the output fall time, leading to a faster system power down sequencing.

5 Getting Started Hardware

This section will provide an overview of PCB hardware.

5.1 Dual TPS22966 Connections and Test Points

Table 3 shows a summary of the connections and test points for the dual TPS22966:

Table 3. Dual TPS22966 Connections and Test Points

CONNECTION	NAME	DESCRIPTION
J21	V_{IN}	DC Input to V_{IN}
J22	V_{OUT}	Load Connection for V_{OUT}
JP22	V_{BIAS} Power	Connects V_{BIAS} to V_{IN}
JP21	ON Control	Connects ON pin to V_{IN} or GND
TP21	V_{IN} Sense	Sense Connection to V_{IN}
TP26	V_{OUT} Sense	Sense Connection to V_{OUT}
TP24	V_{BIAS}	V_{BIAS} Connection
TP23	ON	Enable Connection
TP22, TP27, TP28, TP29	GND	Connection to Board Ground

5.2 Triple TPS22959 Connections and Test Points

Table 4 shows a summary of the connections and test points for the triple TPS22959:

Table 4. Triple TPS22959 Connections and Test Points

CONNECTION	NAME	DESCRIPTION
J31	V_{IN}	DC Input to V_{IN}
J32	V_{OUT}	Load Connection for V_{OUT}
JP31	V_{BIAS} Power	Connects V_{BIAS} to V_{IN}
JP32	ON Control	Connects ON pin to V_{IN} or GND
TP31	V_{IN} Sense	Sense Connection to V_{IN}
TP35	V_{OUT} Sense	Sense Connection to V_{OUT}
TP33	V_{BIAS}	V_{BIAS} Connection
TP34	ON	Enable Connection
TP32, TP36, TP37, TP38	GND	Connection to Board Ground

6 Test Setup

Figure 5 and Figure 6 show how to collect ON Resistance and turn on measurements for the dual TPS22966 circuit. A similar setup can be used for the triple TPS22959 circuit.

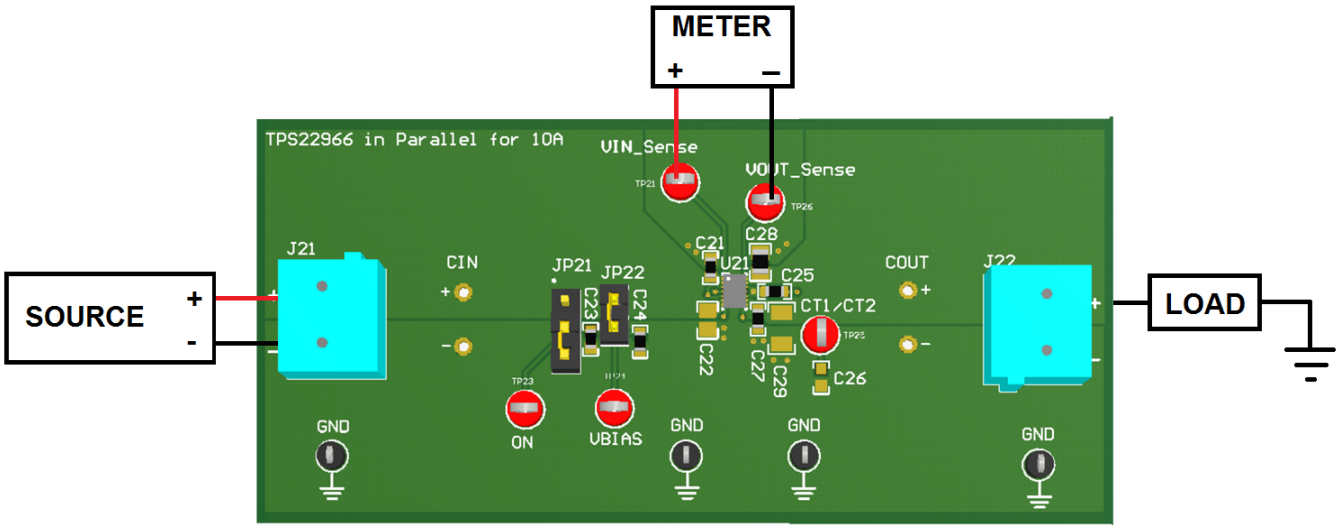

Figure 5. ON Resistance Test Setup

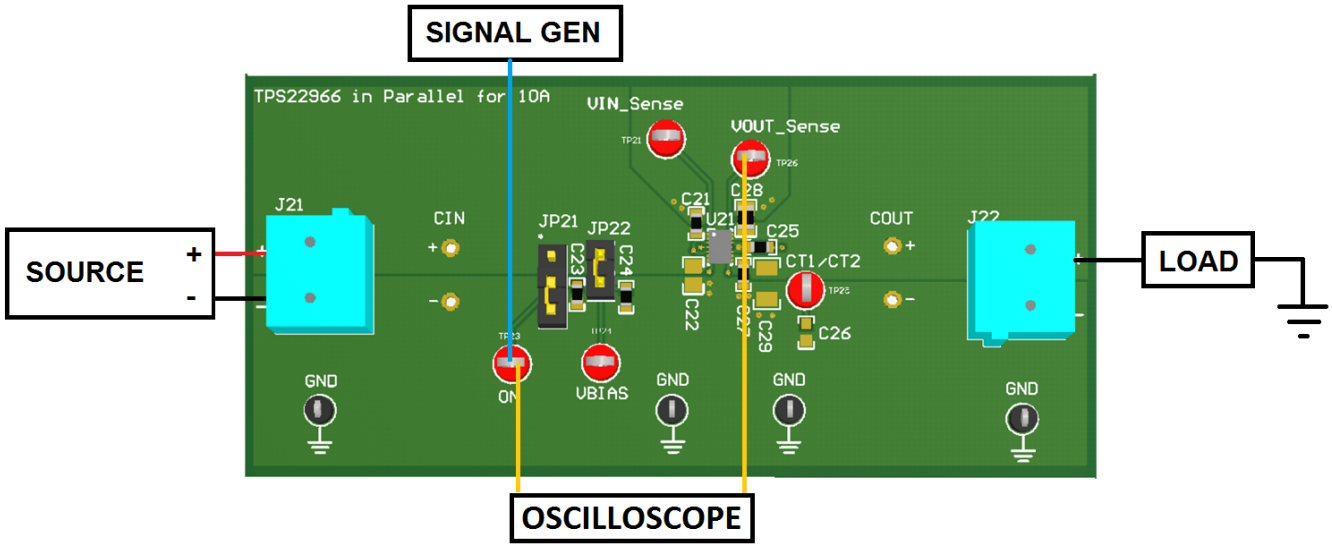

Figure 6. Turn On Test Setup

7 Dual TPS22966 Test Data

This section will cover the test data from the dual TPS22966 circuit.

7.1 ON Resistance vs. Load Current

Table 5 provides a summary of the ON Resistance measured at various loads:

Table 5. ON Resistance vs. Load Current

LOAD CURRENT	$V_{IN} = V_{BIAS} = 5$ V	$V_{IN} = V_{BIAS} = 3.3$ V
200 mA	7.8 mΩ	8.7 mΩ
1 A	7.8 mΩ	8.7 mΩ
5 A	7.9 mΩ	8.8 mΩ
10 A	8.6 mΩ	9.7 mΩ

7.2 Turn On Waveforms

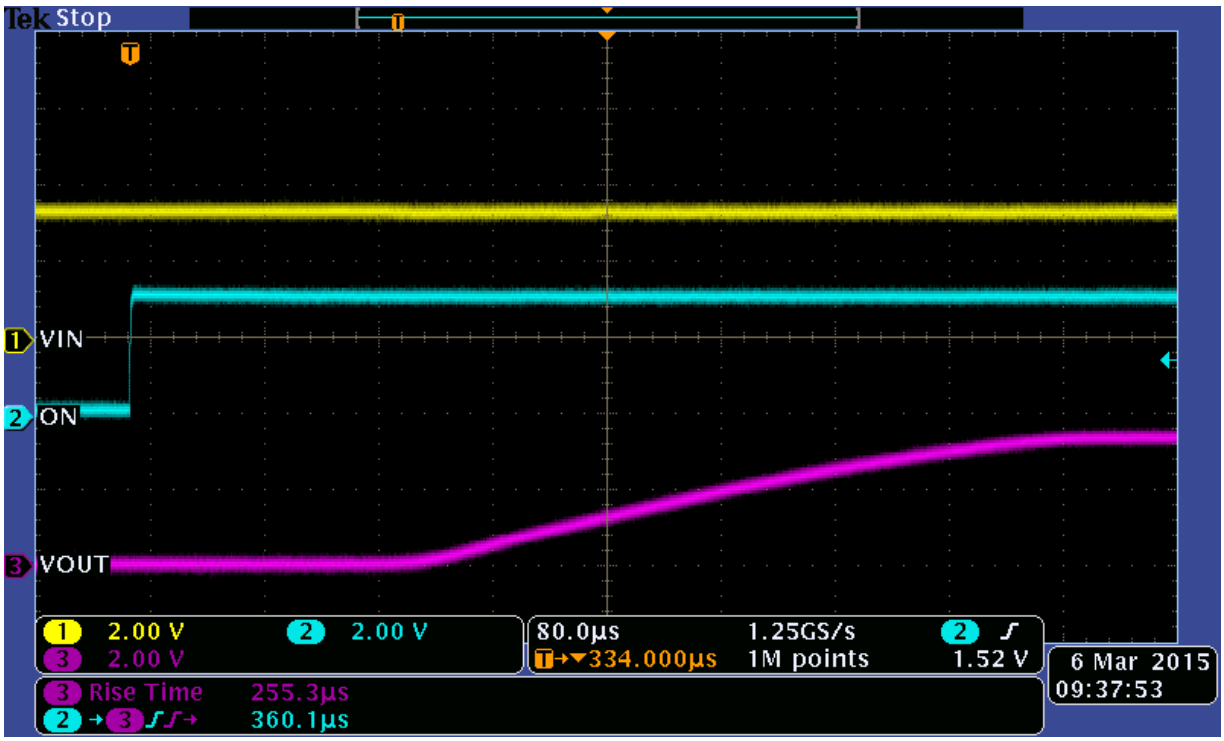

Figure 7. Dual TPS22966 Turn On Waveform with $V_{IN} = V_{BIAS} = 3.3$ V

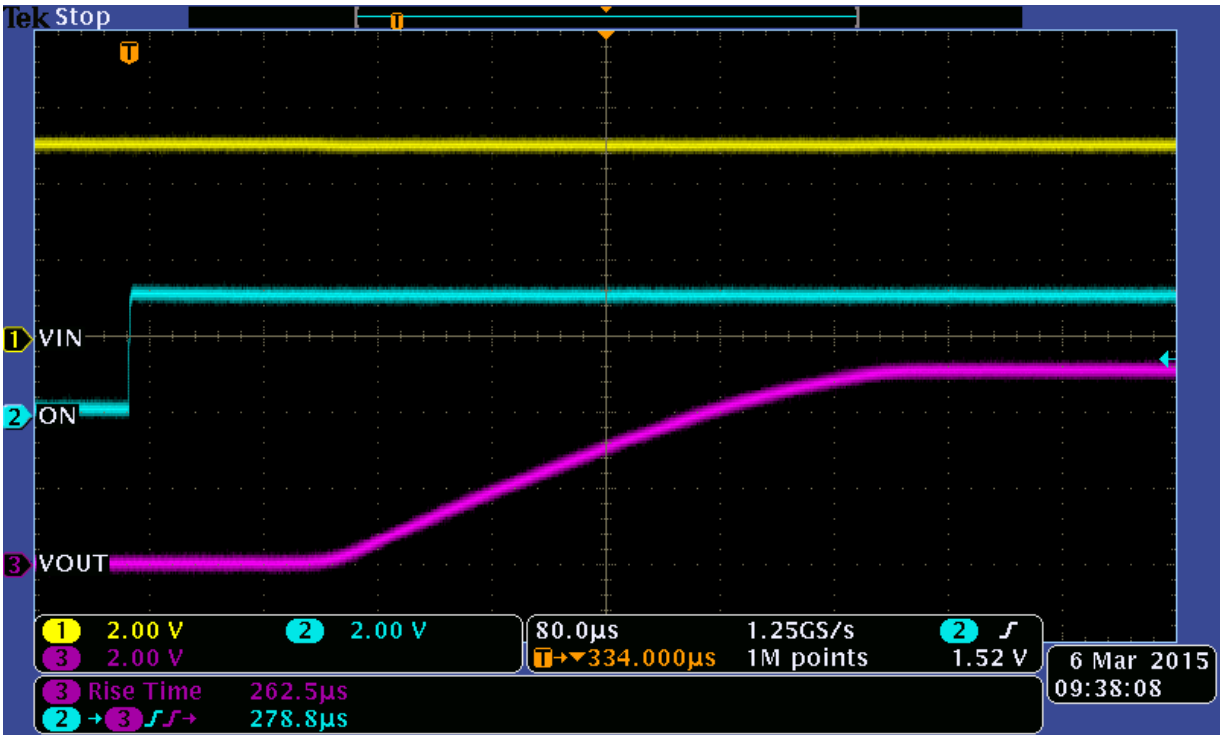

Figure 8. Dual TPS22966 Turn On Waveform with V_{IN} = V_{BIAS} = 5 V

8 Triple TPS22959 Test Data

This section will cover the test data from the triple TPS22959 circuit.

8.1 ON Resistance vs. Load Current

Table 6 provides a summary of the ON Resistance measured at various loads:

Table 6. ON Resistance vs. Load Current

LOAD CURRENT	V_{IN} = V_{BIAS} = 5 V	V_{IN} = V_{BIAS} = 3.3 V
200 mA	1.4 mΩ	1.4 mΩ
1 A	1.4 mΩ	1.4 mΩ
5 A	1.4 mΩ	1.4 mΩ
10 A	1.4 mΩ	1.4 mΩ
15 A	1.5 mΩ	1.5 mΩ
30 A	1.6 mΩ	1.7 mΩ

8.2 Turn On Waveforms

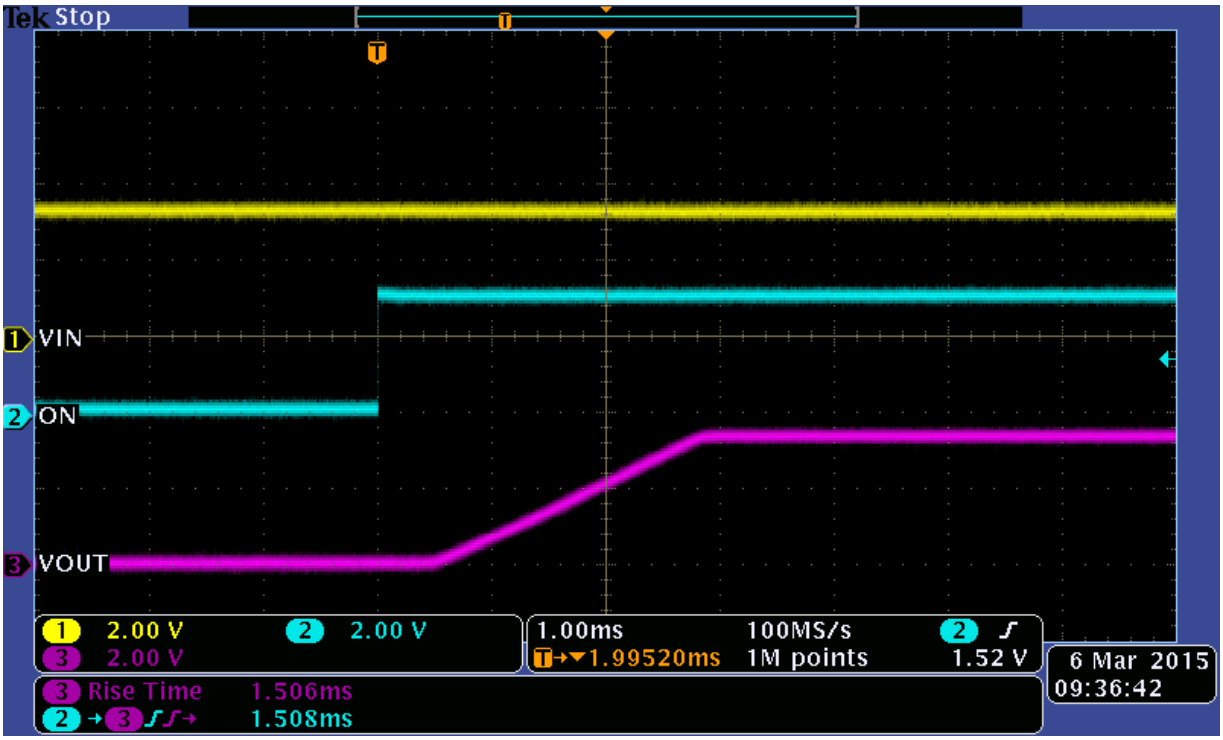

Figure 9. Triple TPS22959 Turn On Waveform with V_{IN} = V_{BIAS} = 3.3 V

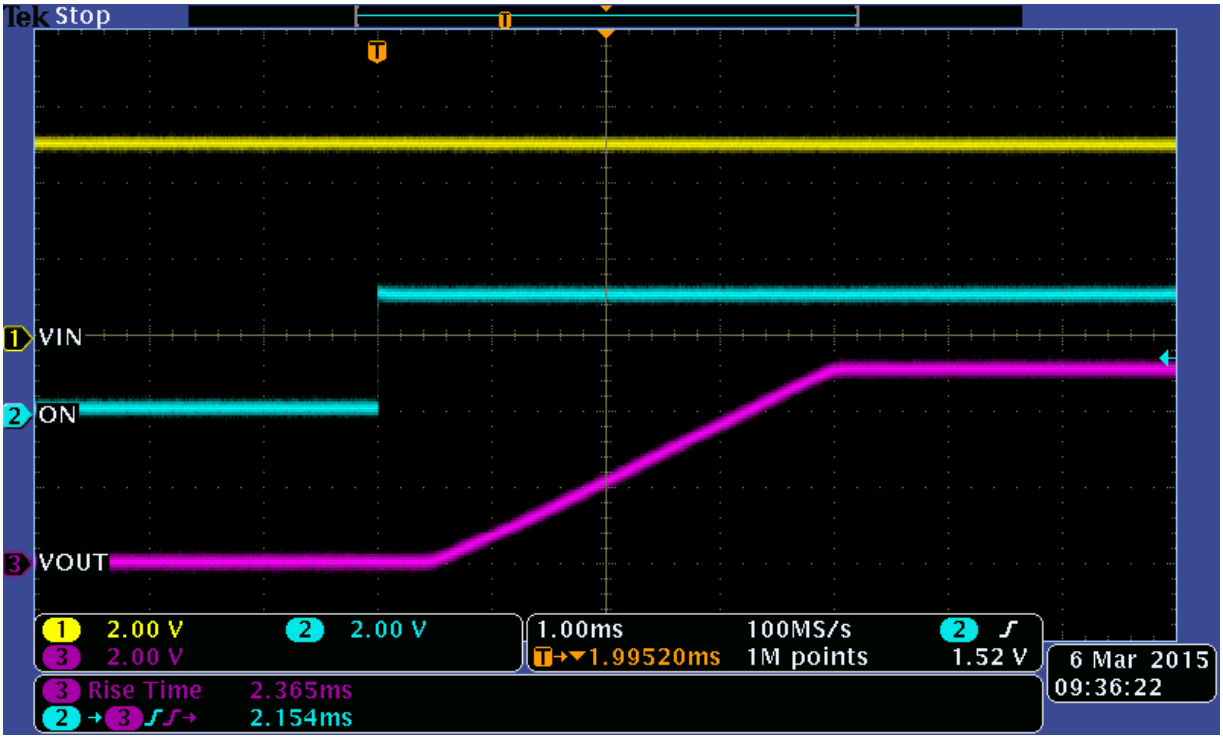

Figure 10. Triple TPS22959 Turn On Waveform with V_{IN} = V_{BIAS} = 5 V

9 Design Files

9.1 Schematics

To download the Schematics, see the design files at TIDA-00513.

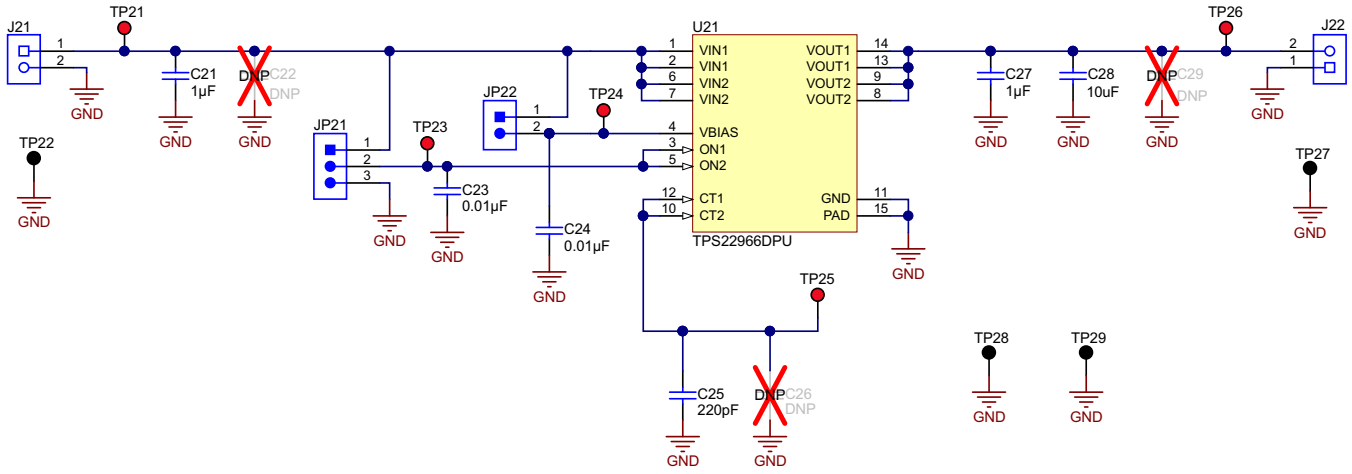

Figure 11. Dual TPS22966 Schematic

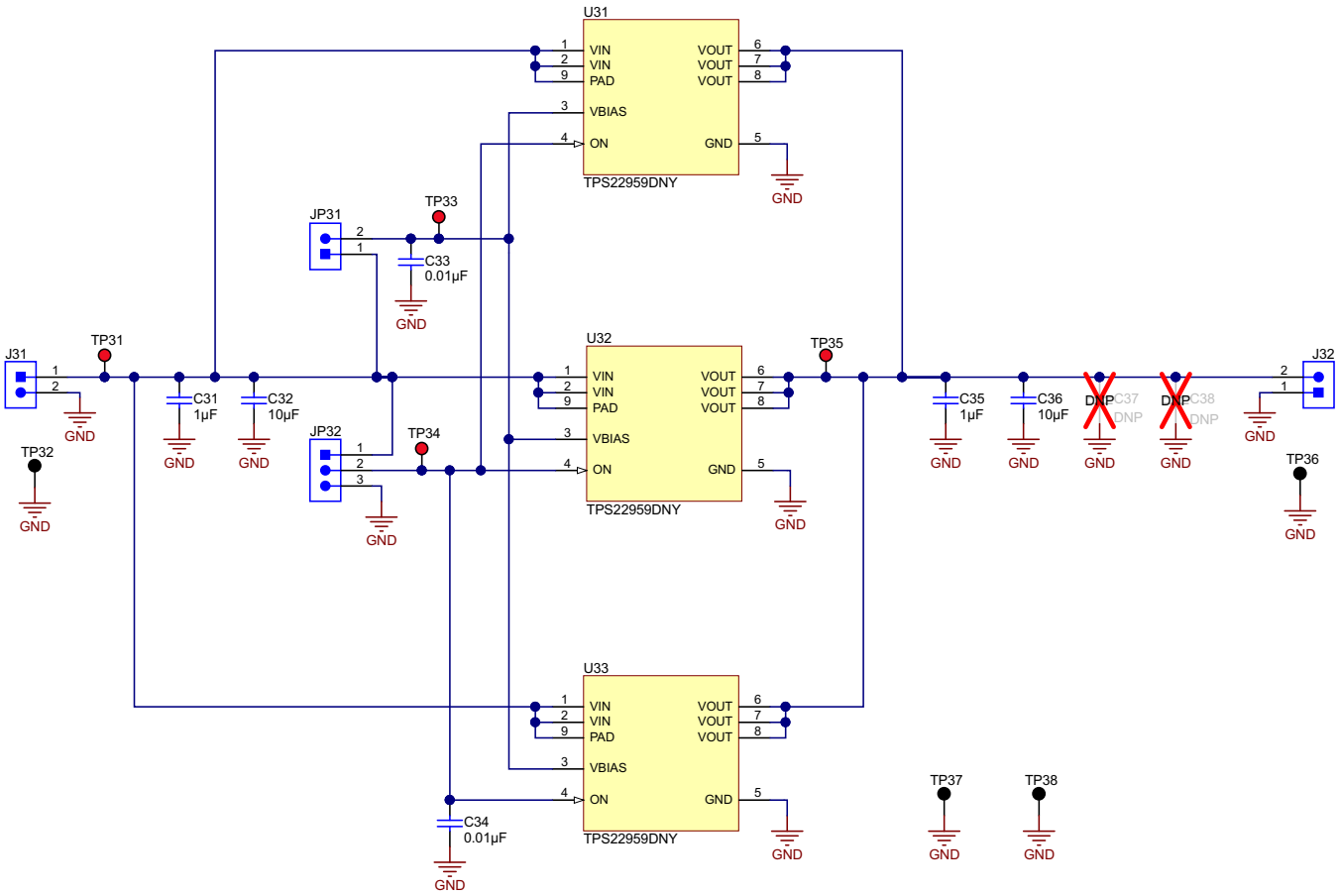

Figure 12. Triple TPS22959 Schematic

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00513.

9.3 Layout Recommendations

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace should be as short as possible to avoid parasitic capacitance.

9.4 Layer Plots

To download the layer plots, see the design files at TIDA-00513.

9.5 Altium Project

To download the Altium project files, see the design files at TIDA-00513.

9.6 Layout Guidelines

To download the Layout Guidelines, see the design files at TIDA-00513.

9.7 Gerber Files

To download the Gerber files, see the design files at TIDA-00513.

9.8 Software Files

To download the software files, see the design files at TIDA-00513.

10 References

1. Texas Instruments Application Report, *Load Switch Thermal Considerations*, 2004 (SLVUA74)

11 About the Author

ADAM HOOVER is a Systems Engineer at Texas Instruments, where he is responsible for developing solutions for the industrial segment. Adam earned his Bachelors of Science in Electronics Engineering Technology (EET) from Texas A&M University in College Station, TX.

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