TIDA-00628

TI Designs

85Vac – 440Vac input, UCC28722 based, 15V, 6.5W Snubber-less Flyback Converter using BJT primary switch

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Design Resources

TIDA-00628

UCC28722

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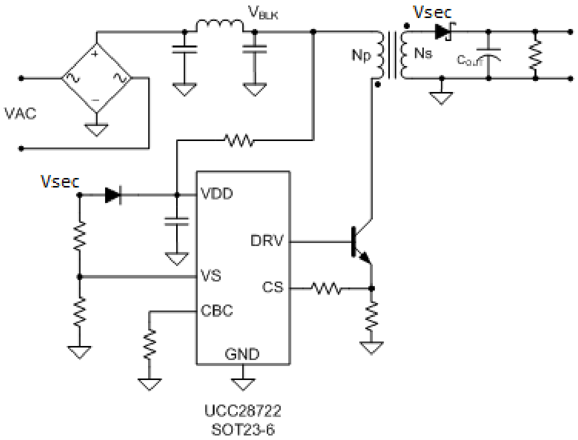
Block Diagram



Design Features

15V, 6.5W non-isolated power supply design which can tolerate input voltage range from low line (85Vac) to peak of 3 phase line-line (440Vac) with minimum component count and system cost

- Flyback for low power applications
- Output Voltage : 15V-dc
- Output Current : 0.433A
- Constant Output current Limit : 0.5A
- Output Over Voltage protection
- Input voltage up to 440Vrms
- No snubber - reduces system cost and PCB area
- BJT switch to reduce system cost
- Non Isolated output reduces transformer complexity
- Conducted Emissions: CISPR 22, Class B
- Operating temperature : - 40°C to 85°C

Featured Applications

- Industrial power supplies
- Bias supplies in 3 phase systems

Board Image

1 Key System Specifications

Parameter	Specification			
	Min	Typ	Max	Units
Input voltage	85	220	440	Vrms
Input Line Frequency	47	50	63	Hz
Output Voltage	14.5	15	15.5	V
Output Over Voltage		17		V
Output Under Voltage		12		V
Output Current	0.043		0.433	A
Output ripple & noise			150	mVpp
Startup Time			2	s
Load transitent Output Voltage deviation (Min - Max % load step)			0.5	V
EMC Compliance	CISPR22 Class B			

Table 1

2 System Description

In 3 phase systems where there is the potential for the netural connection to drift due to unbalanced loading on the phases, or for equipment to be wrongly connected from phase to phase rather than phase to neutral, voltages of circa 440-500Vac can be seen at the input to the unit.

This input voltage range significantly exceeds the 264Vrms maximum voltage specification of most universal input and hence requires changes to the input stage and possibly the primary switch.

In this design a TVS and High voltage MosFET are used at the input to clamp the bulk capacitor voltage below 450V, which allows only one bulk capacitor to be used, even in the presence of input voltages higher than the normal universal input voltage range.

A high voltage BJT is used as the main primary switch which reduces the system cost as HV BJTs are cheaper than high voltage MosFETs and also the higher voltage rating of the BJT means that a snubber is not required, further reducing the system cost.

This BJT is driven by the UCC28722 controller. The UCC28722 is a primary side regulated flyback controller with a current source output designed for driving BJT's as the flyback main switch.
This design is a single output flyback with a nominal output voltage of 15V.

Because the output is not isolated from the input, the output winding can be used to power the IC and also used as the sense winding for output voltage control. Thus no bias winding is required and the transformer complexity is reduced.

2.1 UCC28722

The UCC28722 is a Primary side regulated flyback controller, but as mentioned above, because this is a non-isolated application the feedback can be fed back directly from the output, also increasing the regulation accuracy and reducing the complexity of the system.

The controller provides constant current regulation and overvoltage protection as well as output voltage regulation.
The controller operates in discontinuous conduction mode with valley-switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range.
The controller also offers output over-voltage protection and input brown out protection features.

2.1.1 UCC28722 Features

- Dynamic BJT Drive information from the primary power switch and flyback winding for precise control of the output
- 80-kHz Maximum Switching support high efficiency operation at all load levels without sacrificing output transient
- Quasi-Resonant Valley-Switching Operation for Highest Overall Efficiency
- Wide VDD Range Allows Small Bias Capacitor
- Output Overvoltage, Low-Line, and Overcurrent Protection Functions
- SOT23-6 Package

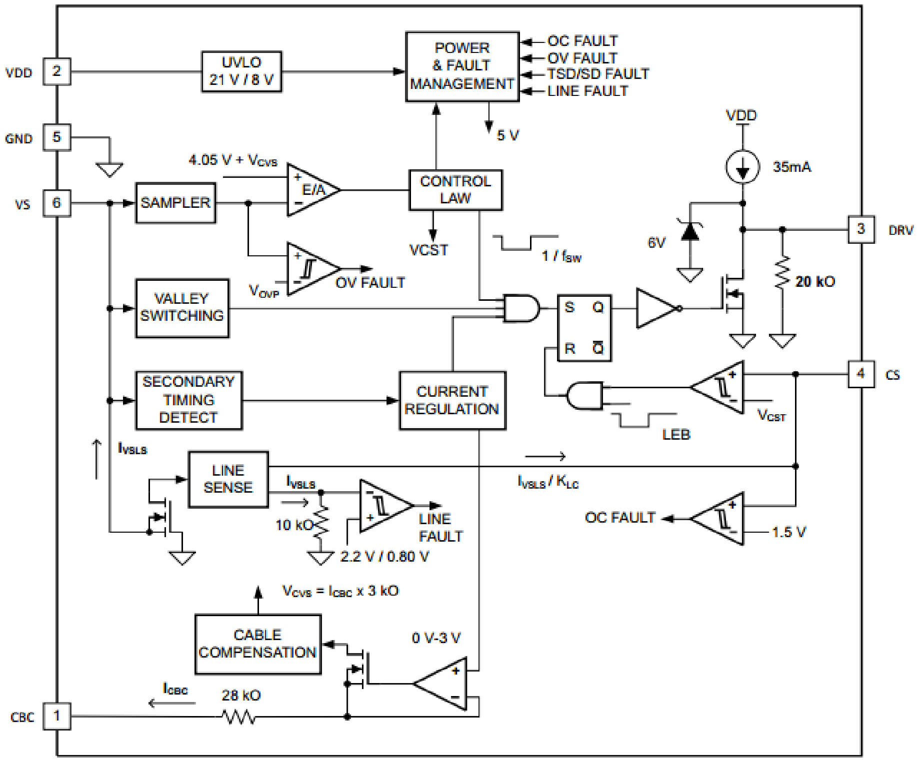


Figure 1 : UCC28722 Functional Block Diagram

3 System Design

3.1 Input stage

Resistor R1 is a fusible resistor. It limits the inrush current and provides protection in case of component failure causing a short circuit downstream of the fuse. Excessive current causes the fusible resistor to fail open circuit.
It also provides some attenuation during surge voltage events at the input to the converter.

A position is also provided for a MOV to be fitted for further line voltage surge attenuation.

D1 provides half wave rectification of the input sine wave. D7 is added to improve the conducted emissions from the unit. If EMI filtering is not required D7 can be removed.

An input voltage range of 440Vrms (~622Vdc) is specified which means that the standard approach of using a 400Vdc rated bulk cap to support the output during ac peaks and during the holdup period is not possible.

One possible approach is to use stack two 400V bulk caps in series to double the voltage rating. However since putting capacitors in series reduces their effective capacitance, both capacitors must have twice the required capacitance, so four times the required bulk capacitance are needed to increase the voltage rating in this way.

Another approach is to use a TVS or some other voltage clamp device to clamp the voltage before rectifying it onto the bulk capacitor as shown below. This circuit requires a high voltage MosFET and TVS or MOV but removes the need for two bulk caps in series. One 450Vdc bulk cap can now be used.

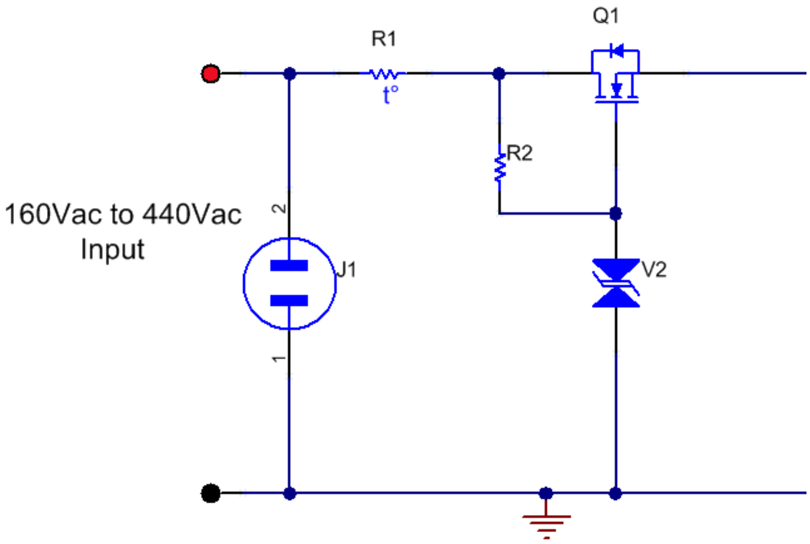


Figure 2 : Input Clamp Circuit

A differential mode filter is inserted between the clamp and the bulk capacitor to filter the voltage developed across the bulk capacitor ESR by the switch current and the voltage swing across the transformer interwinding capacitance. Values are based on testing for particular transformer construction, PCB layout etc.

For a half wave rectified input the required bulk capacitance can be estimated from the formula.

$$C_{BULK(min)} = \frac{\frac{2 \times P_{IN}}{f_{LINE(min)}} \times \left[\frac{1}{RCT} - \frac{1}{2 \times \pi} \times arccos\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right]}{2 \times V_{IN(min)}^2 - V_{BULK(min)}^2}$$

Where

RCT = 1 for a half wave rectified input (shown as a solid grey line in the figure below), and
= 2 for a full wave rectified input (shown as a dashed grey line in the figure below)

The bulk cap voltage is shown in black

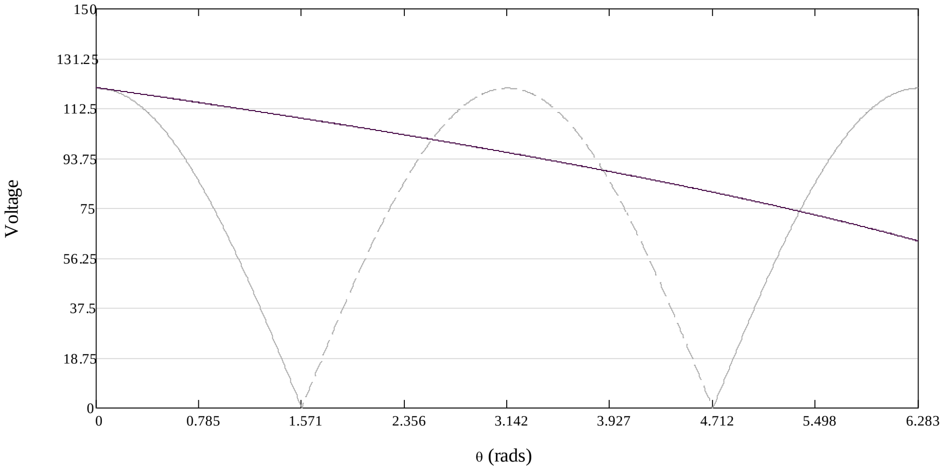


Figure 3 : Input Voltage and Bulk Cap Voltage

And

- $P_{in} = \frac{V_{out} * I_{out}}{\eta}$
- $V_{bulk(min)} = 75V$
- $V_{in(min)} = 85V$

A bulk capacitor of 33uF was used in this design.

3.2 Transformer Turns Ratio

The first consideration for the transformer is what reflected voltage to chose.
The reflected voltage and max on and off duty cycles will dictate the minimum bulk voltage at which the load can be supplied.

The maximum secondary diode conduction duty cycle is 42.5%. From equation 14 of the datasheet

$$\mathrm{D_{max}} = 1 - \left(\frac{\mathrm{t_R}}{2} \cdot \mathrm{f_{max}}\right) - \mathrm{D_{MAGCC}}$$

(and targeting a maximum switching frequency of 65kHz), this gives a maximum duty cycle of ~50%.

Therefore the minimum bulk voltage which can support the load is

$$\mathrm{V_{bulk\_min}} = \frac{\mathrm{V_{reflected}} \cdot \mathrm{D_{MAGCC}}}{\mathrm{D_{max}}}$$

A reflected voltage of ~70-71V was chosen as it is close to the minimum bulk voltage at low line, giving a minimum bulk voltage to maintain regulation of ~ 60V.

This results in a turns ratio of 4.54 to the 15V winding, assuming a schottky diode drop of 0.5V on the output.

$$N = \frac{V_{reflected}}{V_{out\_15} + V_{rect}} = 4.5$$

As will be seen later, the eventual turns ratio is 4.47

3.3 Current Sense Resistance

A current limit of 120% of the maximum load current is chosen to allow some margin before entering constant current limit operation. Above this level the output voltage will decrease with increasing load.

P_{max} = 6.5W, therefore P_{limit} = 7.8W. This is equivalent to a current of 0.506A on the 15V output.

From equation 16 in the datasheet the current sense resistor is therefore

$$\mathrm{R_{cs}} = \frac{\mathrm{V_{ccr}} \cdot \mathrm{N} \cdot \sqrt{\eta_{\mathrm{traffo}}}}{2 \cdot \mathrm{I_{limit}}} = 1.351\Omega$$

Choosing an Rcs of 1.35Ω gives a peak primary current of

$$\mathrm{I_{pk\_pri}} = \frac{\mathrm{V_{cs\_max}}}{\mathrm{R_{cs}}} = 0.577\mathrm{A}$$

And an inductance of

$$\mathrm{L} = 2 \cdot \frac{\mathrm{P_{limit}}}{\eta_{\mathrm{traffo}}} \cdot \left(\frac{\mathrm{R_{CS}}}{\mathrm{Vcs_{max}}}\right)^2 \cdot \frac{1}{\mathrm{f_{sw}}} = 881\ \mu\mathrm{H}$$

3.4 Transformer Design

An E16/8/5 is chosen as the transformer core size. A small transformer may be sufficient to transfer the power but the higher number of turns and the narrower winding window would result in a higher layer count, which would reduce the efficiency significantly.

Copper losses are reduced by

1) The reduced length of copper in the winding
2) The increased strand diameter allowed by the larger winding window
3) The reduction in AC resistance with the reduced number of layers.

Reducing the number of layers also has the significant effect of reducing the leakage inductance, which

1) Increasing the efficiency
2) Reducing the magnitude of the leakage inductance ring, which reduces the electromagnetic emissions from the unit.
3) Providing more margin to the maximum switch rated voltage.

With this core size and targeting a peak flux density of ~333mT, the following numbers of turns were chosen,

N_{pri} = 76
N_{sec} = 17

3.5 Output capacitor

The output capacitor must be sized to handle the output rms ripple current.
The rms ripple current can be calculated as

$$\mathrm{Iout_{ripple}} = \sqrt{\mathrm{Isec_{rms}}^2 - \mathrm{Iout_{max}}^2}$$

$$\mathrm{Isec_{rms}} = \mathrm{I_{pk\_pri}} \cdot \mathrm{N} \cdot \sqrt{\frac{\mathrm{D_{MAGCC}}}{3}} = 0.931\mathrm{A}$$

The ripple current rating of the capacitor is given in the datasheet.

For stability, it is also recommended that the output capacitance is greater than

$$\mathrm{Cout} > \frac{400 \cdot \mathrm{I_{limit}}}{\mathrm{Vout} \cdot \mathrm{fsw_{max}}} \approx 270\ \mu\mathrm{F}$$

3.6 Output Voltage Ripple

The output voltage ripple is equal to

$$\mathrm{Vout}_{\mathrm{ripple}} = \mathrm{I}_{\mathrm{pk\_pri}} \cdot \mathrm{N} \cdot \mathrm{Z}_{\mathrm{Cout}}$$

Where Z_{cout} is the complex impedance of the output capacitance.
Z_{cout} is approximately equal to

$$\mathrm{Z}_{\mathrm{Cout}} = \sqrt{\frac{\mathrm{D}_{\mathrm{MAGCC}}}{2 \cdot \pi \cdot \mathrm{f}_{\mathrm{sw}} \cdot \mathrm{C}_{\mathrm{out}}}^{2} + \mathrm{ESR}_{\mathrm{C}_{\mathrm{out}}}{}^{2}}$$

This equation assumes that the ESL of the capacitor is negligible at the switching frequency.

It may be necessary to place some ceramic capacitance is placed across the output to filter out higher order harmonics of the switching frequency, where the ESL of the electrolytic is not necessarily negligible.

This ceramic capacitance also affects the complex impedance of the output capacitance network. This effect can be accounted for in the calculation but the equation becomes significantly more complicated. The impact can be neglected to a first order.

If the output ripple is greater than desired, extra output capacitance may be required or in some cases an output filter.

3.7 Transient Response

The transient response of the unit is given by

$$\Delta\mathrm{Vout} = \frac{\mathrm{I}_{\mathrm{tran}}}{\mathrm{C}_{\mathrm{out}}} \cdot \left(\frac{1}{\mathrm{fsw}_{\mathrm{pre\_tran}}} + 150\mu\mathrm{s}\right)$$

Where

I_{tran}	=	the maximum transient load step
fsw_{pre_tran}	=	the minimum switching frequency before the load step occurs. This will be set by the minimum load present before the load step and has a big impact on the transient performance and required output capacitance.

If the output transient deviation is too large, more output capacitance may be required.

Two 150uF capacitors were used in this design.

3.8 Vdd Capacitance

The Vdd capacitance is sized, as described in the datasheet, according to the formula.

$$\mathrm{C_{DD}} = \frac{\left[\mathrm{I_{run}} + \mathrm{I_{DRS(max)}} \cdot \mathrm{D_{Max}}\right] \cdot \frac{\left(\mathrm{C_{out}} \cdot \mathrm{V_{out\_UV}}\right)}{\left(\mathrm{I_{limit}} - \mathrm{I_{load}}\right)}}{\mathrm{Vdd_{on}} - \mathrm{Vdd_{off}}}$$

Where

$\mathrm{I_{run}}$ = the current consumption of the IC

$\mathrm{I_{DRS(max)}}$ = the maximum switch drive current. Using this figure gives some margin on the choice of Vdd capacitance and the current drawn will actually equal the average drive current, not the maximum drive current.

$$\mathrm{C_{DD}} = \frac{[3\mathrm{mA} + 42\mathrm{mA} \cdot 0.575] \cdot \frac{(300\mu\mathrm{F} \cdot 10\mathrm{V})}{(.506 - 0.043)}}{19 - 8.3} = 12.8\mathrm{uF}$$

A 22uF alumimum electrolytic capacitor were used in this design. This will allow the unit to start into ~ 50% load.
Note; if using ceramic capacitors as the bias capacitors that the capacitance of ceramic caps decreases with bias voltage. The decrease varies from part to part but for some parts the capacitance can be below 50% of it's nominal value when it has half it's rated voltage across it.

3.9 Startup resistor

The startup resistor is chosen based on the required startup time according to the equation;

$$\mathrm{R_{startup}} = \frac{\mathrm{Vacpk}}{\mathrm{I_{dd\_start}} + \frac{\mathrm{Vdd_{on}} \cdot \mathrm{C_{Vdd}}}{\mathrm{T_{start}}}}$$

For a 2s startup time at Vacpk_min this gives

$$\mathrm{R_{startup}} = \frac{127\ \mathrm{V}}{1\mathrm{mA} + \frac{19\mathrm{V} \cdot 22\mu\mathrm{f}}{2\mathrm{s}}} = 572\mathrm{k}\Omega$$

Two 270kΩ resistors in series were used to maintain high voltage spacing from the bulk cap. This gives a startup time of 1s at 220Vac.

3.10 Output voltage Sense Resistors

The output voltage sense resistors are also chosen per the datasheet equations.

$$R_{S1} = \frac{\sqrt{2} \cdot Vin_{min}}{N_{PA} \cdot I_{VSL\_run}}$$

$$R_{S2} = \frac{R_{S1} \cdot V_{VSR}}{N_{AS} \cdot (Vout + V_F) - V_{VSR}}$$

Where

I_{VSL_run} = The Vs line-sense run current

V_{VSR} = The regulation voltage at the Vs pin

V_F = The forward drop of the output regulator

N_{PA} = The primary to auxiliary turns ratio. If the secondary and auxiliary have the same number of turns, as in this design, this is equal to N.

N_{AS} = The secondary to auxiliary turns ratio. If the secondary and auxiliary have the same number of turns, as in this design, this is 1.

$$R_{S1} = \frac{\sqrt{2} \cdot 85}{4.47 \cdot 225mA} = 119.5k\Omega$$

A 120kΩ resistor was used.

$$R_{S2} = \frac{120k\Omega \cdot 4.05V}{(15V + 0.5V) - 4.05V} = 42.27k\Omega$$

A 42.2kΩ resistor was used.

3.11 Line Feed-forward Resistor

$$R_{LC} = \frac{K_{LC} \cdot R_{S1} \cdot R_{CS} \cdot t_D \cdot N_{PA}}{L_P}$$

t_D = current-sense delay including NPN transistor turn-off delay, add ~50 ns to transistor delay

K_{LC} = a current-scaling constant given in the electrical characteristics section of the datasheet.

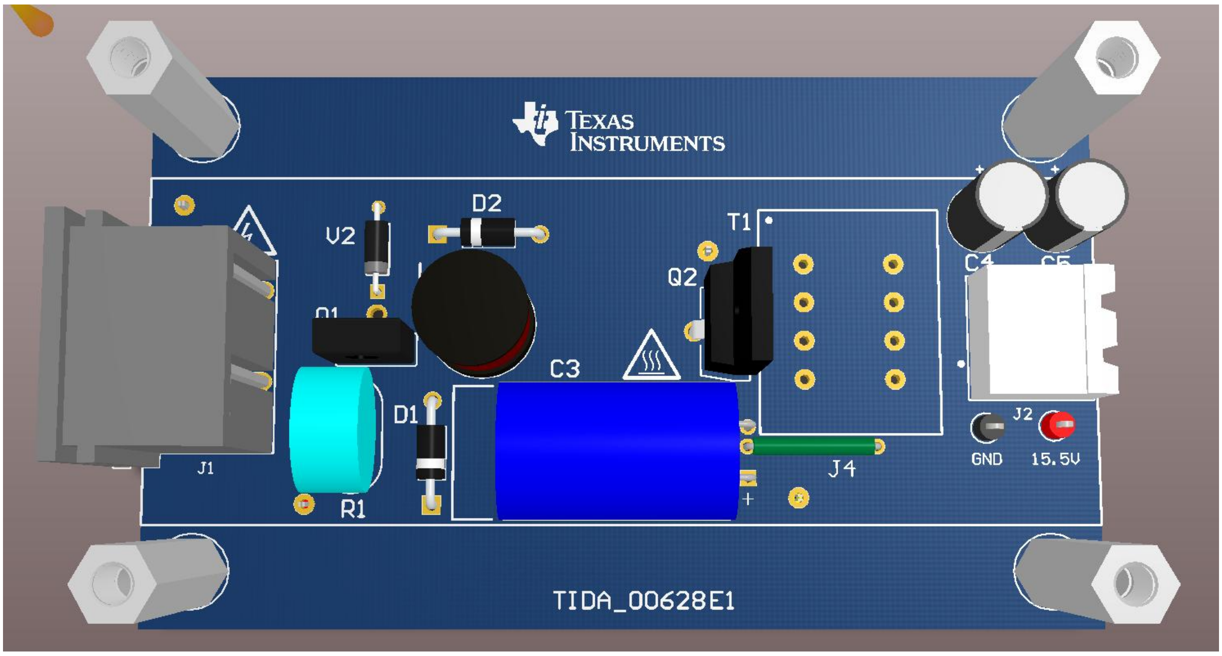
$$R_{LC} = \frac{25 \cdot 120k\Omega \cdot 1.35\Omega \cdot 150ns \cdot 4.47}{881mH} = 3.07k\Omega$$

A 3.09kΩ resistor was used.

4 Getting Started Hardware

4.1 Hardware Overview.

The design hardware is shown in Figure 4. A standard figure-of-8 AC receptacle is used on the input. The load is connected to terminal block J2. J3 on the BoM is the mating part into which the load terminal wires may be screwed.
The board should always be operated within the conditions specified in Table 1 above.



5 Test Data

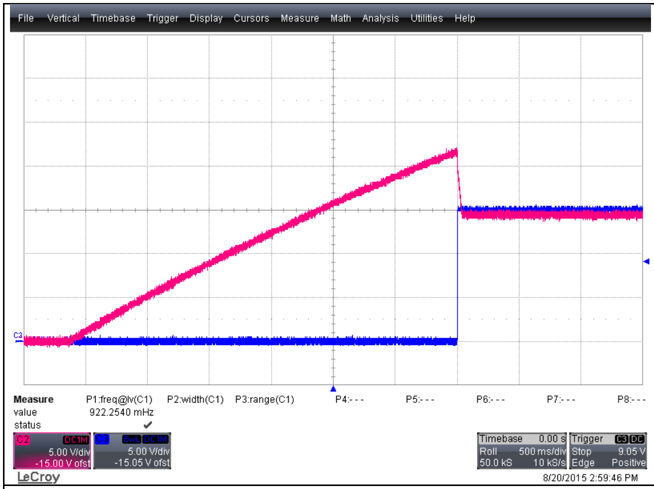
The results shown below are taken at 220Vac input except where specified otherwise.

5.1 Efficiency

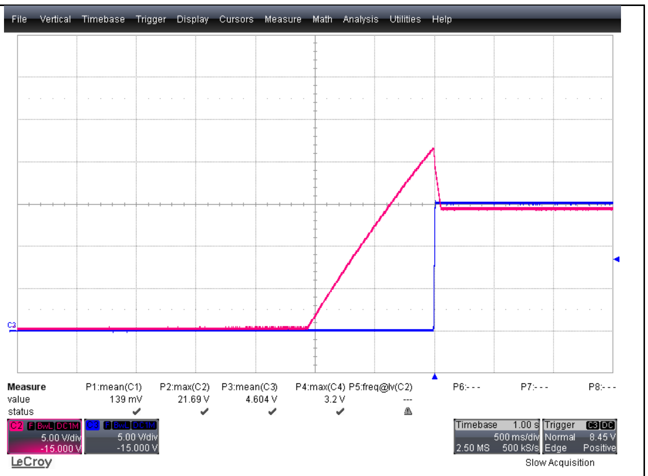
(V)	(Hz)	Pin (W)	(V)	(A)	Pout (W)	Eff (%)
230	50	1.043	15.085	0.043	0.648	62.07
		1.898	15.073	0.092	1.384	72.92
		2.768	15.074	0.141	2.121	76.61
		3.653	15.085	0.190	2.860	78.28
		4.547	15.095	0.238	3.600	79.16
		5.447	15.102	0.287	4.340	79.67
		6.342	15.107	0.336	5.079	80.09
		7.243	15.116	0.385	5.822	80.38
		8.148	15.133	0.434	6.568	80.61
		9.055	15.153	0.483	7.317	80.81

5.2 Startup and Risetime

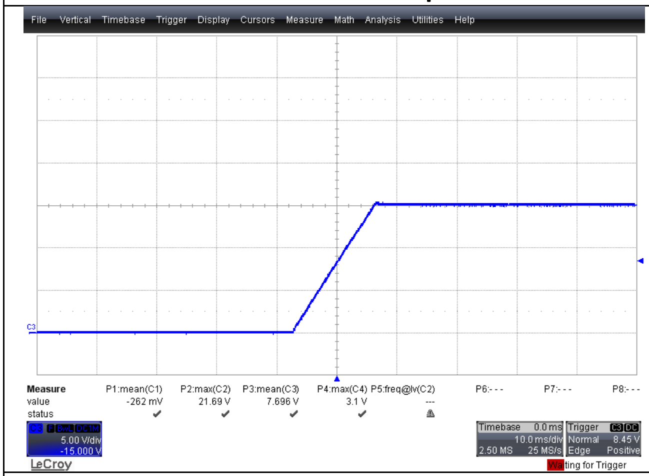
The plots below show Vbias in Pin and Vout in blue.



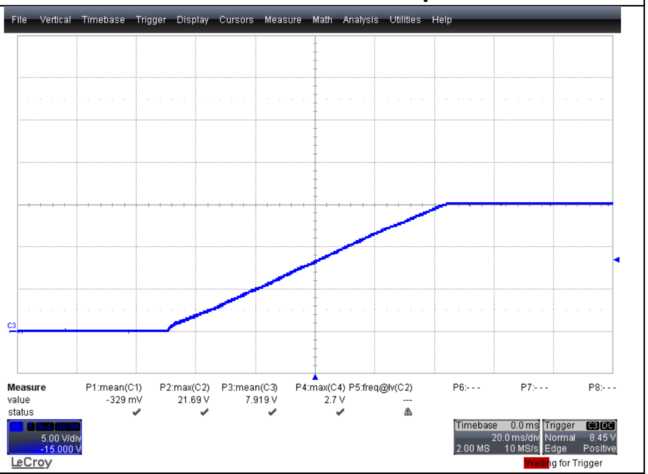
85Vac : Minimum Load startup



220Vac : Minimum Load startup



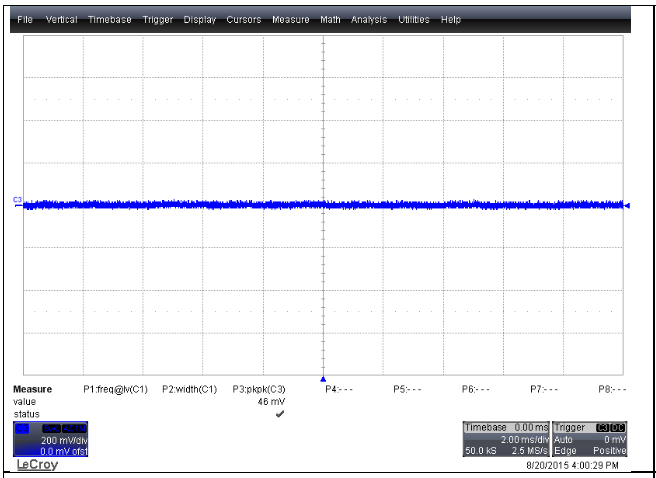
220Vac : Vout Risetime @ minimum load*



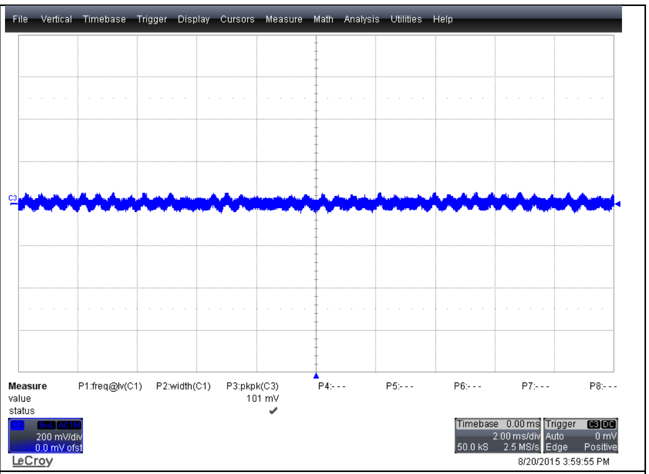
220Vac : Vout Risetime @ full load

* Risetime is independent of input voltage.

5.3 Output Ripple and Noise

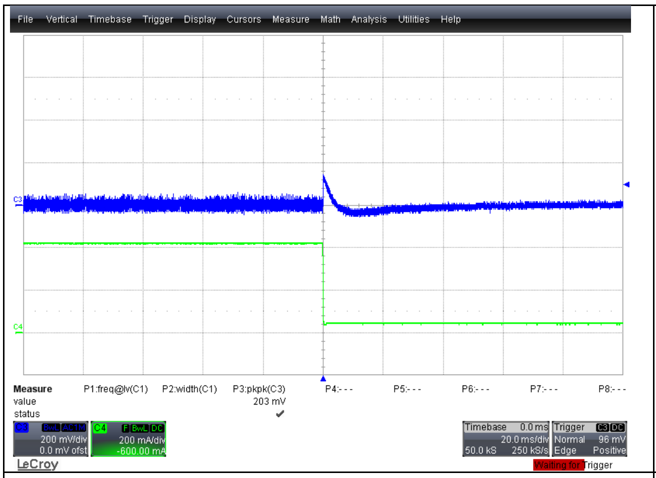


220Vac : Vout ripple @ Minimum Load

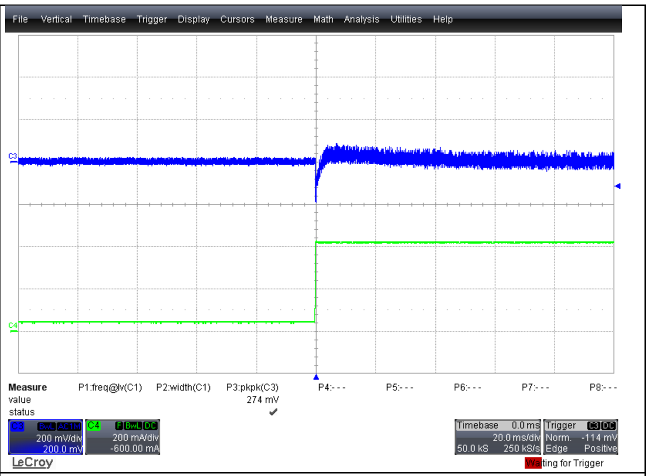


220Vac : Vout ripple @ Full Load

5.4 Transient Response

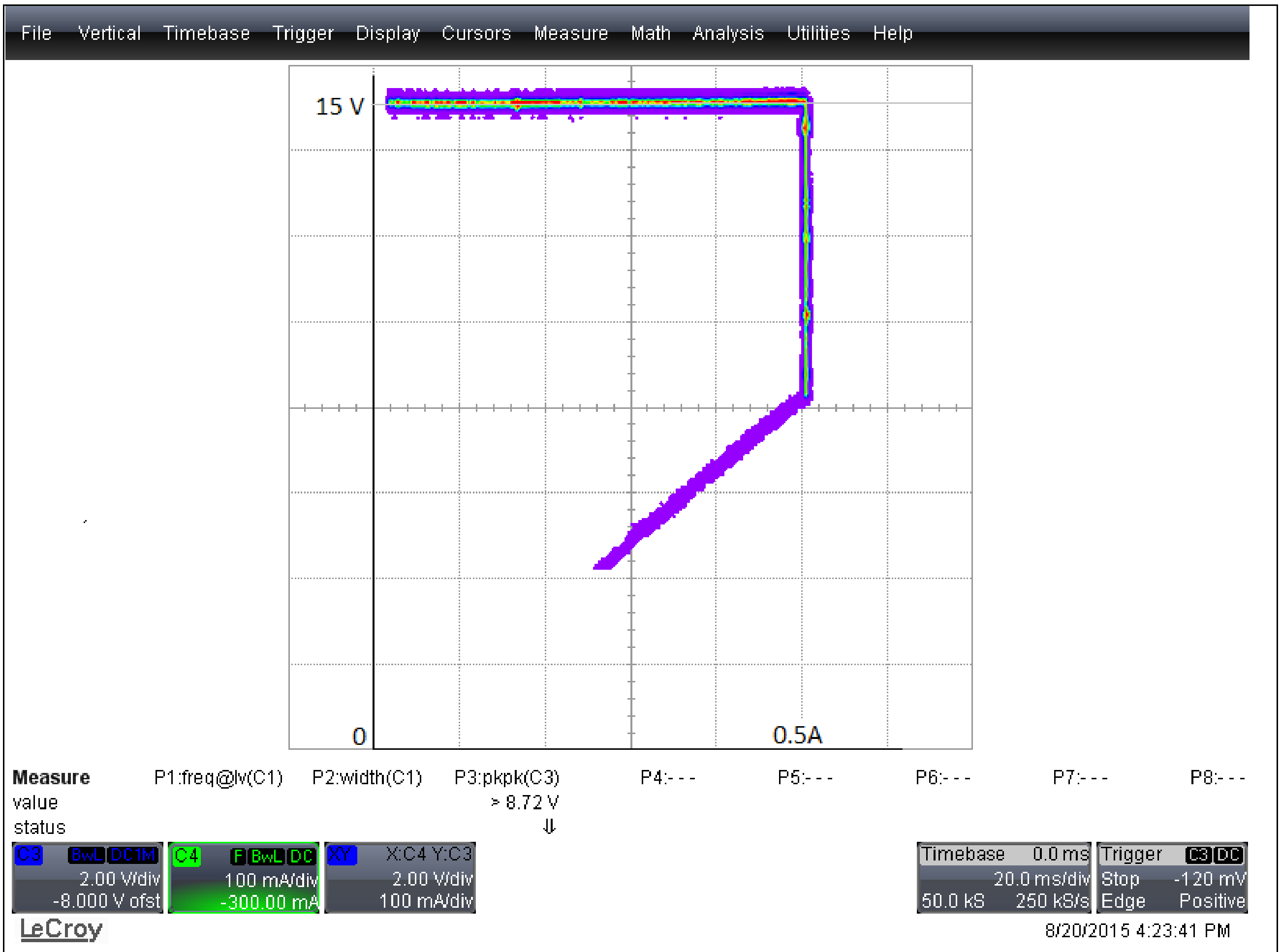


220Vac : Full load to Minimum Load step



220Vac : Minimum load to Full Load step

5.5 Output current and voltage characteristic.



```
Measure   P1:freq@lv(C1)   P2:width(C1)   P3:pkpk(C3)   P4:- - -   P5:- - -   P6:- - -   P7:- - -   P8:- - -
value                                     > 8.72 V
status                                    ⇓

C3   BwL DC1M     C4   F BwL DC      XY   X:C4 Y:C3      Timebase       0.0 ms    Trigger    C3 DC
      2.00 V/div        100 mA/div          2.00 V/div               20.0 ms/div  Stop      -120 mV
   -8.000 V ofst       -300.00 mA           100 mA/div   50.0 kS      250 kS/s    Edge      Positive
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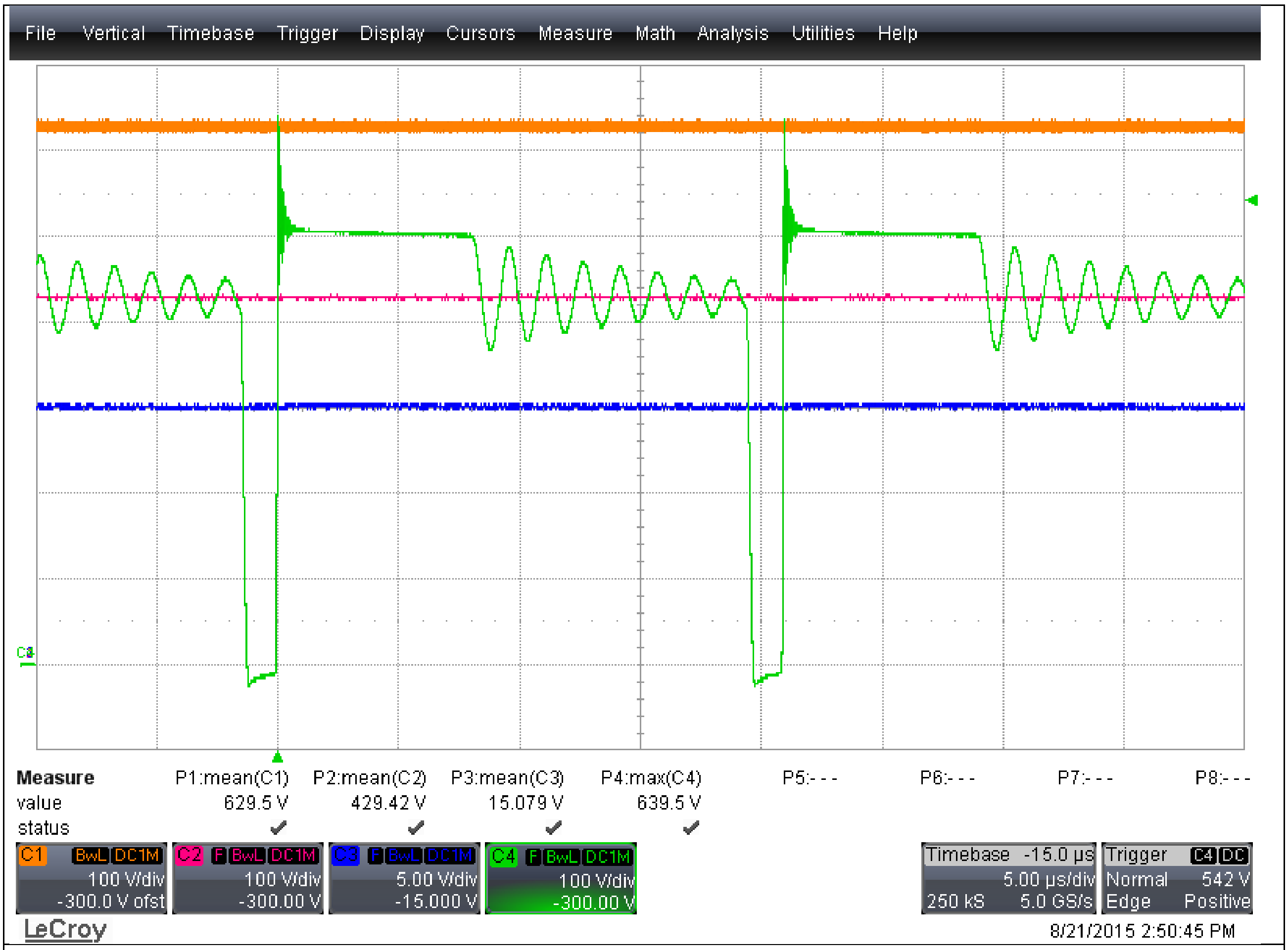
220Vac : Output voltage v Load current

5.6 Bulk voltage and Switch node voltage at 630Vdc in, full load



Measure	P1:mean(C1)	P2:mean(C2)	P3:mean(C3)	P4:max(C4)	P5:- - -	P6:- - -	P7:- - -	P8:- - -
value	629.5 V	429.42 V	15.079 V	639.5 V				
status	✓	✓	✓	✓				

C1 BwL DC1M 100 V/div -300.0 V ofst

C2 F BwL DC1M 100 V/div -300.00 V

C3 F BwL DC1M 5.00 V/div -15.000 V

C4 F BwL DC1M 100 V/div -300.00 V

Timebase -15.0 µs 5.00 µs/div 250 kS 5.0 GS/s

Trigger C4 DC Normal 542 V Edge Positive

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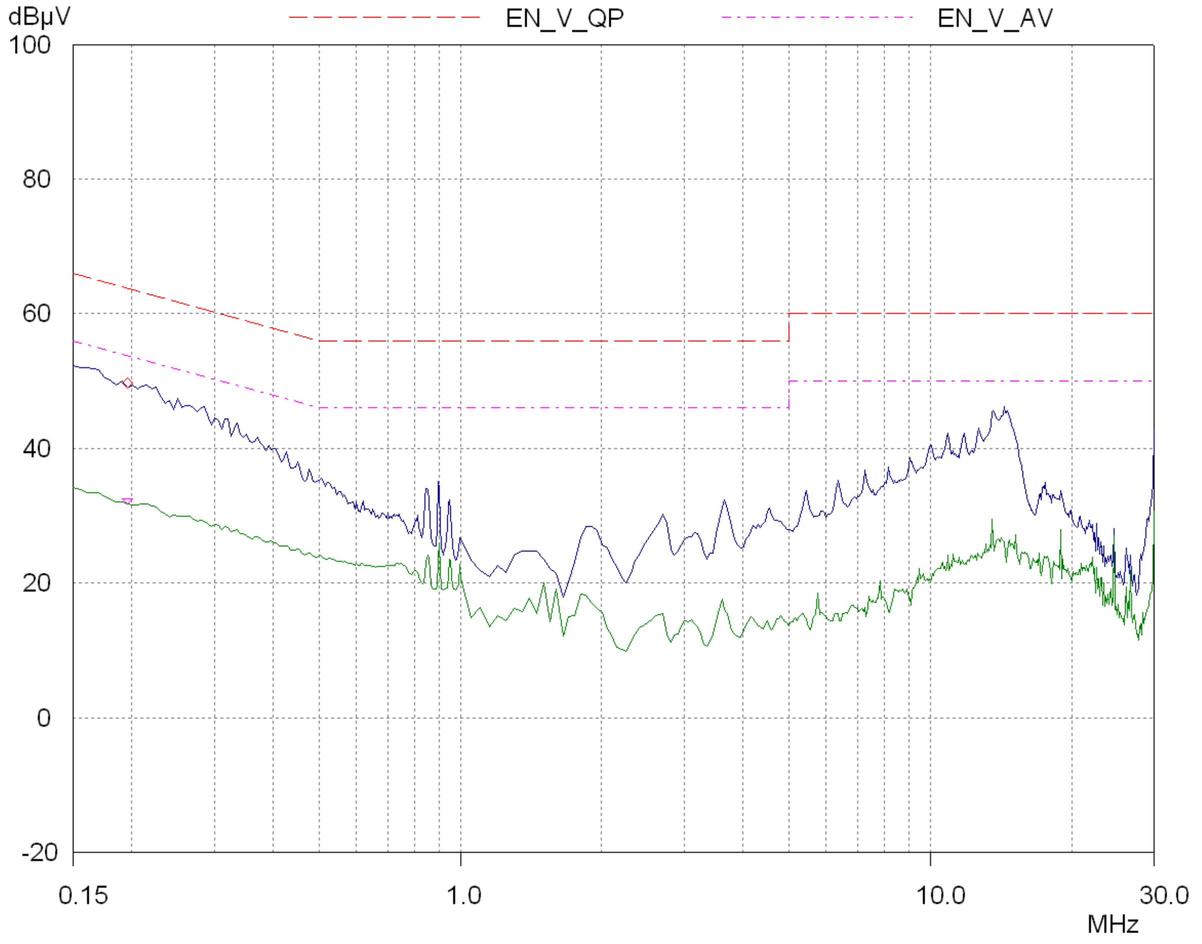
C1: Vdc input : 630V

C2: Bulk voltage after input voltage clamp : 429.5V

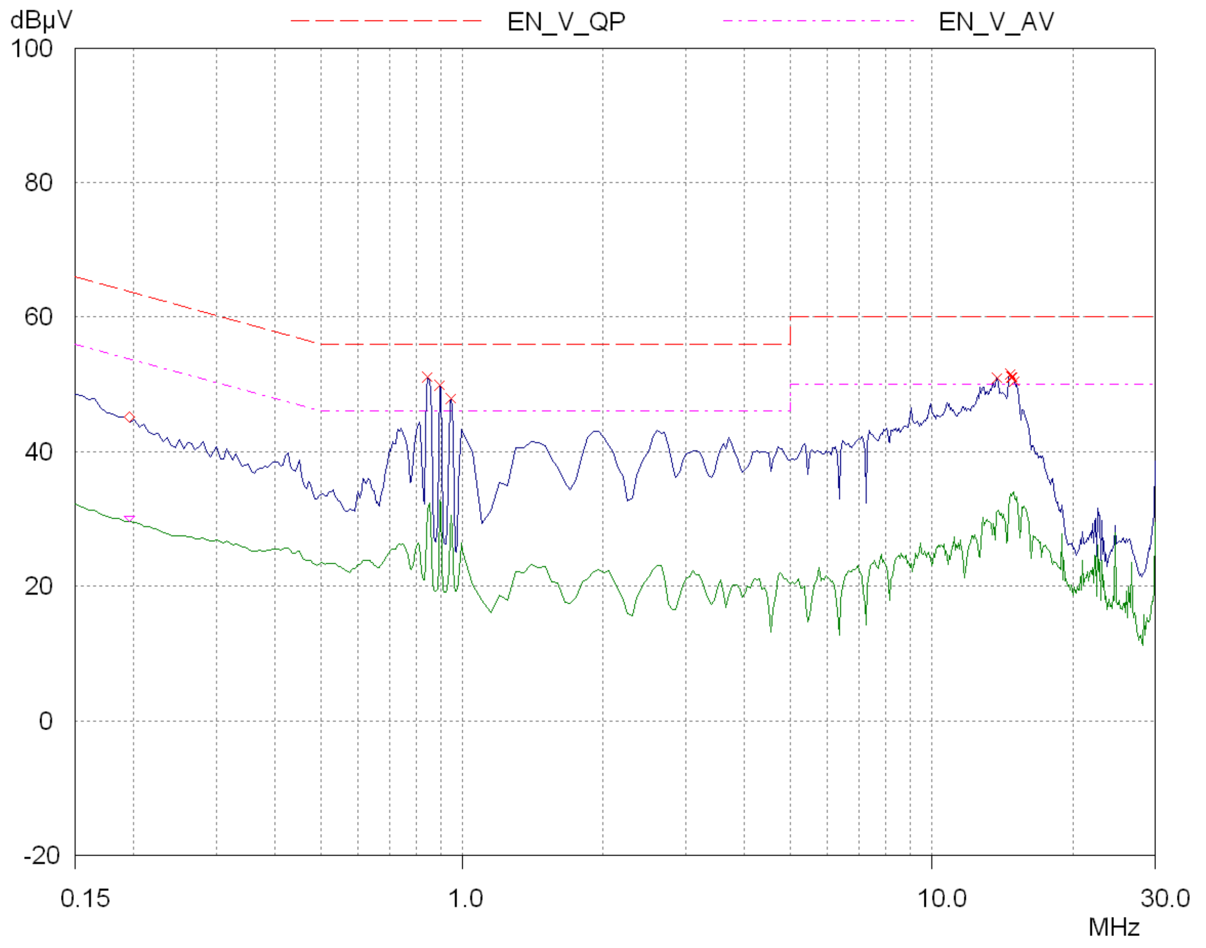
C3: Vout

C4 : Switch node voltage, peak voltage = 640V, BJT switch rating = 1050V.

5.7 EMI Measurement



Conducted Emissions, 220Vac in, 6.5W Load, L1 (Live)

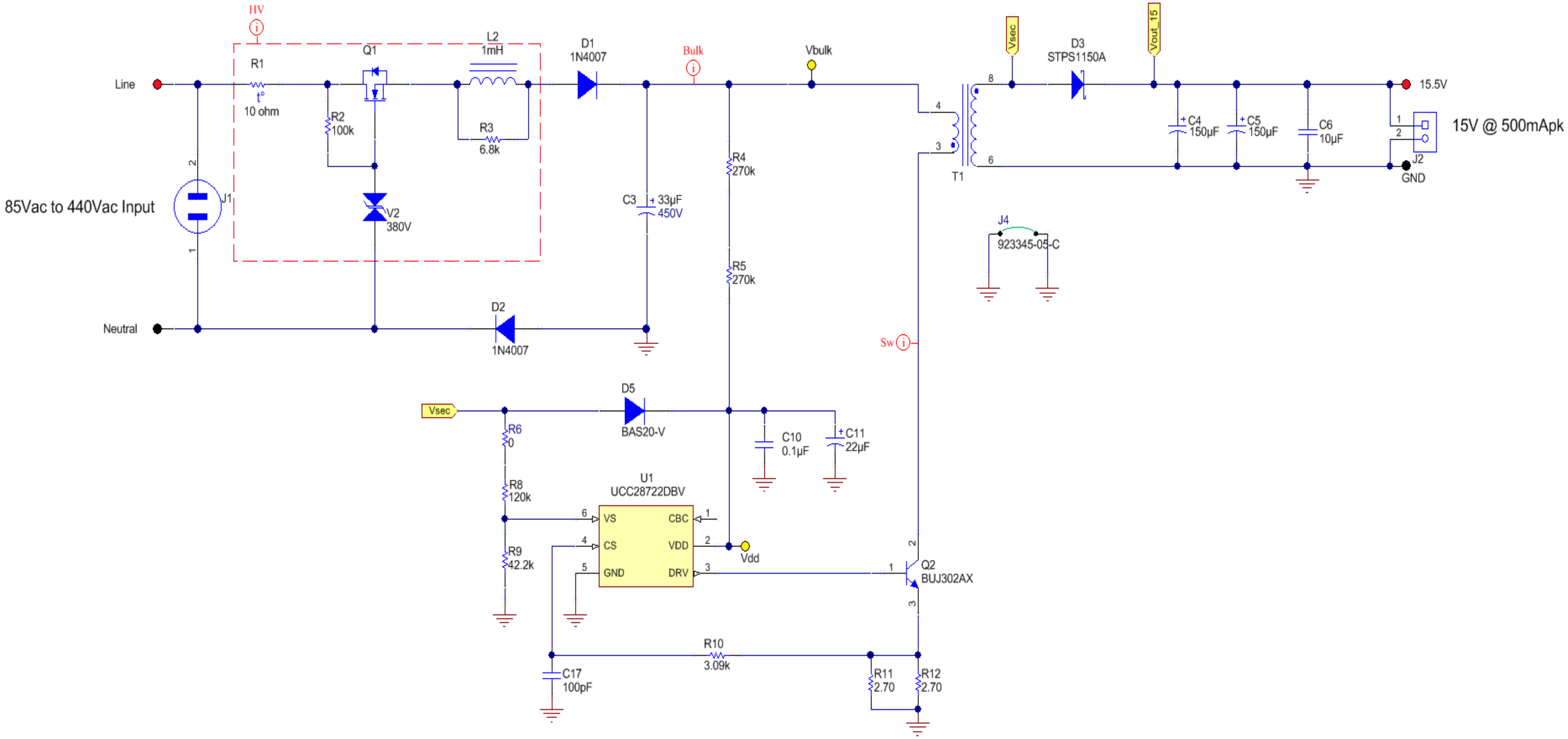


Conducted Emissions, 220Vac in, 6.5W Load, L2 (Neutral)

6 Design Files

6.1 Schematic

To download the schematic for the board, see the design files at http://www.ti.com/tool/TIDA_00628



6.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/TIDA_00628

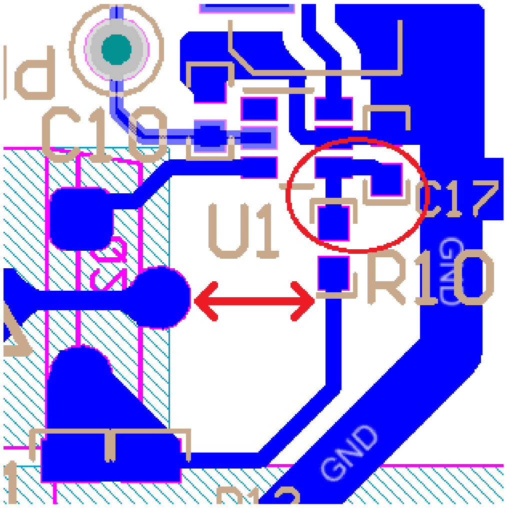
TIDA_00628
REV E1 Bill of Materials

Designator	Description	Manufacturer	PartNumber	Quantity
!PCB	Printed Circuit Board	Any		1
15.5V, Line	Test Point, TH, Miniature, Red	Keystone	5000	2
C3	CAP, AL, 33 µF, 400 V, +/- 20%, TH	Rubycon	450BXW33MEFC12.5X25	1
C4, C5	CAP ALUM 150UF 20% 25V RADIAL	United Chemi-Con	EKYB250ELL151MF11D	2
C6	CAP, CERM, 10uF, 50V, +/-10%, X7R, 1210	MuRata	GRM32ER71H106KA12L	1
C10	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	AVX	06035C104KAT2A	1
C11	CAP, AL, 22 µF, 35 V, +/- 20%, 0.76 ohm, SMD	Nichicon	UUD1V220MCL1GS	1
C17	CAP, CERM, 100 pF, 25 V, +/- 10%, X7R, 0603	AVX	06033C101KAT2A	1
D1, D2	Diode, P-N, 1000V, 1A, TH	Fairchild Semiconductor	1N4007	2
D3	Diode, Schottky, 150V, 1A, SMA	ST Microelectronics	STPS1150A	1
D5	DIODE SWITCH 200V 200MA SOD323	Vishay	BAS20-V	1
GND, Neutral	Test Point, TH, Miniature, Black	Keystone	5001	2
H1, H2, H3, H4	Standoff, Hex, 1"L #6-32 Nylon, M-F	Keystone	4820	4
H5, H6, H7, H8	Standoff, Hex, 1"L #6-32 Nylon	Keystone	1903E	4
J1	AC Receptacle, 2.5A, R/A, TH	Qualtek Electronics Corporation	770W-X2/10	1
J2	Terminal Block, 2x1, 5.08mm, TH	FCI	20020110-H021A01LF	1
J3	Term Block Plug 2 Pos 5.08MM	FCI	20020006-H021B01LF	1
J4	Jumper Wire, 500mil spacing, Green, pkg of 200	3M	923345-05-C	1
L2	Inductor, Wirewound, Ferrite, 1000uH, 0.42A, 2.5 ohm, TH	Wurth Elektronik eiSos	744743102	1
Q1	MOSFET N-CH 800V 1.5A TO-220F	Fairchild Semiconductor	FQPF2N80	1
Q2	Transistor, NPN, xxV, 4A, TO-220F	NXP Semiconductors	BUJ302AX	1

R1	Thermistor NTC, 10 ohm, 20%, Disc_11.5mmx6mm	EPCOS Inc	B57236S0100M000	1
R2	RES, 100 k, 5%, 0.75 W, 2010	Vishay-Dale	CRCW2010100KJNEF	1
R3	RES, 6.8 k, 5%, 0.75 W, 2010	Vishay-Dale	CRCW20106K80JNEF	1
R4, R5	RES, 270 k, 5%, 0.25 W, 1206	Vishay-Dale	CRCW1206270KJNEA	2
R6	RES, 0, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12060000Z0EA	1
R8	RES, xxx ohm, x%, xW, [PackageReference]	Panasonic Electronic Components	ERJ-P6WF1203V	1
R9	RES, 42.2 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0742K2L	1
R10	RES, 3.09 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06033K09FKEA	1
R11, R12	RES, 2.70, 1%, 0.25 W, 1206	Yageo America	RC1206FR-072R7L	2
T1	1 Input 4 Output XFMR	Used in BOM report	Used in BOM report	1
U1	Constant-Voltage, Constant-Current Controller	Texas Instruments	UCC28722DBV	1
V2	TVS DIODE 342VWM 706VC DO15	STMicroelectronics	P6KE400CARL	1
Vbulk, Vdd	Test Point, Miniature, Yellow, TH	Keystone	5004	2

6.3 PCB Layout Recommendations

Recommend not routing CS track close to Switch node as noise from switching edge can couple onto CS pin. R10 and C17 should be placed close to the CS pin and C17 should grounded close to GND pin of IC.



7 About the Author

Billy Long is a Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the High Voltage power supply market. Billy brings to this role his extensive experience in power supply design and system development. Billy earned his Bachelor of Electrical and Electronic Engineering (BEE) from University Collage Cork, Ireland.

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