TI Designs

Automotive ADAS Reference Design for Four-Camera Hub With MIPI CSI-2 Output

TEXAS INSTRUMENTS

Description

This camera hub reference design allows connection of up to four 1.3-megapixel cameras to a TDA3x system-on-chip (SoC) evaluation module (EVM). Each camera connects to the hub through a single coax cable. Using FPD-Link III connections, the cameras are connected to a four-port deserializer. The output of the deserializer is MIPI CSI-2. The design also allows connection of other types of sensors for sensor fusion use cases.

Resources

|	
TIDA-01005	Design Folder
DS90UB964A-Q1	Product Folder
TPS55340-Q1	Product Folder
TPS62160-Q1	Product Folder
TPS7B7702-Q1	Product Folder
SN74LVC1G125-Q1	Product Folder
TS3USB221A-Q1	Product Folder
MSP430F2272-Q1	Product Folder
TIDA-00421	Design Folder

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Features

- Accepts Four Camera Inputs Over FPD-Link III
- Provides Wide-Range Supply Voltage for Power Over Coax (4 V to 14 V)
- Directly Connects to CSI-2 Video Ports on TDA3x EVM
- Car Battery Can Directly Supply Board Power
- Utilizes MSP430™ microcontroller (MCU) to Initialize and Configure Video Pipeline
- Design Compatible With Onboard MCU, Without MCU, or With External MCU
- Works With Any Camera That Uses Compatible FPD-Link III Serializer

Applications

- ADAS Vision Systems
- Surround View Systems
- Fusion Systems

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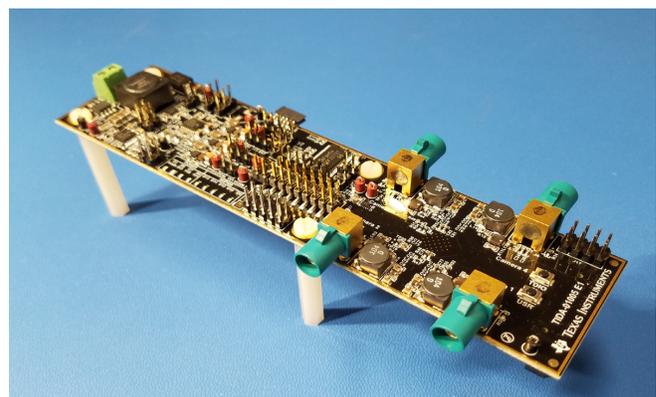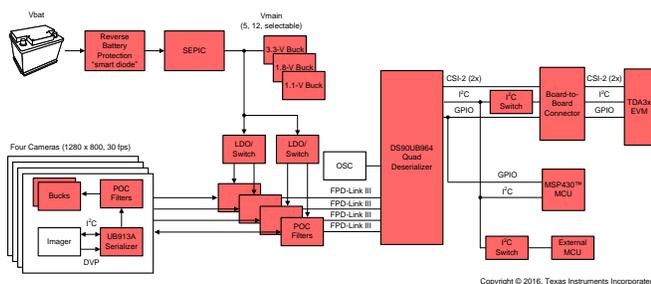
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Automotive ADAS Reference Design for Four-Camera Hub With MIPI CSI-2 Output   1

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1 System Overview

1.1 System Description

Many automotive advanced driver assistance systems (ADAS) require multiple cameras. This TIDA-01005 TI Design addresses these requirements by combining the outputs from four 1.3-megapixel imagers into two MIPI CSI-2 video ports. These video ports are available on an external connector that can attach to a TDA3x EVM or a similar SoC or processor.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Supply voltage	4 V < 12 V (typ) > 17 V	From external supply
Total power consumption without cameras	1.7 W (typ), > 2 W	At 12 V
Total power consumption with four TIDA-00421 cameras	5.5 W (typ), > 6 W	At 12 V

1.3 Block Diagram

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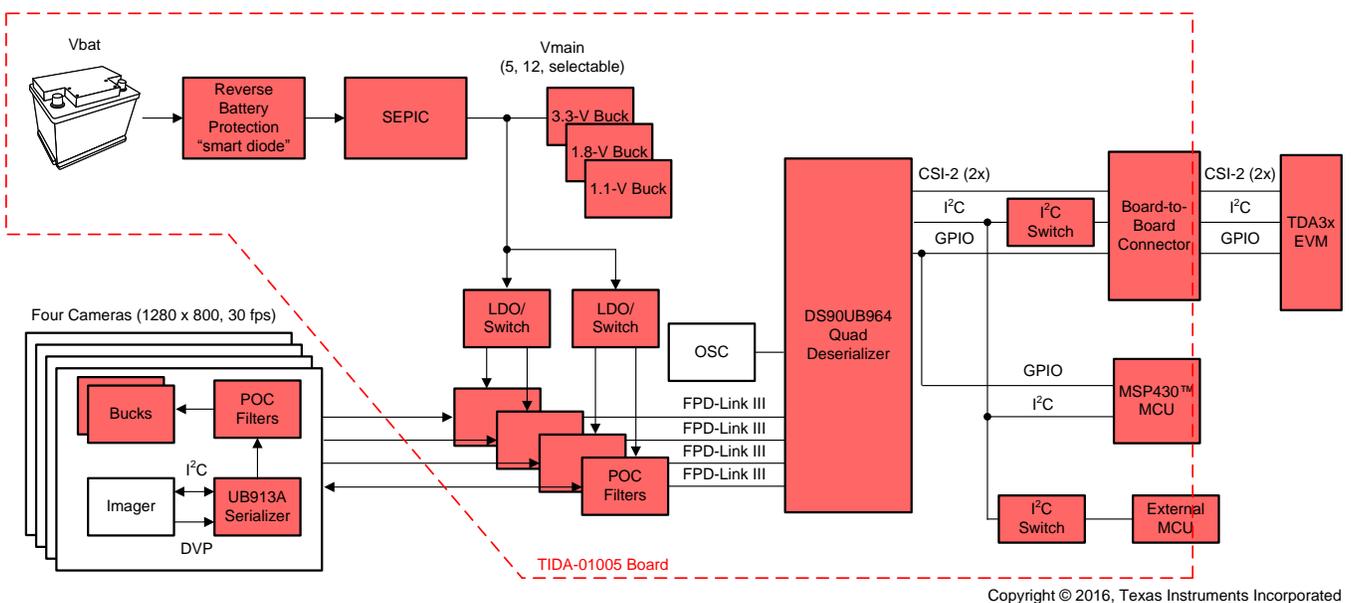
Figure 1. TIDA-01005 Block Diagram and System Partition

1.4 Highlighted Products

1.4.1 DS90UB964A-Q1

The DS90UB964A-Q1 is a four-input version of the deserializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).

1.4.2   TPS55340-Q1

The TPS55340-Q1 is a monolithic non-synchronous switching converter with an integrated 5-A, 40-V power switch. The device can be configured in several standard switching-regulator topologies including boost, single-ended primary-inductor converter (SEPIC), and isolated flyback. The device has a wide input voltage range to support applications with input voltage from 2.9 V to 38 V.

1.4.3   TPS62160-Q1

The TPS62160-Q1 is an easy to use synchronous step-down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response.

1.4.4   TPS7B7702-Q1

The TPS7B7702-Q1 is a dual-channel antenna low-dropout regulator (LDO) with current sense. This high-voltage LDO is designed to operate with a wide input voltage range from 4.5 V to 40 V. The device also has overcurrent protection and can withstand a short-to-ground or a short-to-battery on its outputs.

1.4.5   SN74LVC1G125-Q1

The SN74LVC1G125-Q1 is an automotive-qualified version of a single bus buffer gate with a three-state output.

1.4.6   TS3USB221A-Q1

The TS3USB221A-Q1 is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB input and output (I/O) connections.

1.4.7   MSP430F2272-Q1

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers (MCUs) consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally-controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 1 µs.

1.4.8   TIDA-00421

This reference design frequently makes references to the TIDA-00421 TI-Design, which is an automotive 1.3-megapixel camera module built around a DS90UB913A serializer and an OmniVision OV10640 imager. Refer to the details in the TIDA-00421 reference design *Automotive 1.3M Camera Module Reference Design With OV10640, DS90UB913A, and Power Over Coax* (TIDUB74). Other camera reference designs that can be used with this design are:

- TIDA-00262 reference design – *Optimized Automotive 1M Pixel Camera Module Design for Uncompressed Digital Video over Coax* (TIDUBQ5)
- TIDA-01002 reference design – *Automotive 1MP Camera Module Reference Design with YUV422 Output, FPD-Link III and Power over Coax* (TIDUC90)

  The following subsections provide more information on each device and why they were chosen for this application.

1.5 Design Considerations

1.5.1 DS90UB964A-Q1

Using a serializer and deserializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements.

The DS90UB964-Q1 four-channel deserializer takes this simplification one step further. Each camera in the system is connected to the deserializer through a single coax cable. Using power-over-coax (PoC) filters, the power for each camera is also included on the single coax connection. By using these filters, video, I²C control, diagnostics, and power can all be transmitted up to 15 m on a single inexpensive coax cable. For more information on the cable itself, refer to the *Cable Requirements for the DS90UB913A & DS90UB914A* application note[6] (SNLA229).

In this design, the DS90UB964-Q1 is paired with a DS90UB913A-Q1 that is on a separate camera board (TIDA-00421). The DS90UB913A-Q1 FPD-Link III 1.4-Gbit/s serializer is intended to link with megapixel image sensors. The serializer transforms a parallel LVCMOS data bus (video port) along with a bidirectional control bus (I²C port) into a single, high-speed differential pair. The DS90UB913A-Q1 can accept up to 12 bits of data plus 2 bits (for example, HSYNC and VSYNC) and the pixel clock (PCLK) in a range of 25 MHz to 100 MHz. The integrated, bidirectional control channel transfers data over the same differential pair; therefore, it eliminates the requirement for additional wires to program the registers of the image sensors. In addition, the serializer provides up to four GPO pins, which can act as outputs for the input signals that are fed into the deserializer general-purpose input/output (GPIO) pins triggering the image sensors logic. For example, the deserializer and the serializer can be configured in a way so that one GPIO pin on the deserializer side causes one GPO pin on the serializer side to toggle. In other words, the output pins of the serializer reflect the assigned input pins from the deserializer.

Alternatively, the GPO 2 pin can be configured to become a clock output pin when set in external oscillator mode (CLKOUT). In turn, the GPO 3 pin acts as the input for an external clock source (CLKIN). The GPO 3 pin allows the serializer to drive the system clock input (XVCLK) of the image sensor. Another option is to directly control the output value of the GPO on the serializer with the use of a register in the serializer. This feature allows the host MCU or SoC to change this output value through I²C. One example use of this feature is to enable the MCU to control the reset of a device on the camera module.

1.5.2 TPS55340-Q1

For this design, the supply for the cameras is required to be configurable from 5 V to 14 V. With some of this range being above and below the input battery supply, a SEPIC is a good choice to solve this problem. With a simple jumper setting, one of the two most common camera power supplies can be chosen (5 V and 12 V). To select other voltages, the user can modify the feedback resistor network.

Camera sensor circuits are usually sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications, which means that the TPS55340-Q1 switching regulator operating up to 2.5 MHz meets both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

1.5.3 TPS62160-Q1

To generate the low-voltage rails for this design, three of the TPS62160-/Q1 step-down switching power supplies are tied to the main 5-V or 12-V rail. With a maximum input voltage of 17 V, this specification provides a lot of flexibility for the designer when choosing the main rail. This flexibility allows the main rail to be chosen to directly output to cameras, directly supply a CAN PHY or optimize efficiency in the system.

Camera sensor circuits are usually sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. This specification means that the TPS55340-Q1 switching regulator operating up to 2.5 MHz meets both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

1.5.4 TPS7B7702-Q1

Limiting the current available to the cameras is a choice wise for many applications. In this design, the TPS7B7702-Q1 switch limits the current available to the four cameras. Controlling this switch from the MCU also allow the designer to decide when power is to supply each camera and provides the flexibility for the host system to cycle the power to the cameras if this is ever required during start-up, diagnostics, or in response to a detected fault.

1.5.5 SN74LVC1G125-Q1

This one bit buffer has been used in this design to allow the user to quickly determine if the power rails are present and functioning normally. Each of the buffers is connected directly to the power good output of the TLV62160-Q1 power supplies. The output is connected to a light-emitting diode (LED). This circuitry is likely to be removed from a production system.

1.5.6 TS3USB221A-Q1

This design utilizes these high-bandwidth USB switches to dynamically configure the I^2C bus on the board. These parts are much faster than what is required but they work well and are very simple to implement. For more information on the configuration of the I^2C bus, refer to the following Section 1.5.7, which addresses the MCU.

1.5.7 MSP430F2272-Q1

This version of MSP430 is used in this design as a housekeeping and configuration microcontroller, which allows the main SoC in the system to boot in parallel with the configuration of the SER/DES links and camera imagers. Refer to Section 4.1 for more information on this topic.

2 System Design Theory

2.1 *PCB and Form Factor*

This design is primarily specified for use in connection with the TDA3x EVM. The printed-circuit board (PCB) has been designed to mate to the CSI-2 connector on the outer edge of the TDA3x EVM (see Figure 2 and Figure 3). The size of the design can be reduced by removing the GPIO jumpers and power-supply selection jumpers. Furthermore, use of the MCU is unnecessary if the host processor completely handles the setup of the system configuration over I²C. LEDs are a luxury during system and software debug, but they are not required in a production design, either.
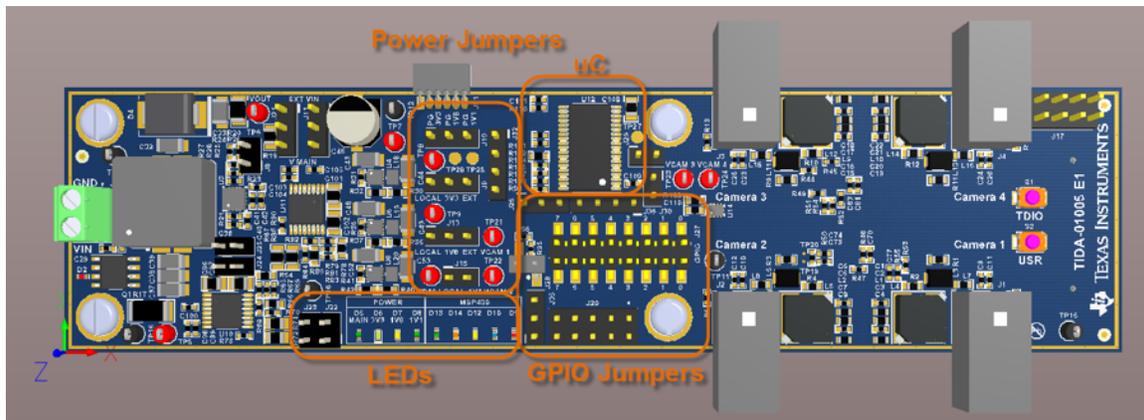
Figure 2. Board—Top View
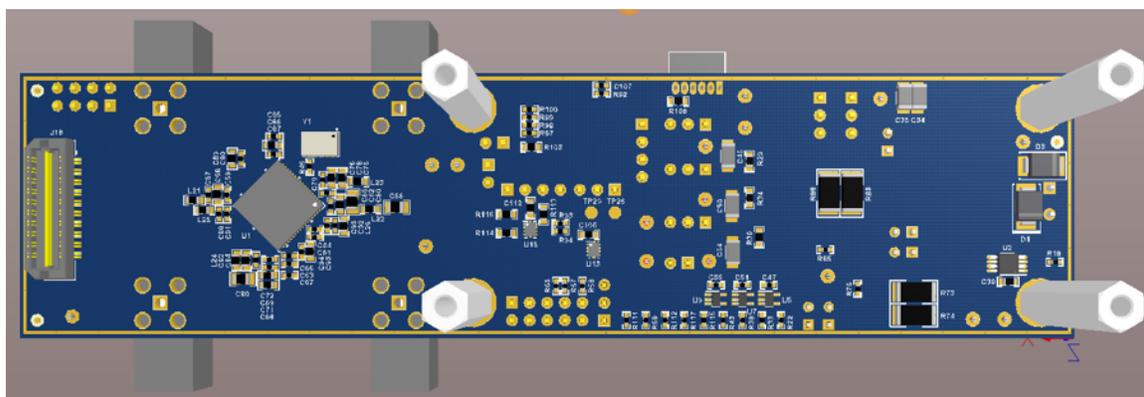
Figure 3. Board—Bottom View

2.2 *I²C Addressing*

2.2.1 Multiple Device Addressing (Aliasing)

Surround view applications require several cameras in a single system. Using multiple cameras of the same build (and therefore fixed to the same physical I²C address) is often a desirable specification. This design uses a common imager in the system, which is the OV10640. This imager default address is 0x30 (0110000x). For a system utilizing more than one imager, GPIO 2/1 can be used to select different addresses for each imager; however, this requires a different build for each camera in the system. Each system would have to be built with one of each unique camera. In a production environment, this

requirement is not desirable. One practical alternative is to use the aliasing feature of the DS90UB964, instead. In the deserializer, unique addresses are assigned to each imager. These aliases are used to refer to the imagers that are all addressed at 0x30 (0110000x). The host microprocessor can now communicate with each imager by using its alias, even though the imagers in each camera are physically addressed identically.

If these cameras are all to be accessed on the same I^{2}C bus, there must be a method of assigning each camera an alias for use when addressing them. The FPD-Link SER/DES parts provide this functionality to assign a slave ID (alias) to each camera. This feature allows the slave devices to be independently addressed. The physical address of the slave and its associated alias IDs are configured by programming the "Slave ID" and "Slave Alias" registers on the deserializer. From the I^{2}C host perspective, this task remaps the address of each slave to its slave alias.

For this design, a common imager used in the system is the OV10640. The default address of this imager is 0x30 (0110000x). For a system utilizing more than one imager, GPIO 2/1 can be used to select different addresses for each imager; however, this requires a different build for each camera in the system. Each system would have to be built with one of each unique camera, which is undesirable in a production environment.

An alternative is to use the aliasing feature of the DS90UB964 device. In the deserializer, unique addresses are assigned to each imager. These aliases are used to refer to the imagers that are all addressed at 0x30 (0110000x). The host microprocessor can then communicate with each imager by using its alias, even though the imagers in each camera are physically addressed identically. Figure 4 shows an example of I^{2}C address aliasing.


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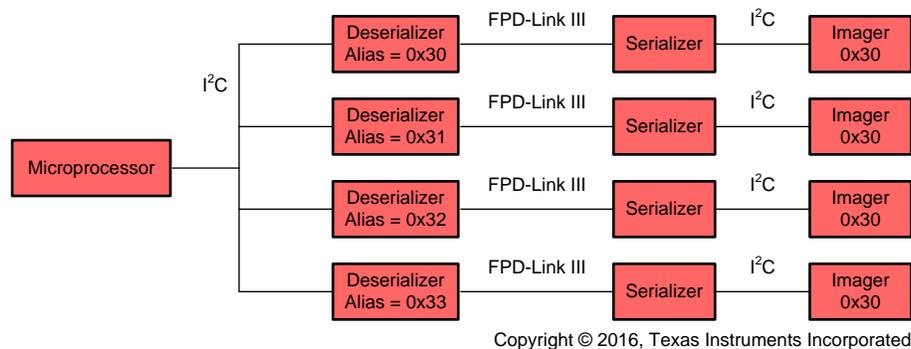
Figure 4. I^{2}C Address Aliasing

2.2.2 I^{2}C Bus Switches and Connections

This system offers six possible I^{2}C hosts. Each host has a role to perform and a slave that they must configure. This requirement complicates the I^{2}C bus connections. Figure 5 shows three I^{2}C switches which are used to configure the I^{2}C bus to accomplish all of the tasks required for initialization of the system. A GPIO has been stationed on the MCU connected to the control pin of each switch. These control pins are labeled with red text under the switch in Figure 5. Their functionality can be described as:

- I^{2}C_SW_EXT: When this switch is open, either the MSP430 or the SoC functions as the I^{2}C host in the system. When this switch closes, it allows the external MCU to take over as host of the I^{2}C bus. If an external MCU is used, place the MSP430 into external MCU mode by setting the jumper J19.
- I^{2}C_SW_SOC: When this switch is open, all SoC I^{2}C traffic is isolated from the TIDA-01005 board. This isolation allows either the local MCU or the external MCU to act as the host. Depending on when this switch is closed, the SoC can either initialize the board or just control the camera after one of the MCUs has initialized the board. Control of the cameras is done by writing I^{2}C commands into the UB96x during normal operation.
- I^{2}C_SW_DES: When this switch is closed, the main I^{2}C bus on the UB96x is connected to the main I^{2}C bus on the board.
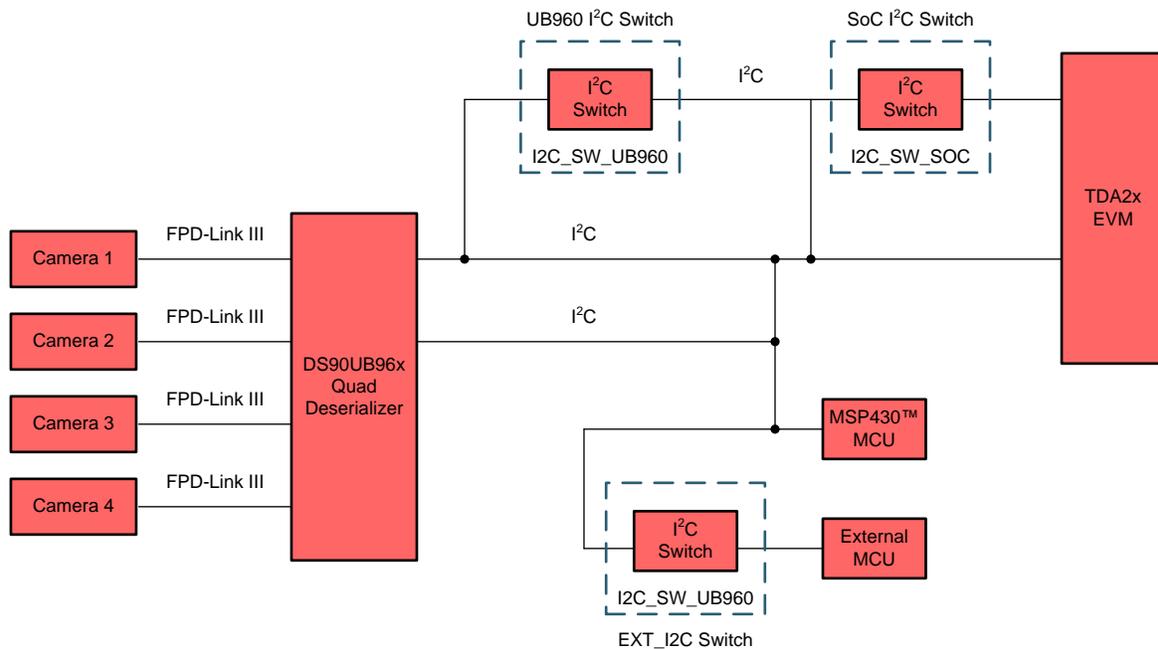
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Figure 5. I²C Bus Diagram

2.2.3   Power-Over-Coax (PoC) Filter

One of the most critical portions of a design that uses PoC is the filter circuitry (see Figure 6). The goal is twofold: deliver a clean DC supply to the input of the switching regulators and protect the FPDLink communication channels from noise coupled backwards from the rest of the system.

The DS90UB964-Q1 and DS90UB913/914 SER/DES devices used in this system communicate over two carrier frequencies: 700 MHz at full speed ("forward channel") and a lower frequency between 1.75 MHz and 3.25 MHz ("back channel") as determined by the deserializer device. The filter should attenuate this rather large band spanning both carriers, hoping to pass only DC. Luckily, the process of filtering the back channel frequency also filters the frequencies from the switching power supplies on the board.

An ideal series 100-µH inductor can work as a low-pass filter, with impedance > 1 KΩ at frequencies starting at 1 MHz; however, because of parasitic capacitances, a real 100-µH inductor would cease to have high impedance around 70 MHz. Another series inductor is necessary to cover the higher-frequency band. A 10-µH inductor ensures that the design has high impedance up to frequencies well above the 700-MHz forward channel. Refer to the *Sending Power Over Coax in DS90UB913A Designs* application note[5] for more details (SNLA224).
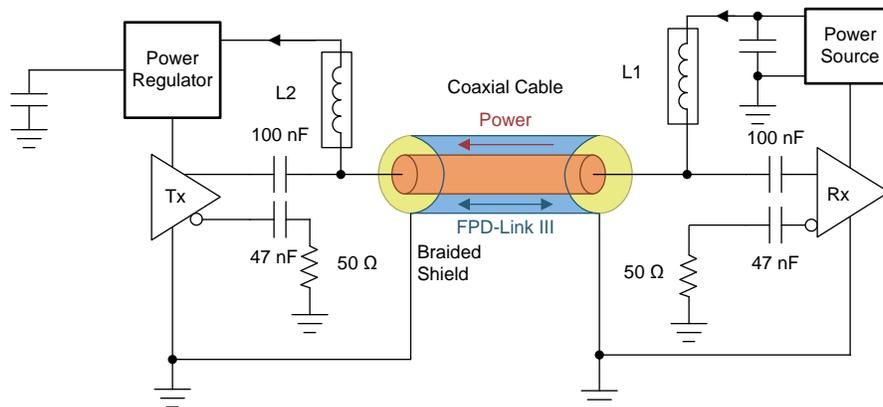
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Figure 6. Power-Over-Coax

2.3 Step-Down Converter

Figure 7 shows the typical application circuit of the step-down converter. Much of the component selection and design theory can be found in the *Application Information* section of the TPS62160 datasheet *TPS6216x 3-V to 17-V, 1-A Step-Down Converters with DCS-Control ™* (SLVSAM2). Only a few external components are available from which to choose during component selection of the step-down converter.
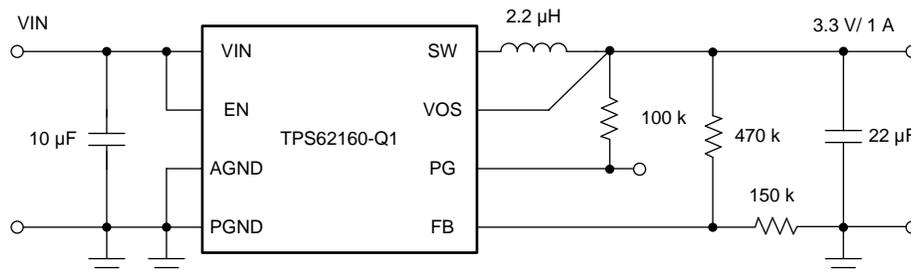
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Figure 7. Typical Application Circuit

2.3.1 Choosing Output Inductance Value

As previously mentioned, maintaining the switching frequency of the converter above 2 MHz is important in this design, which means that the converter must always operate in continuous mode. Because input voltage and output voltage are fixed and the output current is almost constant and easy to predict, the minimum inductance, L, for the converter to operate with continuous inductor current can be calculated using the following Equation 1:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2 \times V_{IN}\, I_{OUT} \times f} = \frac{3.3\,V\left(12\,V - 3.3\,V\right)}{2 \times 12\,V \times 0.250\,A \times 2.1\,MHz} = 2.27\,\mu H$$

(1)

There is a safety margin in the 250-mA current budget. So, a 2.2-uH works well for this application.

After choosing the inductance, the next step is to select an inductor with a proper saturation current. The maximum current through the inductor is going to be the combination of the steady state supply current, as well as the inductor ripple current. The goal is to obtain a sufficiently high current rating that can be minimized as much as possible to reduce the physical size of the inductor. The following Equation 2 is used to calculate the inductor ripple current (from the datasheet):

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$$\Delta I_L = V_{OUT} \times \left(\frac{\left(1 - \dfrac{V_{OUT}}{V_{IN}}\right)}{L \times f_{sw}} \right)$$

(2)

Equation 3 shows the parameters for this design using the TPS62160-Q1:

$$V_{OUT} = 3.3\,V,\ V_{IN} = 12\,V,\ L = 2.2\,\mu H,\ f_{sw} = 2.25\,MHz$$

(3)

Equation 3 yields an inductor ripple current of ΔI_L = 483 mA. The maximum current draw of the system through this regulator is 250 mA. Finally, the following Equation 4 is used to calculate the minimum saturation:

$$L_{sat} \geq \left(I_{max} + \frac{I_{ripple}}{2} \right) \times 1.2 = \left(250\,mA + \frac{483\,mA}{2} \right) \times 1.2 = 589\,mA$$

(4)

A TDK VLS201610HBX-2R2M has been selected for this design, which has a saturation current of 1700 mA with only a 10% drop in inductance. This part comes in a 2×1.6-mm package.

2.3.2 Choosing the Output Capacitor

Because the device is internally compensated, it is only stable for certain component values in the LC output filter. The *Optimizing the TPS62130/40/50/60/70 Output Filter* application note[7] (SLVA463) provides the chart of stable values (see Table 2). The selected 2.2-uH inductor paired with a 22-uF capacitor yields a 32.4-kHz corner frequency, which is well within the recommended stable range for the TPS6216x family.

Table 2. Stability Versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	EFFECTIVE CORNER FREQUENCIES								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
0.47 µH	151.4 kHz	103.8 kHz	70.0 kHz	47.9 kHz	32.8 kHz	23.2 kHz	16.4 kHz	11.6 kHz	8.2 kHz
1.00 µH	103.8 kHz	71.2 kHz	48.0 kHz	32.8 kHz	22.5 kHz	15.9 kHz	11.3 kHz	8.0 kHz	5.6 kHz
2.2 µH	70.0 kHz	48.0 kHz	32.4 kHz	22.1 kHz	15.2 kHz	10.7 kHz	7.6 kHz	5.4 kHz	3.8 kHz
3.3 µH	57.2 kHz	39.2 kHz	26.4 kHz	18.1 kHz	12.4 kHz	8.8 kHz	6.2 kHz	4.4 kHz	3.1 kHz
4.7 µH	47.9 kHz	32.8 kHz	22.1 kHz	15.1 kHz	10.4 kHz	7.3 kHz	5.2 kHz	3.7 kHz	2.6 kHz
10.0 µH	32.8 kHz	22.5 kHz	15.2 kHz	10.4 kHz	7.1 kHz	5.0 kHz	3.6 kHz	2.5 kHz	1.8 kHz
	Recommended for TPS6213x/4x/5x/6x/7x								
	Recommended for TPS6213x/4x/5x only								
	Stable without Cff (within recommended LC corner frequency range)								
	Stable without Cff (outside recommended LC corner frequency range)								
	Unstable								

2.3.3 Choosing Feedback Resistors

The output voltage is determined by the resistor divider to the feedback pin. The following Equation 5 shows the calculation for the output voltage. The goal is to achieve a 3.3-V out while at the same time working with readily-available resistor values.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{ref}} - 1 \right) \rightarrow V_{OUT} = \left(\frac{R1}{R2} + 1 \right) \times V_{ref} = \left(\frac{316\,k\Omega}{100\,k\Omega} + 1 \right) \times 0.8\,V = 3.328\,V$$

(5)

This result provides a close enough output voltage to the desired 3.3 V. For improved accuracy, all feedback resistor dividers should use components with 1% or better tolerance.

3 Getting Started Hardware

3.1 Hardware Configuration

The TIDA-01005 requires configuration before use. Perform the following configuration steps in order to avoid damage to system components. The following configuration is for a four-camera surround view system using TIDA-00421 cameras and a TDA3x EVM. The included power supply powers the EVM while a supply similar to a car battery is used to power the TIDA-01005.

1. Configure the power supply. Add and verify jumpers in the following locations (see Figure 8):

    (a) J21 pins 2 to 3 – Connects output of SEPIC to the high-side switch for cameras

    (b) J11 pins 2 to 3 – Connects output of SEPIC to input of buck converters

    (c) Do not install J8 – Sets SEPIC output to 14 V

    (d) J9 pins 1 to 2 – Selects output from 3.3-V buck instead of external supply

    (e) J13 pins 1 to 2 – Selects output from 1.8-V buck instead of external supply

    (f) J15 pins 1 to 2 – Selects output from 1.1-V buck

2. Set the MCU mode by setting J26. Pins 1 and 2 place the board in local MCU mode and is initialized by the MSP430.

3. Connect TIDA-01005 to the TDA3x EVM.

4. Connect four TIDA-00421 cameras using FAKRA coax cables.

5. Connect HDMI OUT on the TDA3x EVM to monitor using an HDMI cable.

6. Connect the power supply provided with the TDA3x EVM to the input power connector on the EVM.

7. Connect 12 V of input power to J5. Pin 1 is marked VIN. Pin 2 is marked GND. The board is protected against reversing the input voltage. If the polarity of the input voltage is reversed, LED D2 illuminates and Q1 prevents damage to the board.

8. Press the MSP430 RESET button (S1) on the TIDA-01005 board.
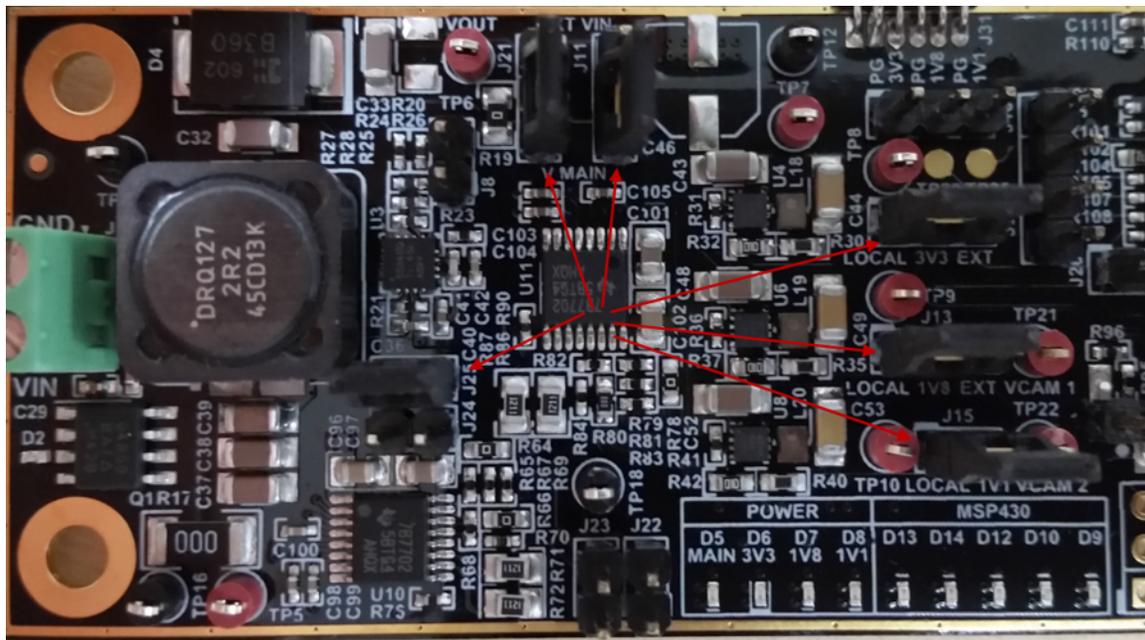
Figure 8. Power Supply Jumpers

3.2 Software

GPIO configuration:

Headers are situated on eight of the GPIOs for the MCU and deserializer (see Figure 9), which allows for maximum flexibility when utilizing these GPIOs as required in each application. This setup also indicates that the jumpers must be correctly set for any configuration. In the case of this design, the use any of the MCU GPIOs is not required, so none of the jumpers are installed.
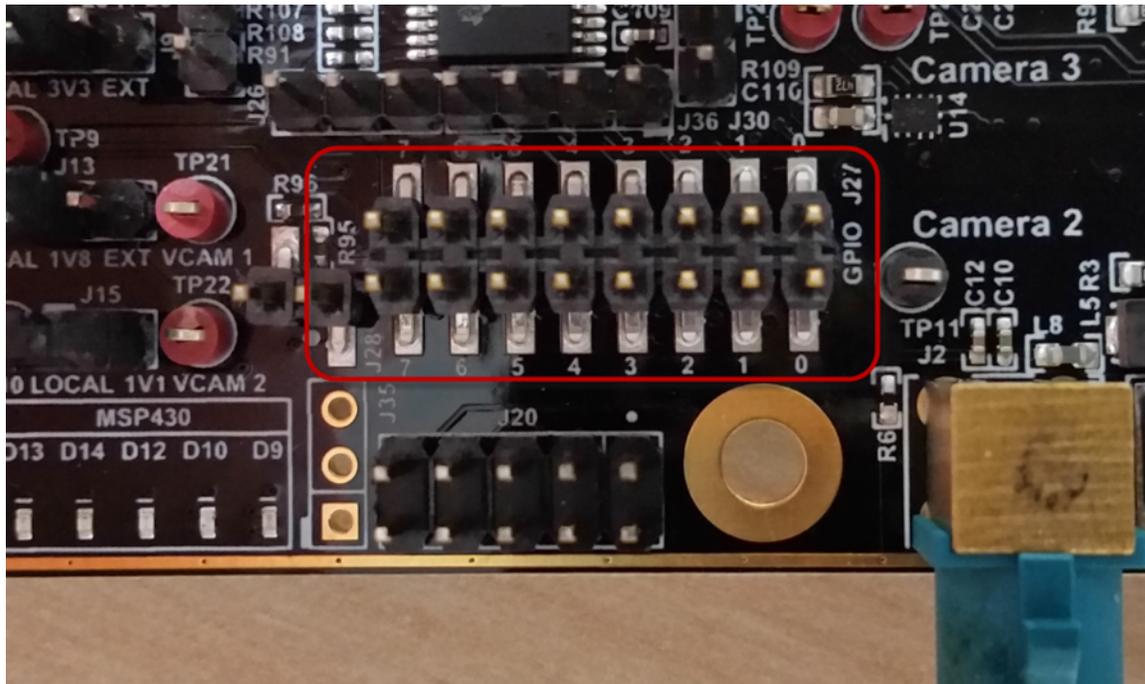
Figure 9. GPIO Jumpers

4   Getting Started Firmware

4.1   Board Boot Sequence

If the board has been placed into local MCU mode (J26), the MSP430 MCU is in control of the start-up sequence of the board. At start-up, pulldown resistors hold the UB964 in RESET mode. When the MCU initializes, it begins the start-up of the rest of the board. The configuration sequence is as follows:

1. MCU (MSP430) boots
2. MCU opens external I^2C switch using: I2C_SW_EXT
3. MCU opens SoC I^2C switch using: I2C_SW_SOC
4. MCU closes UB964 I^2C switch using: I2C_SW_DES
5. MCU releases reset (PDB) pin on UB964 deserializer
6. The deserializer is configured by the MCU over I^2C
7. The serializer is configured for address aliasing by the MCU over I2C through the FPD-Link
8. MCU opens UB964 I^2C switch using: I2C_SW_DES
9. MCU closes external I^2C switch using: I2C_SW_EXT (to allow SoC to have control)
10. MCU changes I^2C pins to inputs (high Z) and loops infinitely

The board is now configured, the imagers are running, and the SoC has control of the imagers across the FPD-Link.

5   Test Setup

For the following tests, the TIDA-01005 board is connected to four TIDA-00421 cameras and a TDA3x EVM to create a surround view system as Figure 10 shows.
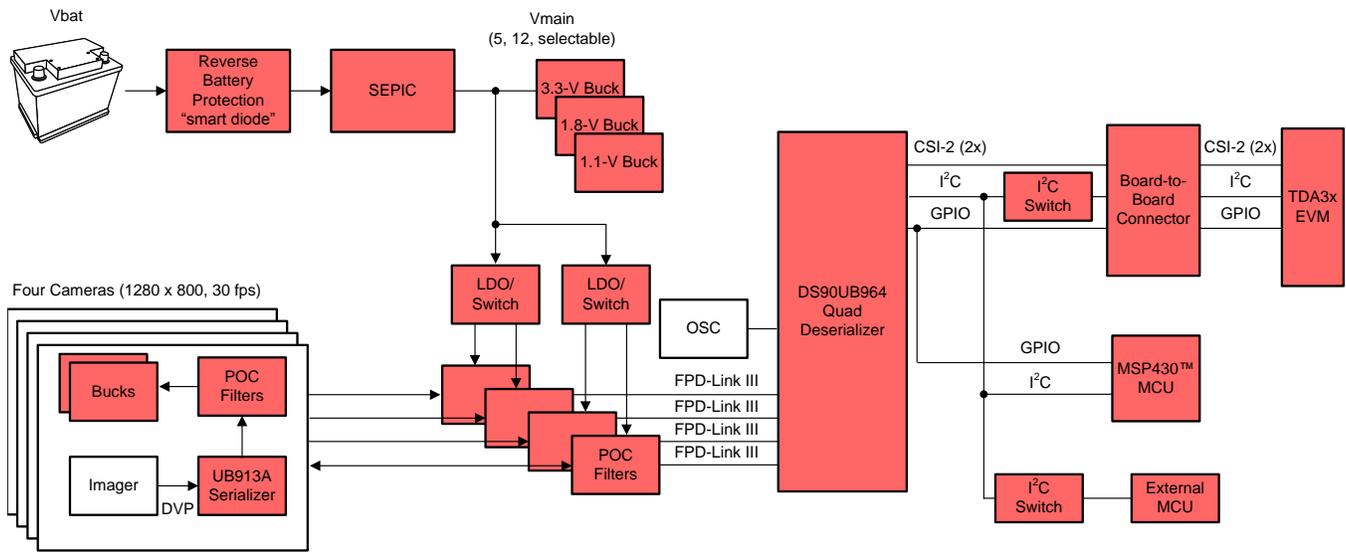
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Figure 10. Simplified Surround-View Block Diagram

5.1 Setup for Verifying Power Supply Start-Up: V$_{IN}$, 3.3-V, 1.8-V, and 1.5-V Rails

Figure 11 shows the setup for measuring the V$_{IN}$, 3.3-V, 1.8-V, and 1.5-V rails.
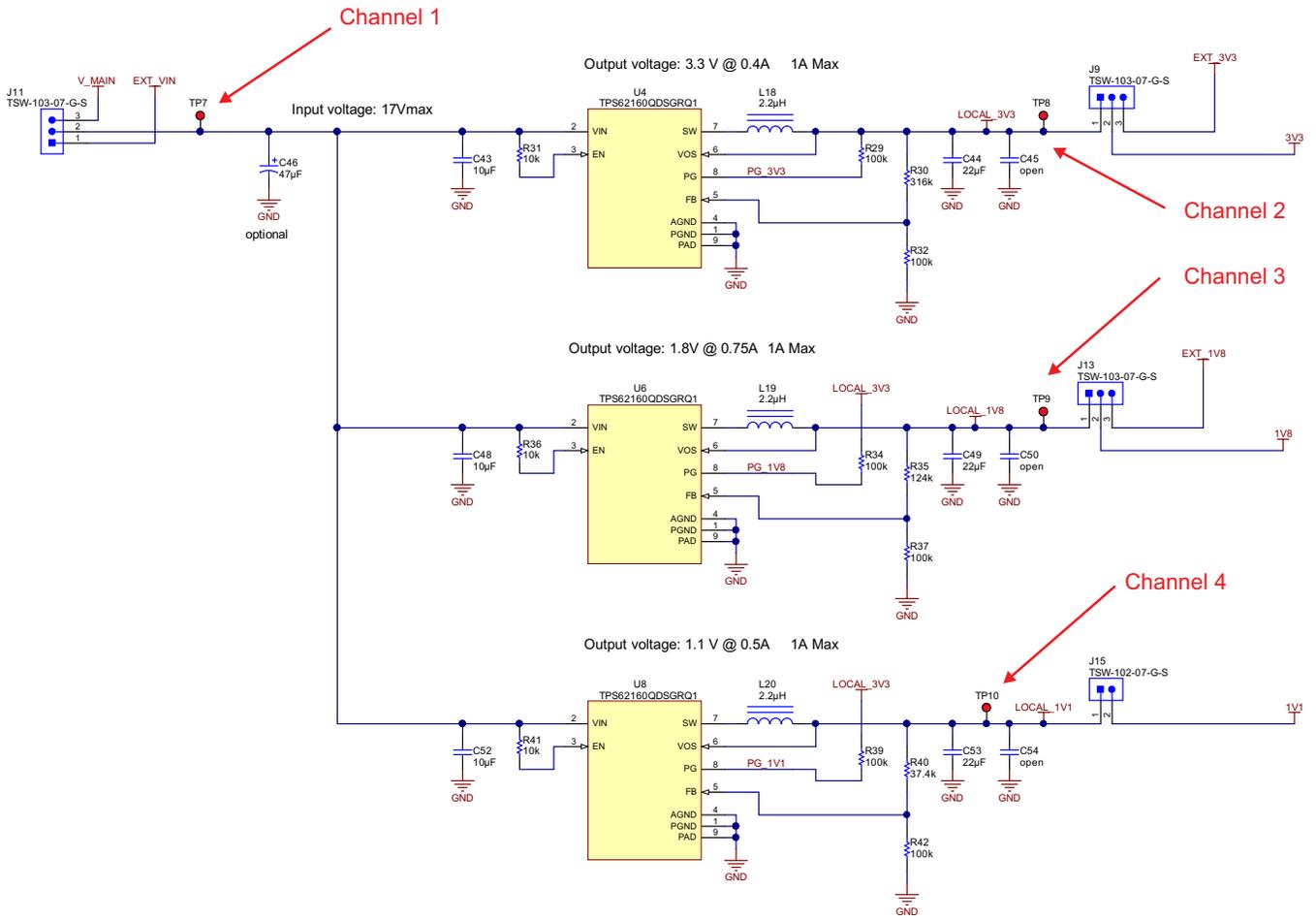
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Figure 11. Setup for Measuring All Power Rails

5.2 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses (see Figure 12). The two busses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)

2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

Connections must be made to both the clock and data lines of each bus.
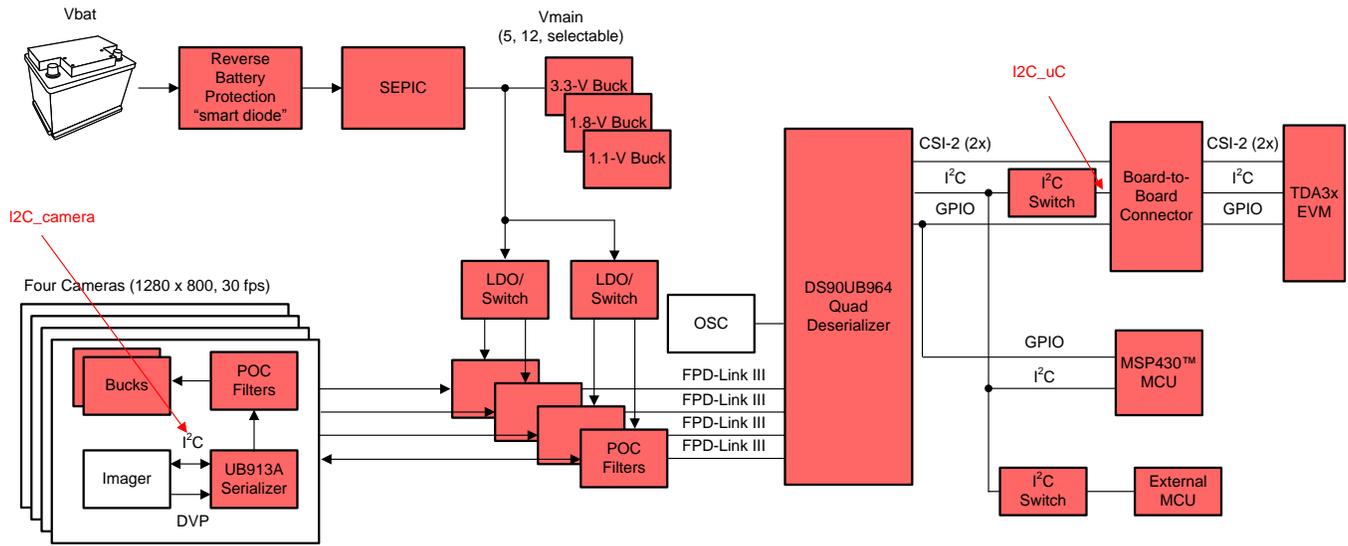
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Figure 12. Setup for Monitoring I²C Transactions

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6   Test Data

The following subsections show the test data from verifying the functionality of the camera design.

6.1   *Power Supply Start-Up: V$_{IN}$, 3.3-V, 1.8-V, and 1.5-V Rails*

The waveforms for the power supply start-up are as follows (see Figure 13):
- Channel 1 (blue): 14-V regulated power out from SEPIC supply (TP7)
- Channel 2 (red): 3.3-V switching converter output (TP8)
- Channel 3 (green): 1.8-V switching converter output (TP9)
- Channel 4 (pink): 1.1-V switching converter output (TP10)

All channels are displayed at 1 V per division. The time scale is 100 µS per division.
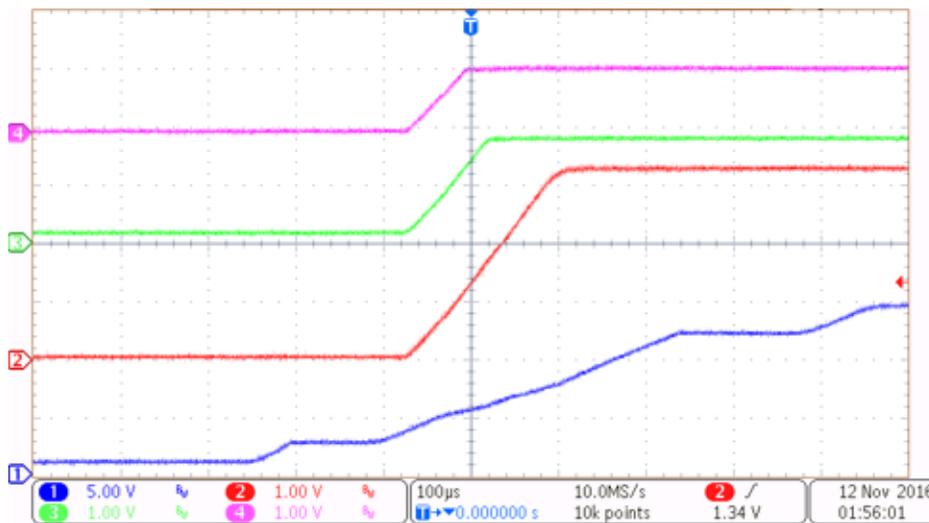
Figure 13. Power Supply Start-Up

6.2   *I²C Communications*

With the supplies up and running, the designer can then check the FPD-Link connection, the I²C aliasing, and the state of the camera or imager in one step. The following Figure 14 shows the initial communication between the microprocessor and the imager. This communication occurs after the microprocessor configures the deserializer, serializer, ISP, and imager on the other end of the link. Because this communication comes from the MCU on the TIDA-01005 board and is acknowledged by the camera (imager) on the TIDA-00421 board, this shows that the communication through the FPD-Link III is working (see Figure 14).
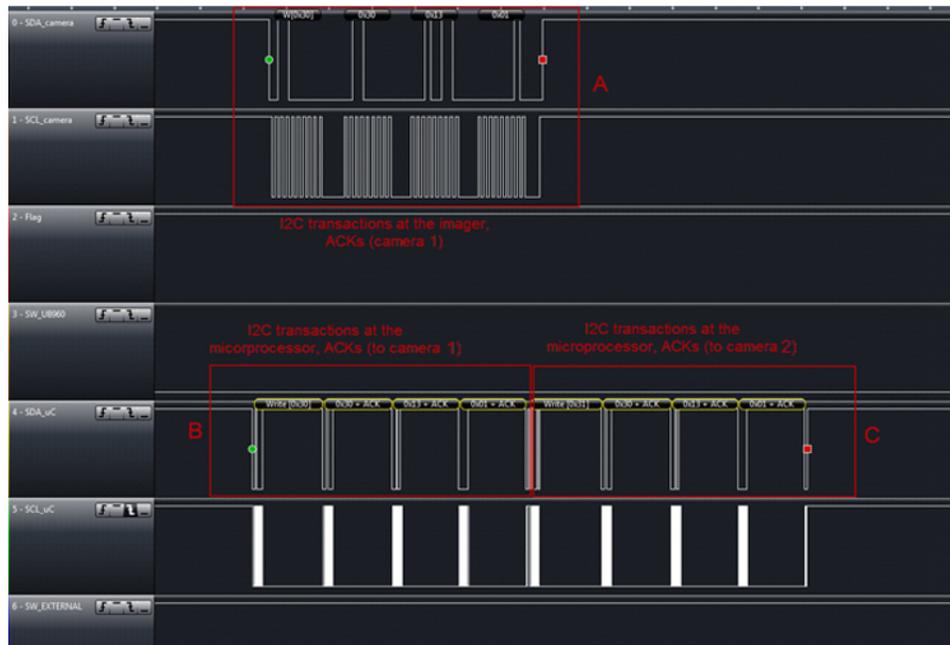
Figure 14. I²C Transactions

In Figure 14, the box labeled B contains the first write from the microprocessor. The first write is addressed to address 0x30, the register address is 0x3013, and the data to be written is 0x1. Because the address is 0x30, the logic on the deserializer passes this transaction to the first camera in the system. The write is routed to the imager and the address is aliased to 0x30.

In box A, the same communication is visible but slightly delayed. This is the communication present on the camera 1 I²C bus, measured at the imager.

The write to address 0x31 in box C is for camera 2 (see Figure 15). The deserializer passes this transaction to camera 2 and the address is aliased to 0x30. As is visible from the flow diagram in Figure 15, this transaction is not present on the camera 1 I²C bus because it is not intended for this camera.

By acknowledging the I²C write (ACK in box B), the imager on camera 1 has confirmed that it is present and alive. Similarly, the ACK in box C shows that the imager in camera 2 is responding. Reading the status registers can confirm the status of the imager as well as verify that the correct imager has been installed during assembly.

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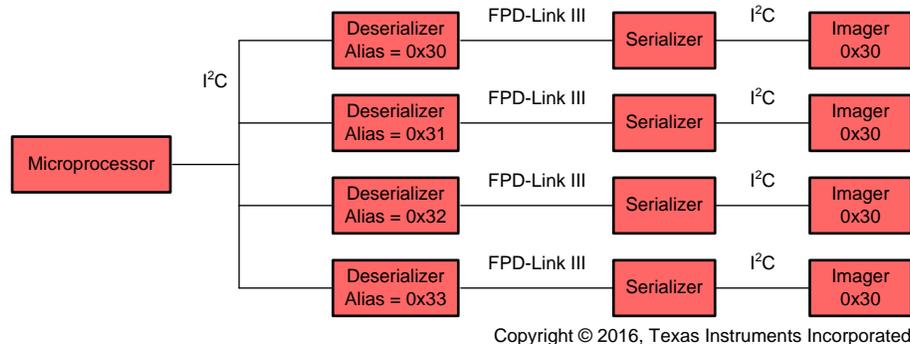
Figure 15. I²C Address Aliasing

6.3 Surround View Video

As Figure 16 shows, the cameras have been mounted to a toy jeep. The video showing the four separate images as well as a combined view from the "top" displays on the liquid-crystal display (LCD) screen.

Figure 16. Surround View Video

7   Board Programming or Reprogramming

If the board has not been programmed or the software requires an update, use the following procedure. MSP430 code:

1. Connect EZ430 development tool to J23
2. Connect USB cable to PC and to EZ430 development tool
3. Open the TI Code Composer Studio™ software
4. Open project files for software to be loaded
5. Select "Debug" to load the software into MSP430
6. Press "Run" to run in a debug environment or remove EZ430
7. Press the MSP430 RESET button (S1) on the TIDA-01005 board
8. The software should then be running on the board

To use the TDA3x software, refer to the TDA3x EVM documentation[8] for details.

8   Design Files

8.1   Schematics

To download the schematics, see the design files at TIDA-01005.

8.2   Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01005.

8.3   PCB Layout Recommendations

8.3.1   PCB Layer Stackup Recommendations

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines.
- If using a four-layer board, layer 2 should be a ground plane. Because most of the components and switching currents are on the top layer, this configuration reduces the inductive effect of the vias when currents are returned through the plane.

An additional two layers have been used in this board to simplify BGA fanout and routing. Figure 17 shows the six-layer stackup used in this board.
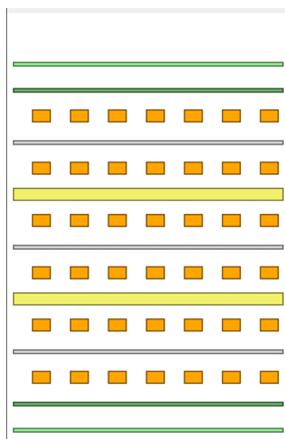
Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Layer 1 - Top Lay...	Signal	Copper	1.4				Top
Dielectric 1	Dielectric	Prepreg	5.91	370HR	4.2		
Layer 2 - GND	Signal	Copper	1.417				Not Allowed
Dielectric 2	Dielectric	Core	10	370HR	4.2		
Layer 3 - PWR	Signal	Copper	1.417				Not Allowed
Dielectric 3	Dielectric	Prepreg	20	370HR	4.2		
Layer 4 - Signal	Signal	Copper	1.417				Not Allowed
Dielectric 4	Dielectric	Core	10	370HR	4.2		
Layer 5 - GND	Signal	Copper	1.417				Not Allowed
Dielectric 5	Dielectric	Prepreg	5.91	370HR	4.2		
Layer 6 - Bottom...	Signal	Copper	1.4				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 17. Layer Stackup

8.3.2   Switching DC-DC Converter

During part placement and routing, it is helpful to always consider the path the current takes through the circuit. The yellow line in Figure 18 shows the input current path travels from the input capacitor (C43), through the switch in the converter (U4) to the inductor (L18), and then out across the output capacitors (C44 and C45). Any return currents from the input capacitor (C43) or the output capacitors (C44 and C45) are joined together on the top side of the board before they are connected to the ground (return) plane (inside the green circle). This occurrence reduces the amount of return currents in the internal ground plane, thereby allowing voltage gradients to be seen by other circuits on the board. This occurrence may not be noticeable in the performance of the converter, but it does reduce its coupled noise into other devices. Figure 18 shows the layout of the switch-mode power supply with the routing outlined and solid.
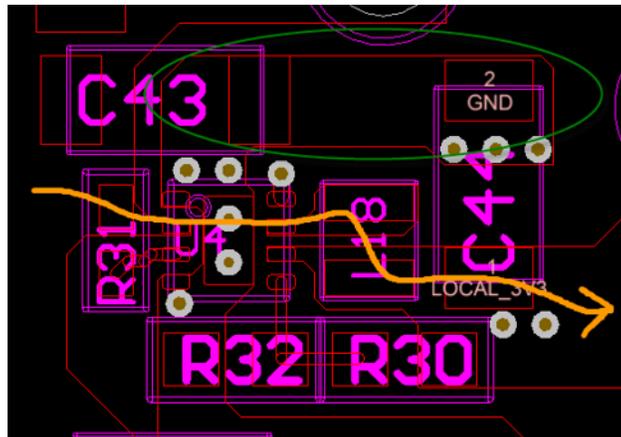
Figure 18. Step-Down Switched-Mode Power Supply Routing

Input capacitors must be placed as close to the integrated circuit (IC) as possible to reduce the parasitic series inductance from the capacitor to the device that it supplies. This placement is especially important for DC-DC converters because the inductance from the capacitor to the high-side switching field-effect transistor (FET) can cause high voltage spikes and ringing on the switch node, which can be damaging to components and cause problems such as electromagnetic interference (EMI).

8.3.3   Deserializer Layout Recommendations

Decoupling capacitors must be located very close to the supply pin on the serializer. Again, this placement requires the designer to consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. An ideal placement is not always possible due to space constraints. Smaller value capacitors that provide higher-frequency decoupling should be placed closest to the device.

Figure 19 shows the supply current from C85, C86, and C87 in yellow. The green line is the return path. The cross sectional area of this loop is very small.
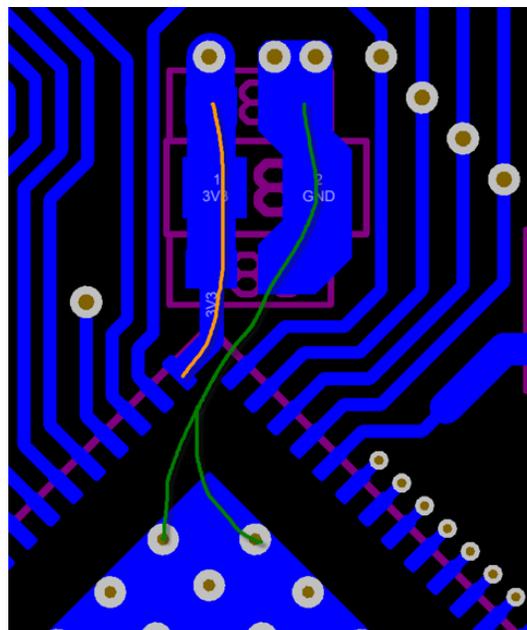
Figure 19. Decoupling Current Loop

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When routing the coaxial input to the PoC filter, be careful to reduce stubs on the low-voltage differential signaling (LVDS) nets. In Figure 20, the high-speed signal comes in from J2 and passes through C10 to U1. The DC current path is through L8 to L5. For the high-speed signal, this path to L8 and L5 is a stub. Minimizing the length of this stub reduces reflections on the LVDS lines and leads to better signal integrity.
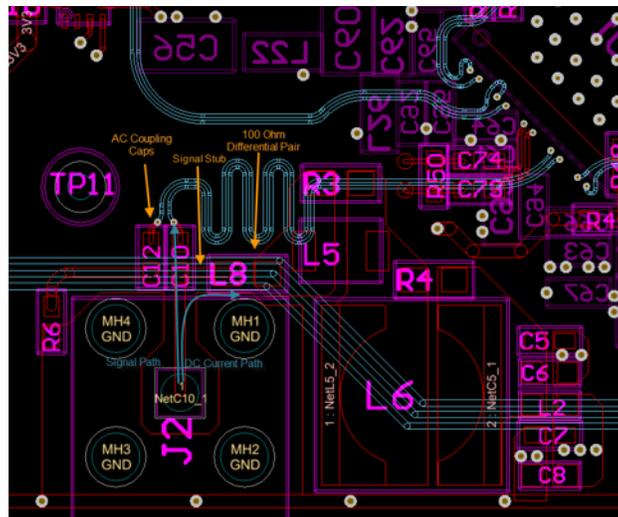
Figure 20. LVDS Signal Pair Routing

8.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-01005.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-01005.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01005.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01005.

9 Software Files

To download the software files, see the design files at TIDA-01005.

10   Related Documentation

1. Texas Instruments, *DS90UB913A-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Serialize*, DS90UB913A-Q1 Datasheet (SNLS443)
2. Texas Instruments, *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™*, TPS6217x-Q1 Datasheet (SLVSCK7)
3. Texas Instruments, *TLV702-Q1 300-mA, Low-I Q , Low-Dropout Regulator*, TLV70215-Q1 and TLV70218-Q1 Datasheet (SLVSC35)
4. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs*, Application Note (SNLA224)
5. Texas Instruments, *Cable Requirements for the DS90UB913A & DS90UB914A*, Application Note (SNLA229)
6. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 Output Filter*, Application Note (SLVA463)
7. Texas Instruments, *TDA3 – SoC Processor for Advanced Driver Assist Systems (ADAS)*, TDA3x Technical Documents

10.1   Trademarks

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11   About the Author

BRIAN SHAFFER is a systems engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, Brian focuses on ADAS (Advanced Driver Assistance Systems) end-equipments, creating reference designs for top automotive OEM and Tier 1 manufacturers. He brings to this role, his experience in high reliability infrared cameras, power supplies for portable devices, cameras for automotive platforms, and embedded systems design. Brian earned his bachelor of science in electrical engineering from Kansas State University in Manhattan, KS.

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