TI Designs: TIDA-050002

55-W Dual Buck-Boost LED Driver Reference Design for Automotive High and Low Beam Headlight

Description

This reference design describes a TPS92692-Q1 LED driver in a dual, high-beam and low-beam application with a single controller and power stage. The design operates in boost mode to provide the high beam and in boost to battery mode to provide the low beam. The single controller power stage design results in a simpler and more cost-effective lighting system. Additional design flexibility of the TPS92692 device includes analog and PWM dimming support as well as built-in monitoring for fault detection and protection of the continuous LED current. EMI filtering is included and designed to meet CISPR-25, Class 5 conduction requirements.

Resources

TIDA-050002	Design Folder
TPS92692-Q1	Product Folder
TPS92692 Boost and Boost-to-Battery EVM	Tool Folder

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Features

- Dual mode:
  - Boost mode for high beam and low beam
  - Boost to battery for low beam
- CISPR-25 Class 3 and Class 5 EMI Solutions
- Switching frequency outside of AM band
- Spread spectrum frequency modulation
- Operation through warm crank and load dump
- Continuous LED current monitoring output
- Overvoltage protection and input undervoltage lockout

Applications

- Automotive Lighting:
  - Headlights
- Industrial Cameras

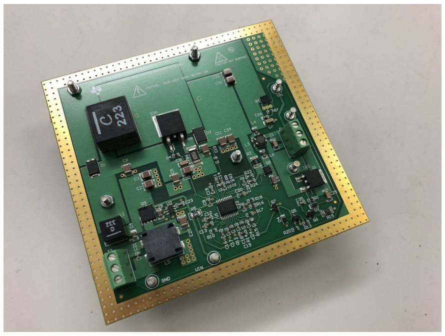
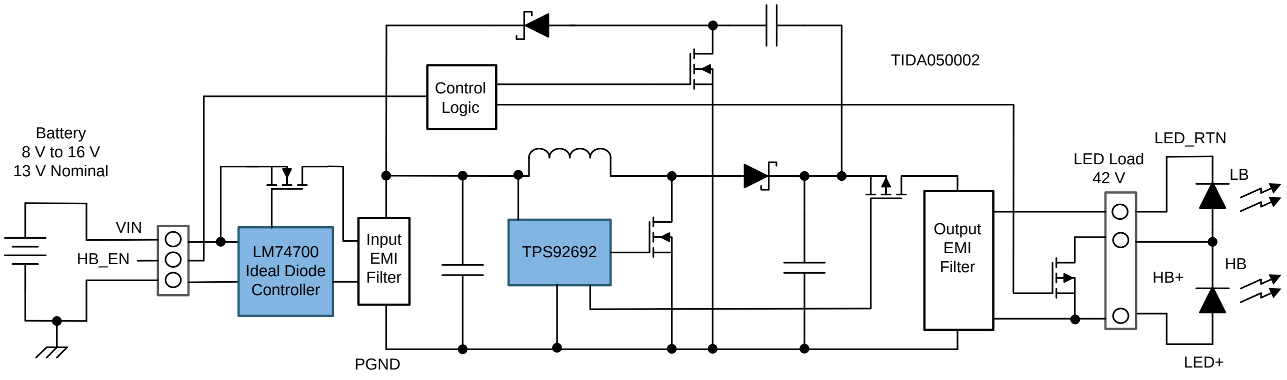


Figure 1. TIDA-050002 Board Image



1 System Description

This reference design describes a high-power (55-W) LED driver for automotive front light application. The design uses a single controller and power stage solution for driving both the high beam and the low beam. Traditional implementation uses two separate controllers and power stages. This new approach minimizes cost and circuitry while providing high-quality lighting solutions in terms of electromagnetic interference, thermal efficiency and light quality.

The design gives a simple, eas- to-adopt implementation for a high-power and output accuracy LED driver with integrated current monitoring. This design uses the TPS92692 multi-topology controller and has an input voltage range from 8 V to 16 V. This design meets CISPR-25 Class 5 EMI standards with shielding, and the switching frequency of the controller operates outside the AM frequency band. The TPS92692 controller offers external frequency synchronization, spread spectrum frequency modulation as well as analog dimmer and PWM dimming features that can be used along with this reference design for a variety of other automotive lighting applications.

The LED current is set nominally to 1.25 A with the switching frequency set at 275 kHz.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN} input voltage (nominal)		8	13	16	V
V_{IN} input voltage (min or max)	Warm crank or load dump	6		42	V
V_{IN} undervoltage lockout			4.4		V
OUTPUT CHARACTERISTICS					
LED forward voltage			3.2		V
Number of LED in series		8		14	
V_{LED} output voltage	LED+ to LED– (3-V for low beam mode)	3		44	V
I_{LED} output current	seven LEDs for high beam and seven LEDs for low beam, I_{OUT} = 1.25 A	1.18	1.25	1.31	A
Output power				55	W
PWM dimming range					
SYSTEM CHARACTERISTICS					
Output overvoltage protection level			62		V
Overvoltage hysteresis			3		V
f_{SW} switching frequency			275		kHz
Efficiency	V_{IN} = 13 V, seven LEDs for high beam and seven LEDs for low beam, I_{OUT} = 1.25 A		91%		
	V_{IN} = 13 V, seven LEDs for low beam, I_{OUT} = 1.25 A		86%		
EMI (conducted)		CISPR-25 Class 3 without shield and Class 5 with shield			
BASE BOARD CHARACTERISTICS					
Form factor		4.0" L × 3.8" W			
Number of layers		4			
Height	Including heat sink and shield	1.7"			

2 System Overview

2.1 Block Diagram

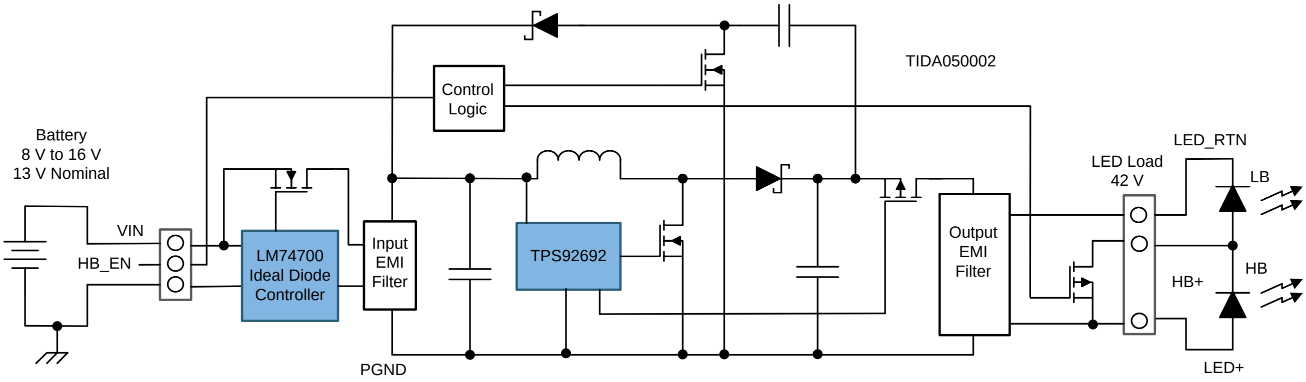


Figure 2. TIDA-050002 Block Diagram

2.2 Highlighted Products

2.2.1 TPS92692-Q1

The TPS92692 device is a versatile LED controller that can support a range of topologies. The device is intended for high-brightness LED lighting applications where efficiency, high accuracy, high power, and PWM or analog dimming (or both) are important. The device includes a gate driver for an external LED string disconnect FET to enable faster turn-on and turn-off of the LED string for high contrast ratios. In addition, it has the capability for Spread Spectrum Frequency Modulation for improved EMI performance.

A low-offset rail-to-rail current sense amplifier imporves the steady-state accuracy. This amplifier directly measures LED current using either a high-side or a low-side series current sense resistor. The device modulates LED current using either analog dimming, PWM dimming, or both simultaneously. Other features include undervoltage lockout (UVLO), wide input voltage operation, open and over-voltage protection (OVP) operation, and wide-operating temperature range with thermal shutdown.

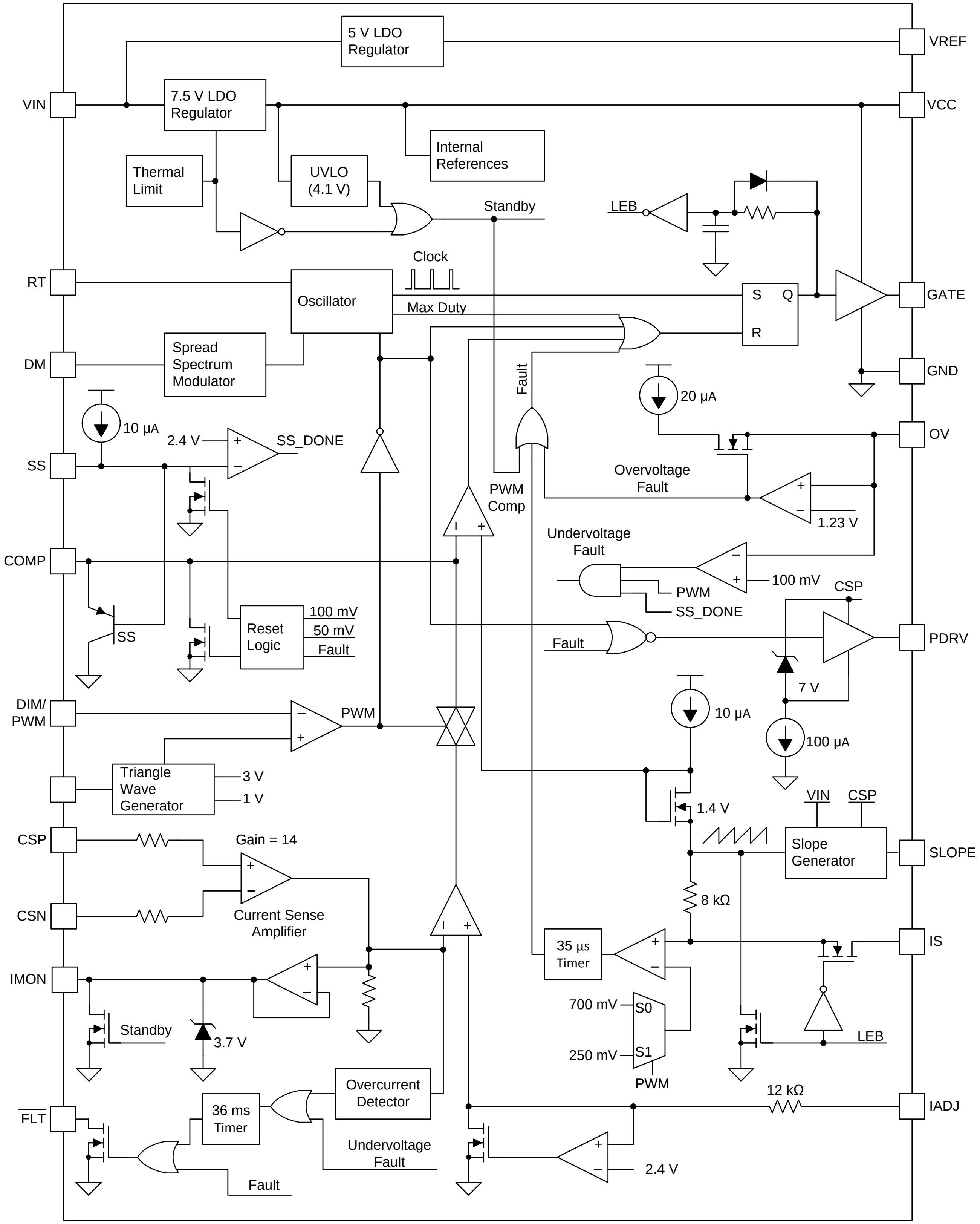


Figure 3. TPS92692 Block Diagram

The TPS92692 device operates at an input range up to 65 V in a thermally enhanced 20-pin HTSSOP package.

Key features of this device include:

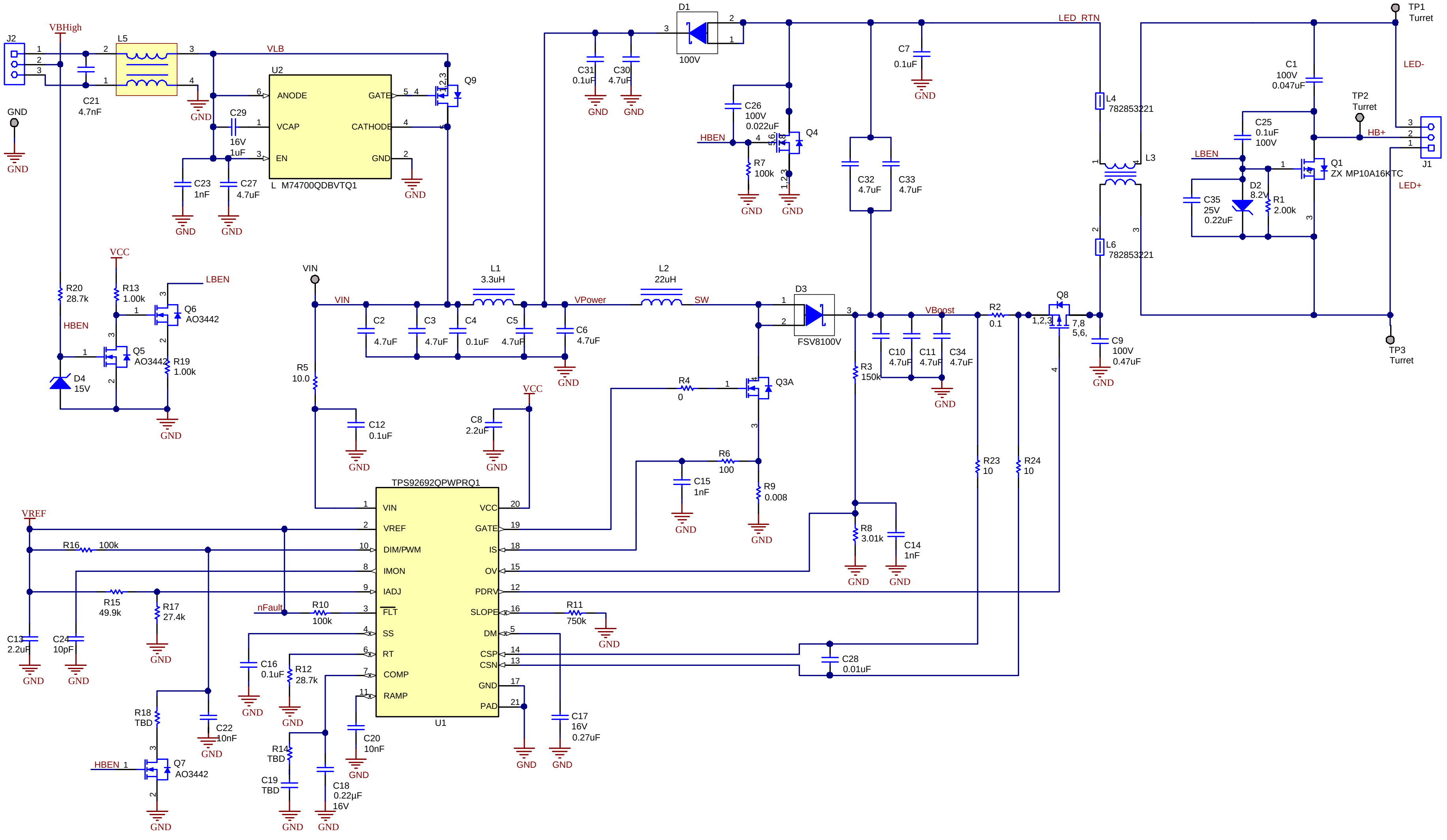
- Wide input voltage range: 4.5 V to 65 V
- Low input offset rail-to-rail current sense amplifier:
  - Better than ±4% LED current accuracy over -40°C to 150°C junction temperature range
  - Compatible with high-side and low-side current sense implementations
- High-impedance analog LED current adjust input (IADJ) with over 15:1 contrast ratio
- Over 1000:1 series FET PWM dimming ratio with integrated series P-Channel dim driver interface
- Spread Spectrum Frequency Modulation for Improved EMI
- Continuous LED current monitor output for system fault detection and diagnoses
- Programmable switching frequency with external clock synchronization capability
- Programmable soft-start and adaptive slope compensation
- Comprehensive fault protection circuitry including VCC UVLO, output OVP, cycle-by-cycle switch current limit, and thermal protection
- TPS92692-Q1: Automotive Q100 Grade 1 qualified

2.3 LM74700

The LM74700 diode controller operates in conjunction with an external N-Channel MOSFET as an ideal diode rectifier for low loss reverse polarity protection. The wide input range of 3 V to 65 V allows control of battery input voltage. With a low RDS(on) external N-Channel MOSFET, a very low forward voltage drop can be achieved while minimizing the power loss.

2.4 System Design Theory

This reference design consists of a high-performance LED controller configured in a boost or buck-boost topology. It uses EMI filtering and a load disconnect FET for high slew rate PWM dimming (see Figure 4). The input voltage range from 8 V to 16 V nominal operation with the capability to run as low as 6 V for warm crank operation. It can operate ss high as 42 V for load dump operation with reduced number of LEDs at output or input voltage transient suppressor since it can exceed the 65 V rating of the TPS92692. This design supports up to 1.25 A of output current and an output power rating of 55 W. The design is optimized to drive seven high beam LEDs and seven low beam LEDs for a total of 14 LED strings at 1.25 A from a typical voltage supply of 13 V. However, multiple combinations of input supplies and LED loads along with external synchronization or PWM can easily be created using this reference design as a starting point. Standard recommended component values (such as the VCC capacitor) are not covered in this section.



R18 is populated to allow for PWM dimming

Figure 4. TIDA050002 Schematic

2.4.1 Design Procedure

The following subsections help calculate component values and ratings. These equations are based on the key specifications listed in Table 1. This high-power example with the controller operating in boost mode for both high beam and low beam influence the component values.

2.4.1.1 Operating Parameters, Duty Cycle

The typical operating duty cycle (D), the maximum operating duty cycle (D_{MAX}), and the minimum operating duty cycle (D_{MIN}) are required to calculate the inductor values. These values can be calculated using the following equations:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} = \frac{44.8\ \text{V} - 13\ \text{V}}{44.8\ \text{V}} = 0.71 \tag{1}$$

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{IN(MIN)}}{V_{OUT(MAX)}} = \frac{47.6\ \text{V} - 7\ \text{V}}{47.6\ \text{V}} = 0.853 \tag{2}$$

$$D_{MIN} = \frac{V_{OUT(MIN)} - V_{IN(MAX)}}{V_{OUT(MIN)}} = \frac{42\ \text{V} - 18\ \text{V}}{42\ \text{V}} = 0.571 \tag{3}$$

2.4.1.2 Setting the Switching Frequency

For this design, a switching frequency of 275 kHz is selected to keep the fundamental switching noise out of the AM band and reduce the switching power loss for thermal reason. The RT resistor (R20) can be calculated for 275 kHz using Equation 4:

$$R_T = \frac{1.432 \times 10^{10}}{(f_{SW})^{1.047}} = \frac{1.432 \times 10^{10}}{(275\ \text{kHz})^{1.047}} = 28.7\ \text{k}\Omega \tag{4}$$

A value of 28.7 kΩ is selected for R12.

2.4.1.3 Inductor Value Calculation

The inductor value is calculated to ensure the circuit operates in continuous conduction mode (CCM) for a certain range of output currents at the typical operating points. In this design, the CCM to DCM boundary is set to about 1/3 of the maximum output power of 55 W, or a 1.25 A LED current with a 44 V LED load. As a result, this power boundary ($P_{O(BDRY)}$) is set for 18 W and the inductor values can be calculated using Equation 5 for the boost regulator:

$$L = \frac{{V_{IN(MAX)}}^2}{2P_{O(BDRY)} \times F_{SW}} \times \left(1 - \frac{V_{IN(TYP)}}{V_{OUT(TYP)}}\right)^2 = \frac{18^2}{2 \times 18 \times 275\ \text{kHz}} \times \left(1 - \frac{14}{44.8}\right)^2 = 23\ \mu\text{H}$$

where

- f_{sw} is the switching frequency of the circuit (5)

A value of 22 µH is selected for L2.

2.4.1.4 Peak Inductor Current

To determine the minimum saturation rating of the inductor current, the peak inductor current at the minimum input voltage must be known and the inductor sized accordingly. This peak inductor current can be calculated using the following equations for average current (I_L) and peak current ($I_{L(PK)}$):

$$I_{L(PK)} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} + \frac{V_{IN(MIN)}}{2 \times L \times F_{SW}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) = \frac{55}{7} + \frac{7}{2 \times 22\,\text{uH} \times 275\,\text{kHz}} \times \left(1 - \frac{7}{47.6}\right) = 8.35\,\text{A} \tag{6}$$

Set the current limit and inductor saturation current rating above 8.35 A.

2.4.1.5 Calculating R_{IS} (R9)

Due to the relatively high peak switch currents in this design, the equation based on current limit results in a much lower value. A $VI_{IS(LIMIT)}$ value of 70 mV is used both for high current demand during load switching from low beam to high beam and for power dissipation purpose. The value can be found using Equation 7:

$$R_{IS} = \frac{V_{IS(LIMIT)}}{I_{L(PEAK)}} = \frac{0.07}{8.35} = 0.008\ \Omega \tag{7}$$

For this design, a value of 0.008 Ω is selected for R9.

2.4.1.6 Minimum Output Capacitance

For this reference design, a maximum peak-to-peak LED ripple current ($\Delta I_{LED(PP)}$) of 50 mA or less is desired. Using the inductor current ripple and the LED string dynamic resistance, the minimum output capacitance can be calculated. For this example, the LED string designed for has a total dynamic resistance (R_D) of 4.2 Ω at 1.25 A of current.

$$C_{OUT(MIN)} = \frac{P_{O(MAX)}}{\Delta I_{LED(P\text{-}P)} \times R_{D(MIN)} \times F_{SW} \times V_{O(MAX)}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}}\right) = \frac{55}{50\,\text{mA} \times 4.2 \times 275\,\text{kHz} \times 47.6} \times \left(1 - \frac{7}{47.6}\right) = 17.05\,\text{uF} \tag{8}$$

A total output capacitance (C10, C11, C24, C32, C33) of 23.5 µF is used.

2.4.1.7 Setting the LED Current

To lower the current sense resistor power dissipation and still keep a potential analog dimming range, the current sense resistor value (R2) can be calculated using Equation 9:

$$R_{CS} = \frac{V_{IADJ(MAX)}}{14 \times I_{LED(MAX)}} = \frac{2.1}{14 \times 1.3} = 0.115\ \Omega \tag{9}$$

A 0.1-Ω,-0.33 W resistor is chosen.

2.4.1.8 Soft-Start Capacitor

A soft-start time of approximately 8 ms is used for this design to reduce stress on the input supply and prevent startup overshoots. The soft-start capacitor can be calculated using Equation 10:

$$C_{SS} = 12.5 \times 10^{-6} \left(t_{SS} - \frac{C_{OUT} \times V_{OUT}}{I_{LED}}\right) = 12.5 \times 10^{-6} \left(8\,\text{ms} - \frac{40\,\mu\text{F} \times 12\,\text{V}}{3\,\text{A}}\right) = 98\,\text{nF} \tag{10}$$

A value of 100 nF is used in this design.

2.4.1.9 Overvoltage Protection (OVP)

To protect the switching FET, diode, and output capacitors during an output open-circuit event, OVP is used. The overvoltage trip point is set to 62 V with 3 V of hysteresis. First, R_{OV2} (R6) is calculated to determine the hysteresis, and then R_{OV1} (R13) is calculated for the correct trip point using the following equations:

$$R_{OV2} = \frac{V_{OV(HYS)}}{20 \times 10^{-6}} = \frac{3}{20 \times 10^{-6}} = 150\ k\Omega$$

(11)

$$R_{OV1} = \frac{1.228}{V_{OV} - 1.228} \times R_{OV2} = \frac{1.228}{62 - 1.228} = 3.03\ k\Omega$$

(12)

The standard values of R6 = 150 kΩ and R13 = 3.01 kΩ are used.

2.4.1.10 Main N-Channel MOSFET Selection

The main switching FET (Q2) needs to be able to stand off the input voltage plus the output voltage, even during output OVP events. This FET must also have a sufficient current rating for this application. The minimum transistor voltage and current rating can be calculated using the following equations:

$$V_{DS} < V_{O(OV)} \times 1.1 = 62 \times 11 = 68.2V$$

(13)

$$I_{Q(RMS)} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} \times \sqrt{\left(1 - \frac{V_{IN(MIN)}}{V_{O(MIN)}}\right)} = \frac{55}{7} \times \sqrt{\left(1 - \frac{7}{42}\right)} = 8.49\ A$$

(14)

A 80-V, D2PAK Q-grade FET is chosen for the switching FET (Q3). This FET is chosen for low gate charge along with good thermal dissipation package.

2.4.1.11 Rectifier Diode Selection

The rectifier diode (D1) must also stand off the input voltage plus the output voltage and be rated for the maximum output current. These ratings can be calculated using the following equations:

$$V_{D(BR)} = V_{O(OV)} \times 1.1 = 62 \times 11 = 68.2\ V$$

(15)

$$I_D = I_{LEDMAX} = 1.3\ A$$

(16)

A 100-V, 8-A Q-grade schottky diode is chosen for D1.

2.4.1.12 Thermal Protection

Internal thermal protection circuitry protects the controller in the event of exceeding the maximum junction temperature. At 175°C, the converter typically shuts down, thus protecting all the circuitry in the reference design. The maximum junction temperature is a function of the system operating points (that is, efficiency, ambient temperature, and thermal management), component choices, and switching frequency.

2.4.2 Designing for Low EMI

2.4.2.1 EMI Performance

Figure 5 shows the passing conducted EMI scan for this design at a nominal 13 V input voltage and driving a 14 LEDs load in both high-beam and low-beam mode (seven LEDs in series for low beam and seven LEDs in series for high beam) at 1.25 A of LED current. The blue trace is the peak scan, and the line labeled *C25Px* denotes the peak limits for CISPR-25 Class 3. The black trace is the average scan with the line labeled "C25Ax" denoting average limits for CISPR-25 Class 3. The scan covers the entire conducted frequency range from 150 kHz to 108 MHz.

This performance by board layout only and without shielding. This pre-compliance test scan is used for engineering development and evaluation and not a certified EMI test result. If an official EMI test result is required, it is the responsibility of the end-user to submit any design based on this reference design to a certified EMI lab.

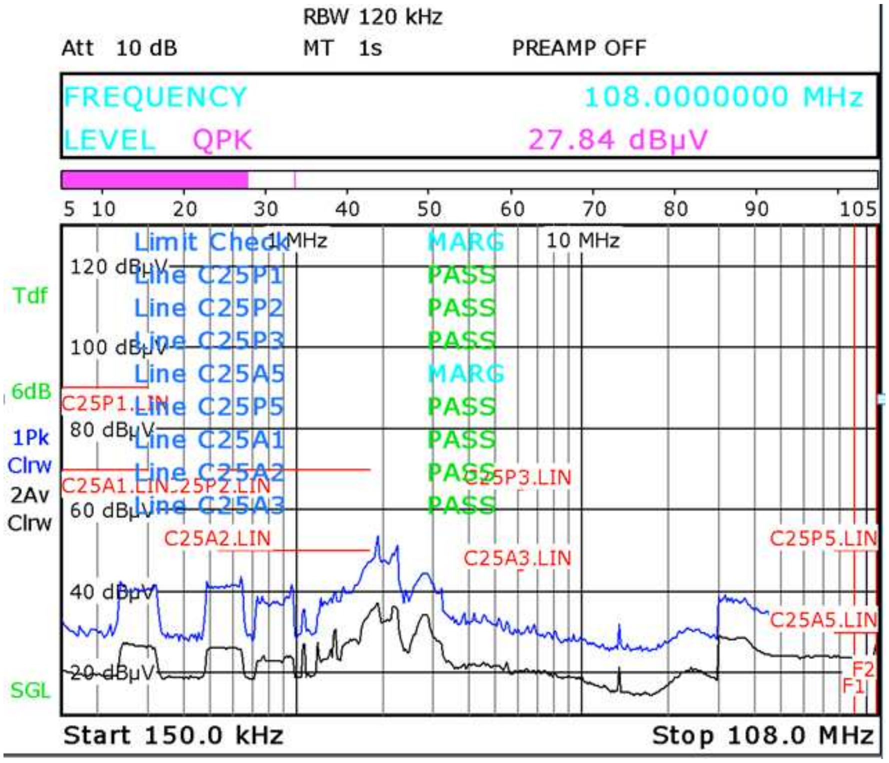


Figure 5. CISPR-25 Class 3 Conducted EMI Scan (C25Px: Peak Limits, C25Ax: Average Limits) No Shielding: V_{IN} = 13 V, V_F = 44 V, I_{LED} = 1.25 A (Pre-Compliance Data)

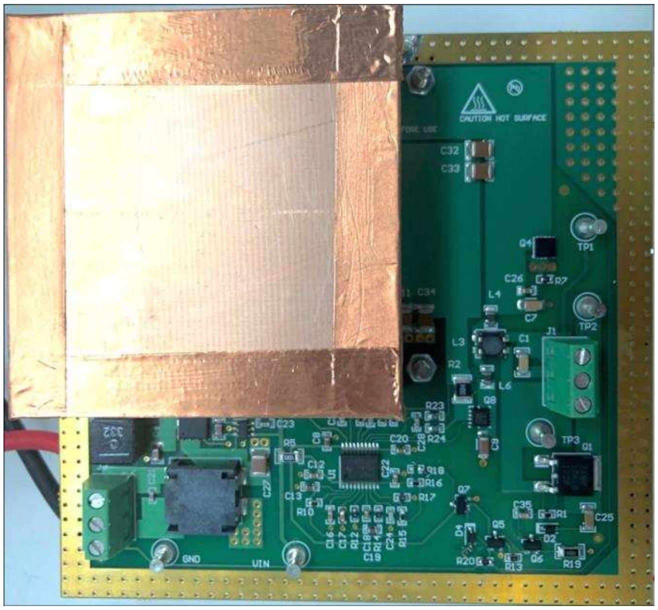


Figure 6. Shielding is required on Switching Components to pass CISPR-25 Class 5 Conducted EMI

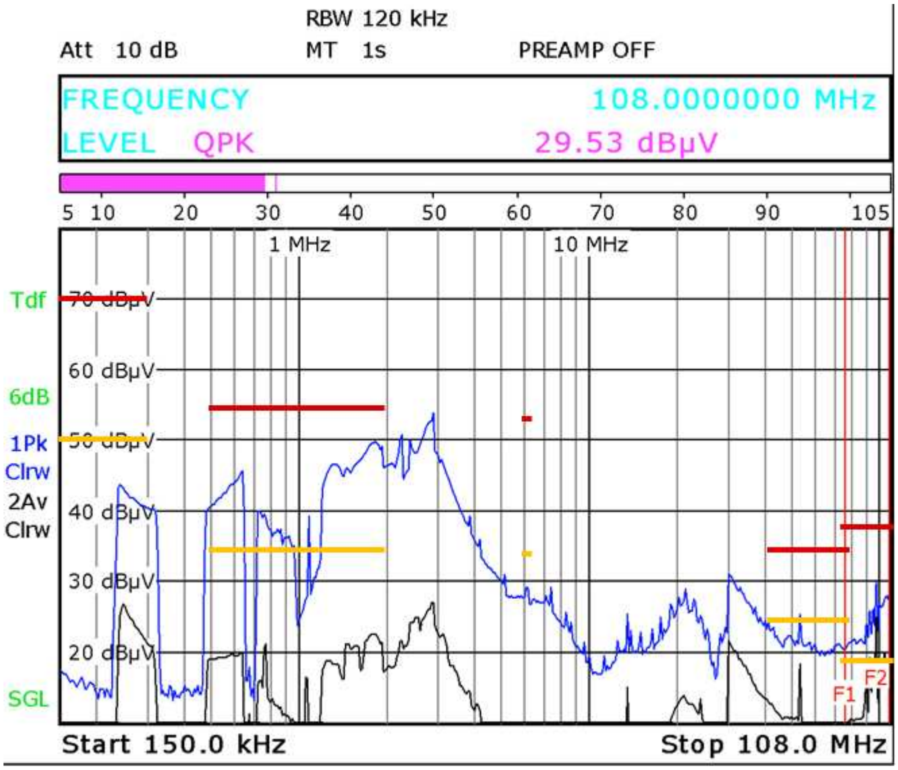


Figure 7. CISPR-25 Class 5 Conducted EMI Scan (C25Px: Peak Limits, C25Ax: Average Limits)
V_{IN} = 13 V, V_F = 44 V, I_{LED} = 1.25 A (Pre-Compliance Data)

2.4.2.2 EMI Filter Design

The input EMI filter consists of a differential mode PI filter formed by the input capacitors (C2 through C3, C4, C5, and C6) and the input inductor (L1). The primary purpose of the filter is to minimize EMI conducted from the circuit to prevent it from interfering with the electrical network supplying power to the LED driver. Frequencies in and around the switching frequency of the LED driver (fundamental and harmonics) are primarily addressed with this filter, and the filter cutoff frequency is determined by the inductor and capacitor resonance. An input common-mode filter (L5) is also included to reduce high-frequency common-mode noise at 30 MHz and above.

Sufficient differential mode noise filtering on the output is generally provided by the output capacitor assuming low equivalent-series-resistance (ESR) ceramics are used as in this reference design for CISPR-25 class 5 conducted limits. A common-mode filter has also been added to the output (L4) to account for high frequencies with unknown loads. This filtering may not be required in an end application depending on the load. This LED driver has been designed with the assumption that a connection to chassis ground is not available.

For more information on EMI filter design, see the application notes *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* and *Input Filter Design for Switching Power Supplies*.

2.4.2.2.1 Additional EMI Considerations

- Higher power levels may likely require increased EMI filtering to pass CISPR-25 class 5 limits. For lower power levels EMI filtering can also be reduced for cost reduction.
- Options include increasing input capacitance or output capacitance (or both), adding ferrite bead resistance to mitigate high-frequency EMI, or increasing input and output choke inductance for common-mode noise reduction

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This reference design does not feature any required hardware or software.

3.2 Testing and Results

3.2.1 Test Setup

Figure 8 shows the test setup. The input voltage was supplied by a DC power supply connected to the connector J2. The LED load is connected to the board using the J1 connector. Four digital multimeters (DMMs) measure input voltage, input current, output voltage, and output current.

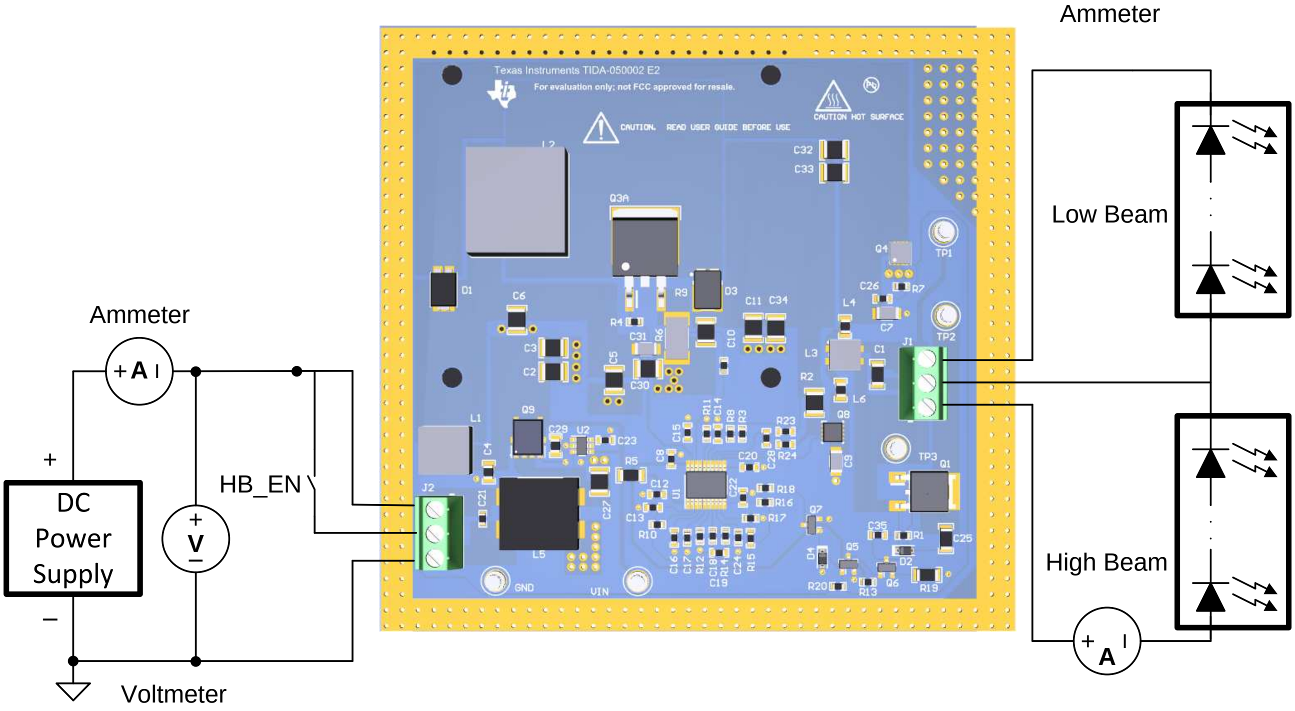


Figure 8. Test Setup Connections

3.2.2 Test Results

The test setup described in Figure 8 generates the following data for efficiency, analog dimming, and PWM dimming measurements.

Unless otherwise noted, these conditions apply to Figure 9 through Figure 20.

- V_{IN} = 13 V
- Number of LEDs for high beam: 7
- Number of LEDs for low beam: 7
- I_{LED} = 1.25 A

3.2.2.1 Nominal Operation Waveforms

LB Only

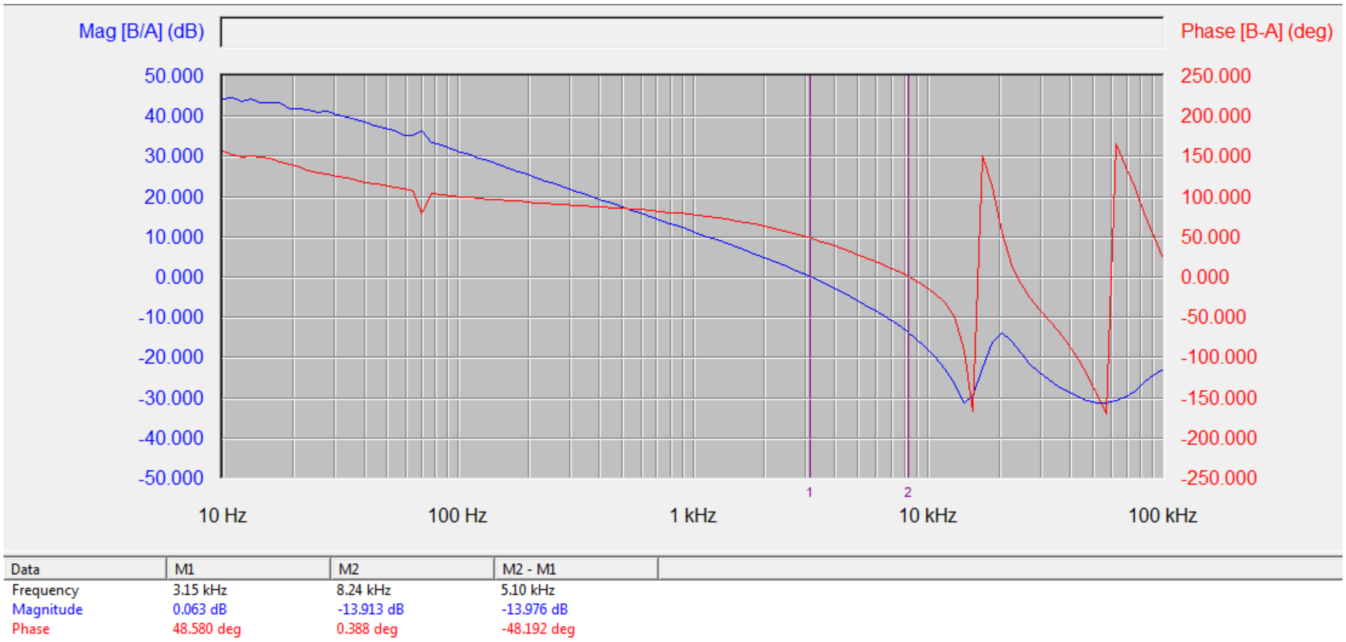
Figure 9. Low Beam Mode Startup—CH1: VIN, CH2: Switch Node (Q3 Drain) Voltage, and CH4: LED Current

HB/LB

Figure 10. High Beam/Low Beam Mode Steady State Switching—CH2: Switch Node (Q3 Drain) Voltage and CH4: LED Current for Ouput power of 55 W

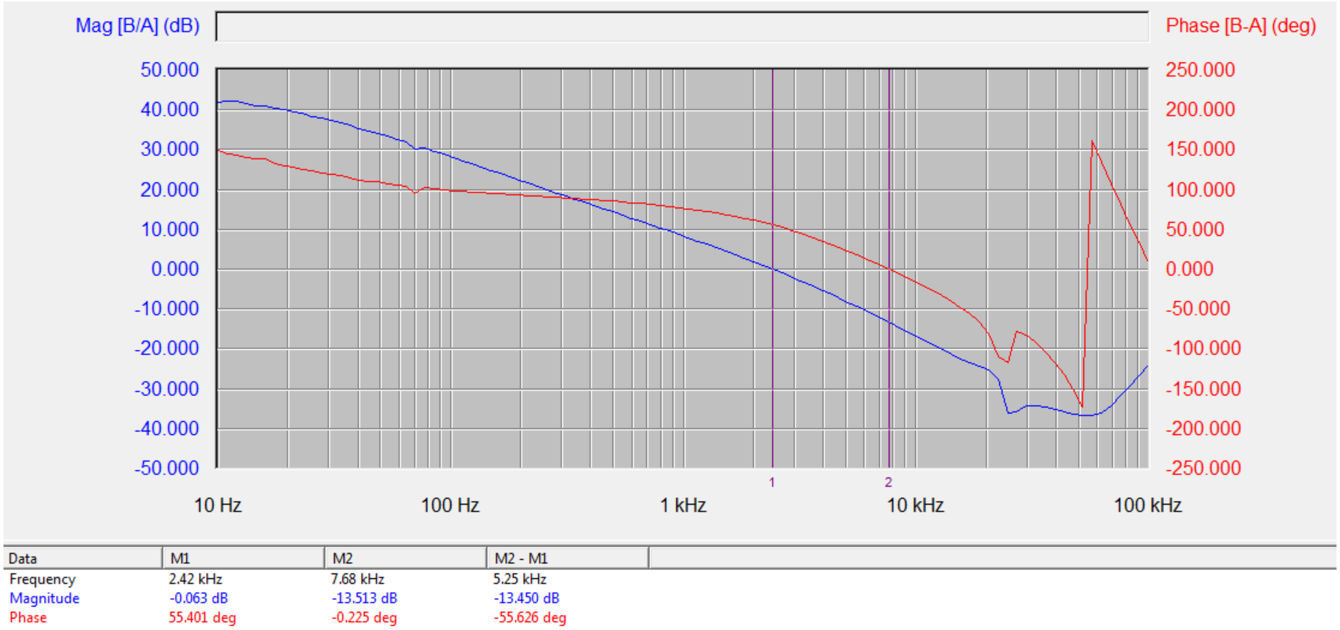
Figure 11. Normal Operation Fswitch at 275 KHz—CH1: Switch Node (Q3 Drain), CH2: VLED in High Beam and Low Beam Mode, and CH4: LED Current for Ouput power of 55 W

Figure 12. 240 Hz, 33% Duty Cycle PWM Dimming Feature with R18 (100 KΩ)— CH1: PDRV, and CH4: LED Current



Data	M1	M2	M2 - M1
Frequency	3.15 kHz	8.24 kHz	5.10 kHz
Magnitude	0.063 dB	-13.913 dB	-13.976 dB
Phase	48.580 deg	0.388 deg	-48.192 deg

**Figure 13. Gain Phase Margin for LB only in Buck Boost Mode (7 LEDs at 27.5 W)
Cross Over: 3.15 kHz Phase Margin: 48.6 Degree Gain Margin: 13.9 dB**

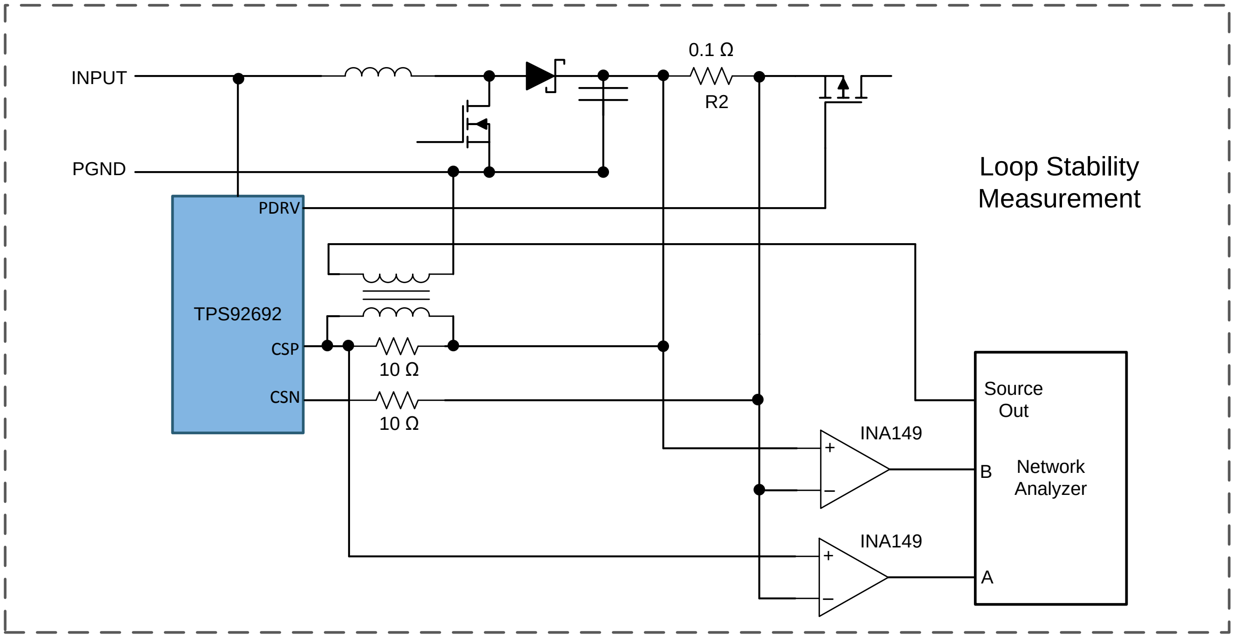


Data	M1	M2	M2 - M1
Frequency	2.42 kHz	7.68 kHz	5.25 kHz
Magnitude	-0.063 dB	-13.513 dB	-13.450 dB
Phase	55.401 deg	-0.225 deg	-55.626 deg

**Figure 14. Gain Phase Margin for HB/LB Boost Mode 55 W (Low Beam: 7 LEDs HB: 7 LEDs)
Cross Over: 2.42 kHz Phase Margin: 55.4 Degree Gain Margin: 13.5 dB**

Figure 15 shows the network analyzer circuit that measures loop stability. In addition, a pair of differential amplifier (INA149) is used to remove high common mode DC voltage from the signal feeding back to the Network Analyzer. An isolation amplifier is used to generate the injection signal. The requirement of INA149 differential amplifiers is to remove high common mode voltage which exceed the input range of the Network Analyzer for gain and phase margin measurements.

Figure 15. Loop Stability Measurements Block Diagram



3.2.2.2 Efficiency and Line Regulation: Done for different power level for Boost (Hi Beam and Lo Beam) or Boost to Battery for Lo Beam only

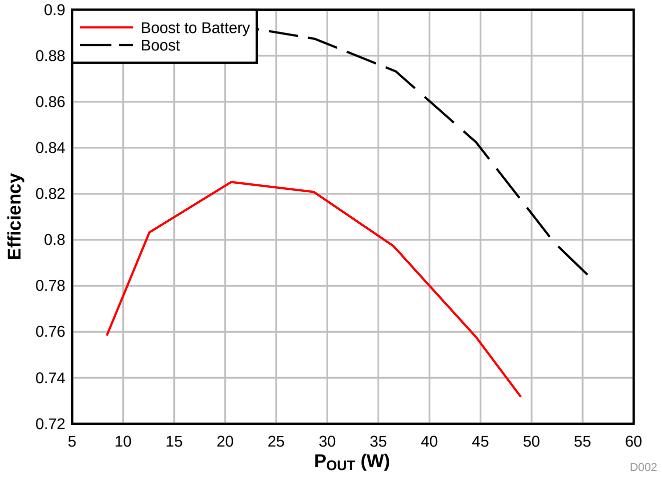


Figure 16. 8-V Input Efficiency versus P_{OUT} (W)

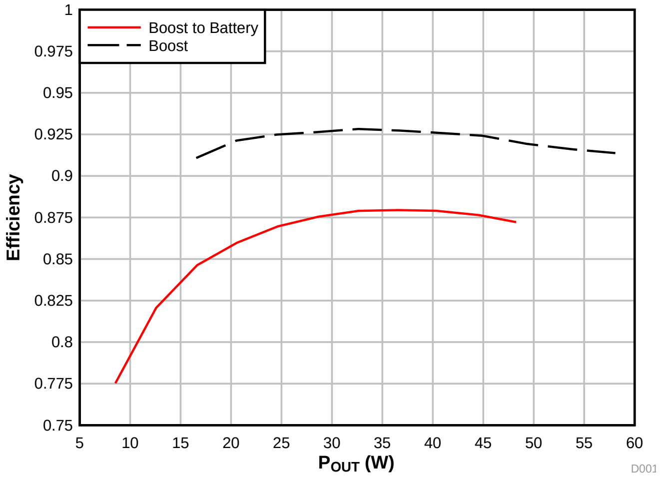


Figure 17. 13-V Input Efficiency versus P_{OUT} (W)

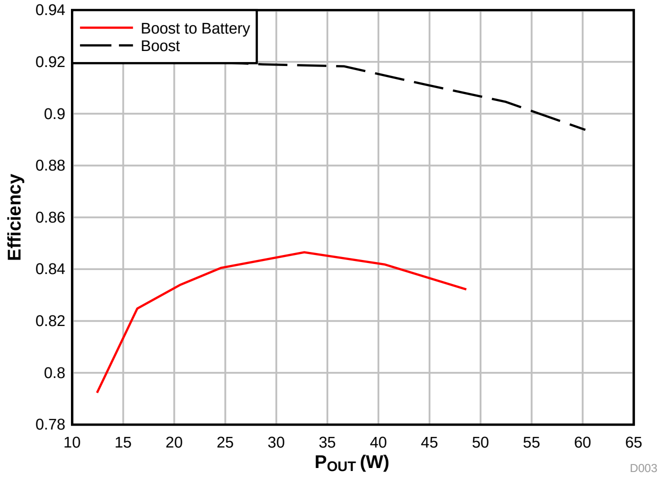


Figure 18. 16-V Input Efficiency versus P_{OUT} (W)

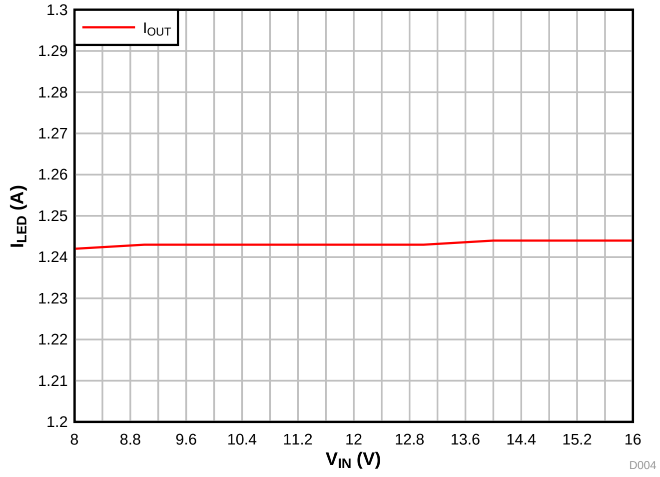


Figure 19. Line Regulation versus Vin

3.2.2.3 Thermal Scan

Figure 20 shows a thermal scan of the board running at a room temperature (≈ 24°C) with no air flow. Table 2 lists measured temperatures of key components.

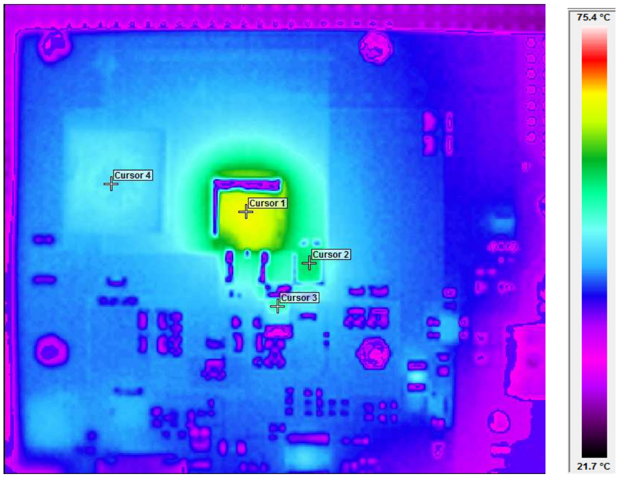


Figure 20. Thermal Scan With Heat Sink—Top-View (Power Components): V_{IN} = 13 V, HB/LB Mode (55 W), I_{LED} = 1.25 A

Table 2. Component Temperatures

CURSOR	COMPONENT	TEMPERATURE (°C)
1	Q3	66.2
2	D3	56.6
3	R9	52.3

Figure 22 shows a thermal scan of the board running at a elevated temperature (≈ 70°C) with no air flow. Table 3 lists measured temperatures of key components.

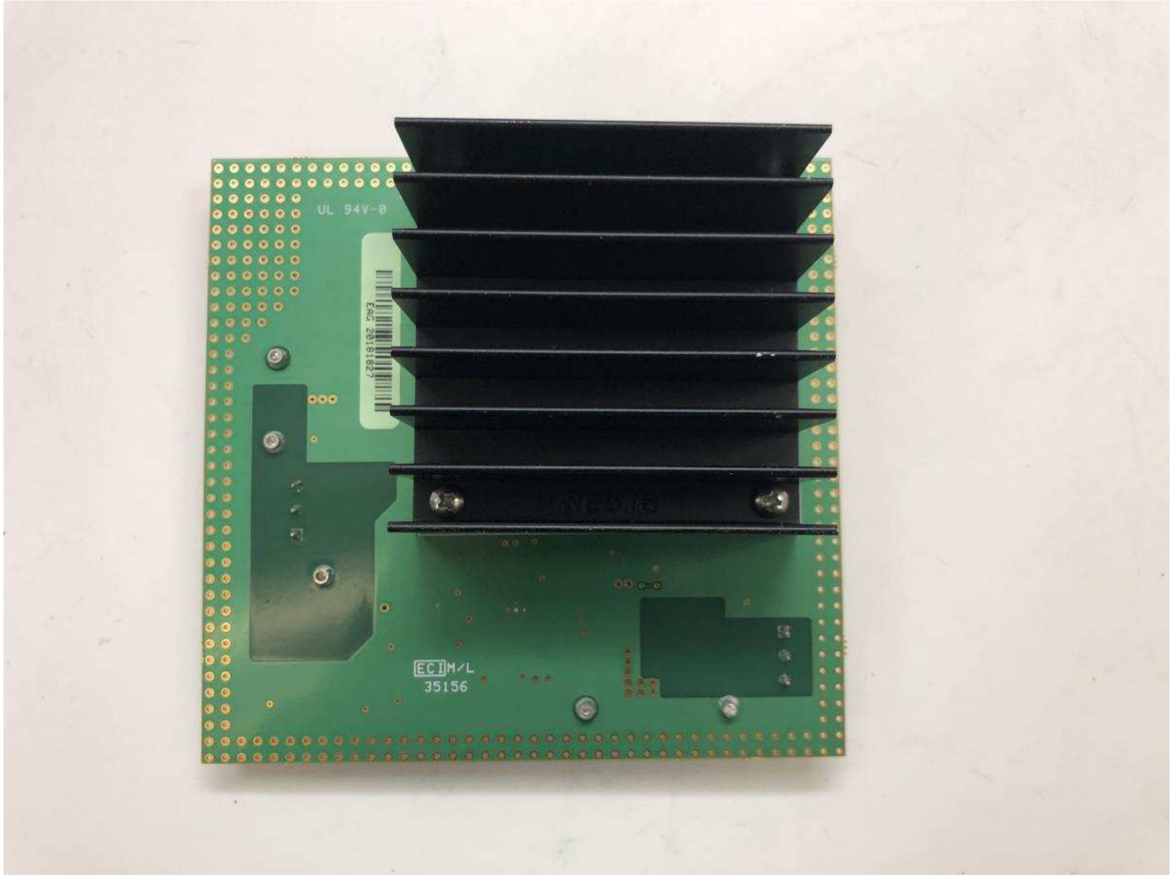


Figure 21. Picture of Heatsink on Board

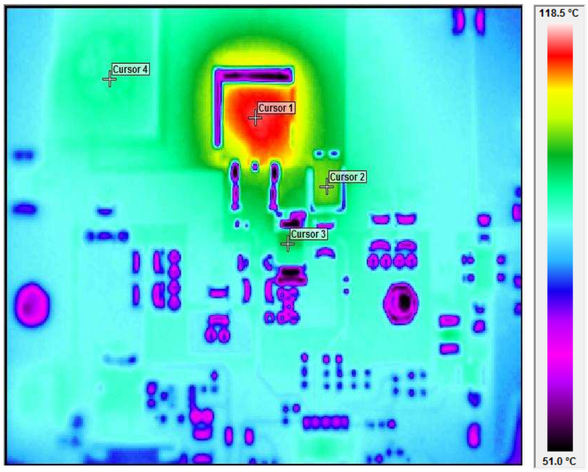


Figure 22. Thermal Scan—Top-View (Power Components): V_{IN} = 13 V, HB/LB mode (55 W), I_{LED} = 1.25 A

Table 3. Component Temperatures

CURSOR	COMPONENT	TEMPERATURE (°C)
1	Q3	114.3
2	D3	100.8
3	R9	91.3

4 Design Files

4.1 Schematics

To download the schematics, see the design files at PMP15027.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP15027.

Table 4. Bill of Materials

Designator	Quantity	Value	Description	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board	TIDA-050002	Any
C1	1	0.047 µF	CAP, CERM, 0.047 µF, 100 V, +/- 10%, X7R, 1206	C3216X7R2A473K115AA	TDK
C2, C3, C5, C6, C10, C11, C27, C30, C32, C33, C34	11	4.7 µF	CAP, CERM, 4.7 µF, 100 V, +/- 10%, X7S, 1210	C3225X7S2A475K200AE	TDK
C4	1	0.1 µF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0805	C2012X7R2A104K125AA	TDK
C7, C31	2	0.1 µF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 1206	C3216X7R2A104K160AA	TDK
C8, C13	2	2.2 µF	CAP, CERM, 2.2 µF, 16 V, +/- 20%, X7S, AEC-Q200 Grade 1, 0603	CGA3E1X7S1C225M080AC	TDK
C9	1	0.47 µF	CAP, CERM, 0.47 µF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	CGA5L2X7R2A474K160AA	TDK
C12, C16	2	0.1 µF	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X8R, AEC-Q200 Grade 0, 0603	CGA3E2X8R1E104K080AA	TDK
C14, C15, C23	3	1000 pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, C0G/NP0, 0603	C1608C0G2A102J080AA	TDK
C17	1	0.27 µF	CAP, CERM, 0.27 µF, 16 V, +/- 10%, X7R, 0603	C0603C274K4RACTU	Kemet
C18	1	0.22 µF	CAP, CERM, 0.22 µF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CL10B224KO8VPNC	Samsung
C19	1	0.033 µF	CAP, CERM, 0.033 µF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0603	CGA3E3X7S2A333K080AB	TDK
C20, C22	2	0.01 µF	CAP, CERM, 0.01 µF, 100 V, +/- 10%, X8R, 0603	C1608X8R2A103K	TDK
C21	1	4700pF	CAP, CERM, 4700 pF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E2X7R2A472K080AA	TDK
C24	1	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	CGA3E2C0G1H100D080AA	TDK
C25	1	0.1 µF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 1206	GRM319R72A104KA01D	MuRata
C26	1	0.022 µF	CAP, CERM, 0.022 µF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E2X7R2A223K080AA	TDK
C28	1	0.01 µF	CAP, CERM, 0.01 µF, 50 V, +/- 5%, C0G/NP0, 0603	C1608NP01H103J080AA	TDK
C29	1	1 µF	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0805	C0805C105K4RACTU	Kemet
C35	1	0.22 µF	CAP, CERM, 0.22 µF, 25 V, +/- 10%, X8R, AEC-Q200 Grade 0, 0603	CGA3E3X8R1E224K080AB	TDK
D1	1	100V	Diode, Schottky, 100 V, 3 A, AEC-Q101, PowerDI5	PDS3100Q-13	Diodes Inc.
D2	1	8.2V	Diode, Zener, 8.2 V, 200 mW, SOD-323	MMSZ5237BS-7-F	Diodes Inc.
D3	1	100V	Diode, Schottky, 100 V, 8 A, AEC-Q101, TO-277A	FSV8100V	Fairchild Semiconductor
D4	1	15V	Diode, Zener, 15 V, 200 mW, SOD-323	MMSZ5245BS-7-F	Diodes Inc.

Table 4. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer
GND, TP1, TP2, TP3, VIN	5		Terminal, Turret, TH, Double	1502-2	Keystone
H13	1		HEATSINK DC/DC HALF BRICK VERT	518-95AB	Wakefield Solutions
J1, J2	2		Terminal Block Receptacle, 3x1, 3.81mm, R/A, TH	1727023	Phoenix Contact
L1	1	3.3uH	Inductor, Shielded, Composite, 3.3 uH, 15.1 A, 0.01 ohm, SMD	XAL7070-332MEB	Coilcraft
L2	1	22uH	Inductor, Shielded, Composite, 22 uH, 14 A, 0.0145 ohm, SMD	XAL1510-223MEB	Coilcraft
L3	1		Coupled inductor, 2.8 A, 0.055 ohm, SMD	ACM4520-421-2P-T000	TDK
L4, L6	2	220 ohm	Ferrite Bead, 220 ohm @ 100 MHz, 2 A, 0805	782853221	Wurth Elektronik
L5	1		Coupled inductor, 8 A, 0.006 ohm, SMD	ACM1211-701-2PL-TL01	TDK
Q1	1	-100V	MOSFET, P-CH, -100 V, -4.6 A, DPAK	ZXMP10A16KTC	Diodes Inc.
Q3A	1	80V	MOSFET, N-CH, 80 V, 75 A, AEC-Q101, DDPAK	BUK9611-80E	NXP Semiconductor
Q4	1	100V	MOSFET, N-CH, 100 V, 3.8 A, 8-PowerVDFN	DMN10H120SFG-13	Diodes Inc.
Q5, Q6, Q7	3	100V	MOSFET, N-CH, 100 V, 1 A, SOT-23	AO3442	AOS
Q8	1	-60V	MOSFET, P-CH, -60 V, -3.6 A, PowerPAK 1212	SI7415DN-T1-GE3	Vishay-Siliconix
Q9	1	60V	MOSFET, N-CH, 60 V, 287 A, AEC-Q101, DFN5 5x6mm	NVMFS5C604NLT1G	ON Semiconductor
R1	1	2.00k	RES, 2.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K00FKEA	Vishay-Dale
R2	1	0.1	RES, 0.1, 1%, 0.33 W, AEC-Q200 Grade 1, 1210	ERJ-L14KF10CU	Panasonic
R3	1	150k	RES, 150 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603150KFKEA	Vishay-Dale
R4	1	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R5	1	10.0	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW120610R0FKEA	Vishay-Dale
R6	1	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100RFKEA	Vishay-Dale
R8	1	3.01k	RES, 3.01 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06033K01FKEA	Vishay-Dale
R9	1	0.008	RES, 0.008, 1%, 2 W, AEC-Q200 Grade 0, 2512	CRE2512-FZ-R008E-2	Bourns
R7,R10, R16, R18	4	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
R11	1	750k	RES, 750 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603750KFKEA	Vishay-Dale
R12	1	28.7k	RES, 28.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060328K7FKEA	Vishay-Dale
R13, R20	2	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00FKEA	Vishay-Dale
R14	1	1.43k	RES, 1.43 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K43FKEA	Vishay-Dale
R15	1	49.9k	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060349K9FKEA	Vishay-Dale
R17, R20	2	27.4k	RES, 27.4 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060327K4FKEA	Vishay-Dale
R19	1	1.00k	RES, 1.00 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	CRCW12061K00FKEA	Vishay-Dale

Table 4. Bill of Materials (continued)

Designator	Quantity	Value	Description	Part Number	Manufacturer
R23, R24	2	10	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310R0JNEA	Vishay-Dale
U1	1		LED Controller With Spread Spectrum Frequency Modulation and Internal PWM Generator, PWP0020D (TSSOP-20)	TPS92692QPWPRQ1	Texas Instruments
U2	1		Low Iq Always ON Smart Diode Controller, DBV0006A (SOT-23-6)	LM74700QDBVTQ1	Texas Instruments

4.3 Layout Prints

To download the layer plots, see the design files at PMP15027.

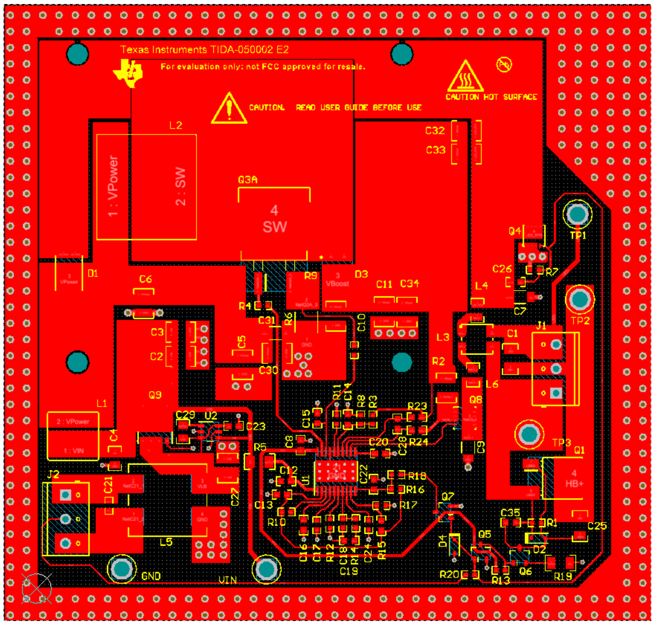


Figure 23. Top Layer

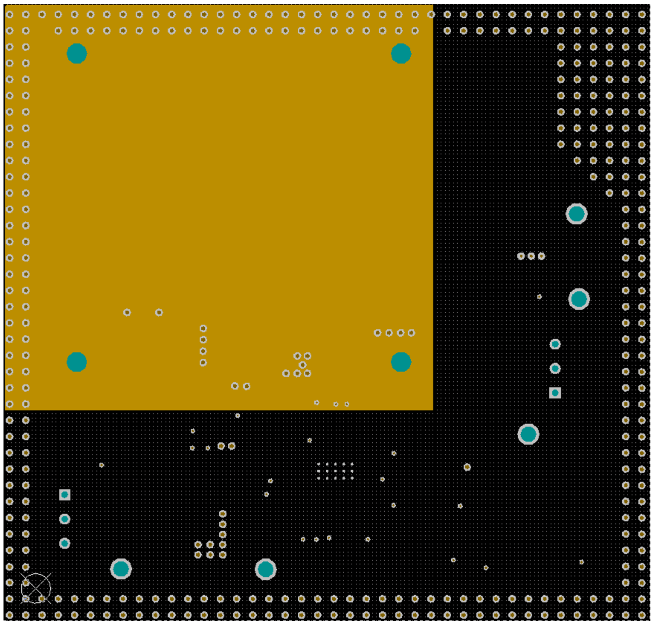


Figure 24. Middle Layer—Top

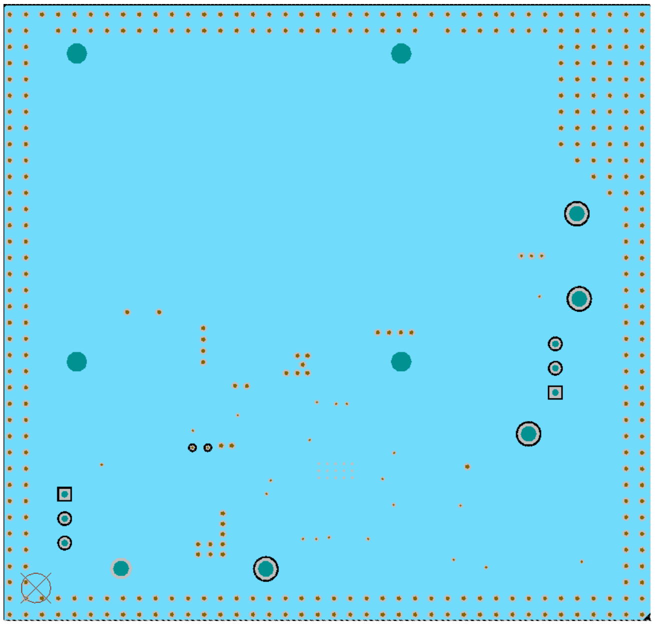


Figure 25. Middle Layer—Bottom

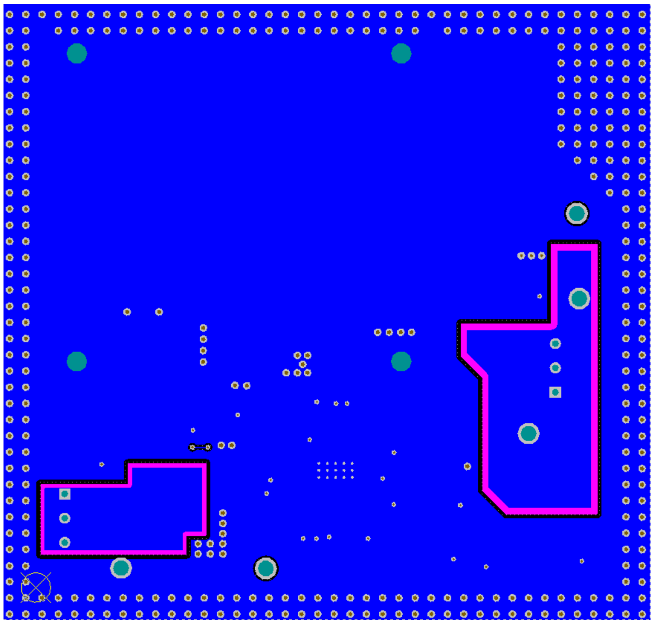


Figure 26. Bottom Layer

4.4 Altium Project

To download the Altium project files, see the design files at PMP15027.

4.5 Gerber Files

To download the Gerber files, see the design files at PMP15027.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at PMP15027.

5 Related Documentation

1. Texas Instruments, *TPS92691/TPS92691-Q1 Multi-Topology LED Driver With Rail-to-Rail Current Sense Amplifier Data Sheet*

5.1 Trademarks

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