Design Guide: TIDA-010236

4-kW GaN Totem-Pole PFC Reference Design for Appliances

Description

This reference design is a 4-kW continuous conduction mode (CCM) totem pole power factor correction (PFC) with a top-cooled gallium nitride (GaN) daughterboard and TMS320F280025C digital controller. Along with the integrated protection features of LMG352x and C2000, full protections are implemented. AC drop, surge, and Conducted Emission (CE) are fully validated, providing a cost-effective, high-efficiency, and robust totem-pole PFC design with C2000 and GaN.

Resources

TIDA-010236	Design Folder
LMG3522R030-Q1	Product Folder
TMS320F280025C	Product Folder
AMC3302	Product Folder
UCC28710	Product Folder
ISO77xx	Product Folder

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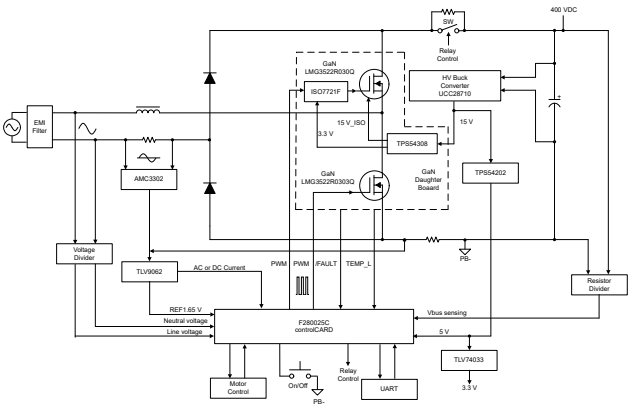
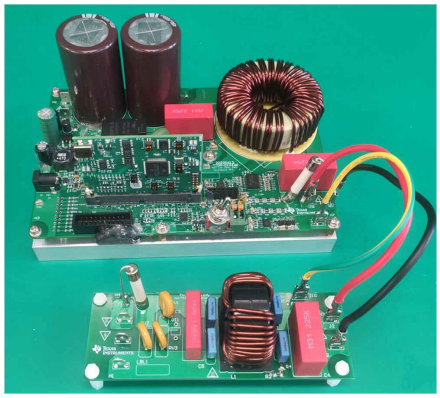
Features

- Maximum power: 4000 W at 200–277 VAC
- Peak efficiency: ≥ 98.66%; power factor: 0.999
- Diode bridge as low-speed switchers
- Onboard auxiliary high-voltage buck power supply
- Single main heat sink design
- Digital PFC with OVP, UVP, OCP, OTP protections, and UART heartbeat report
- Passed Conducted Emission test (EN55032 Class B)

Applications

- Air conditioner outdoor unit
- HVAC motor control
- Single phase online UPS
- Major appliance
- Industrial AC-DC





1 System Description

A typical residential air conditioner system runs under single-phase AC input, with < 4-kW power rate. A PFC stage is required to meet power factor and total harmonic current (iTHD) requirements.

This reference demonstrates a 4-kW, single-phase CCM totem-pole bridgeless PFC with TI GaN and C2000, with isolated current sensing, differential voltage sensing, and an isolated universal asynchronous receiver-transmitter (UART) communication port.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATION
Input Voltage | Frequency	200–277 VAC | 47–63 Hz
Input Current	20 A_{RMS} maximum
Output Voltage	400 VDC
Output Current	10 A maximum
Power Rating	4 kW at 200 VAC
Current THD	≤ 2% at 230 VAC, 4 kW
PFC Inductor	480 µH, diameter 80 mm, height 30 mm, 420 g
Output Capacitance	1000 µF × 2
Switching frequency	Up to 100 kHz
GaN $R_{DS(on)}$	30 mΩ typical

2 System Overview

This system uses the TI C2000 TMDSCNCD280025C controlCARD as the controller, an independent GaN daughter card with the LMG3522030 provides the fast switching leg, and the diode bridge acts as slow switching leg. Circuit design is simplified since the system reference point is DC bus minus.

A UCC28710 high-voltage buck power supply is implemented to provide 15-V auxiliary voltage rails. This design also uses a single main heat sink, providing easy attachment of all power devices.

Using the features of TMS320F280025C and GaN, this design implements full hardware and software protections, including input undervoltage protection (UVP), overvoltage protection (OVP), overcurrent protections (OCP) (with both one-time-shot and cycle-by-cycle), and GaN and heat sink overtemperature protection (OTP). These protections provide for a robust PFC design.

A separated filter board is designed, so electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance can be evaluated with different filters.

An isolated UART communication is implemented to report the board working status summary to the host computer periodically – like a heartbeat – providing an easy-to-understand board status.

2.1 Block Diagram

Figure 2-1 shows the main board block diagram.

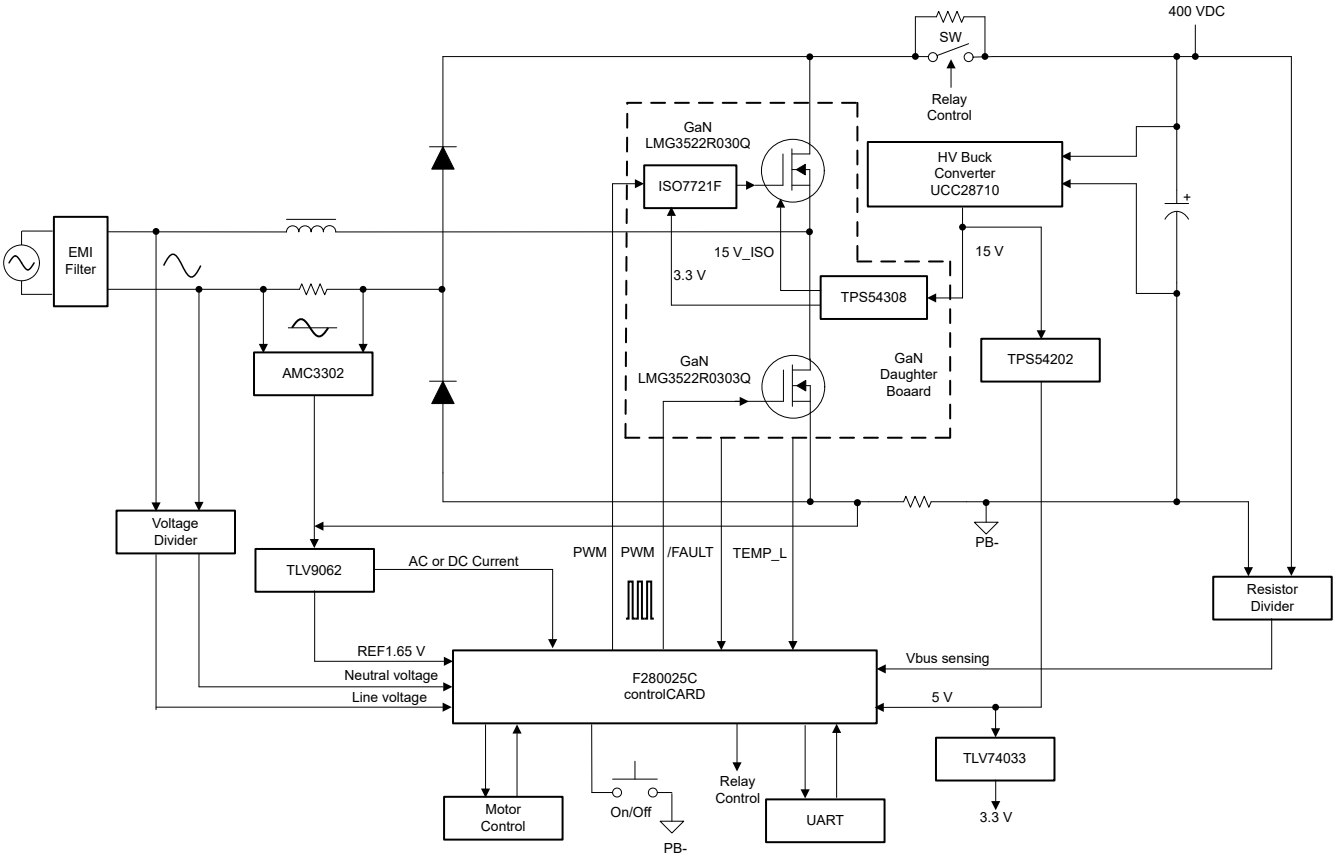


Figure 2-1. Main Board Block Diagram

Figure 2-2 shows GaN daughterboard block diagram.

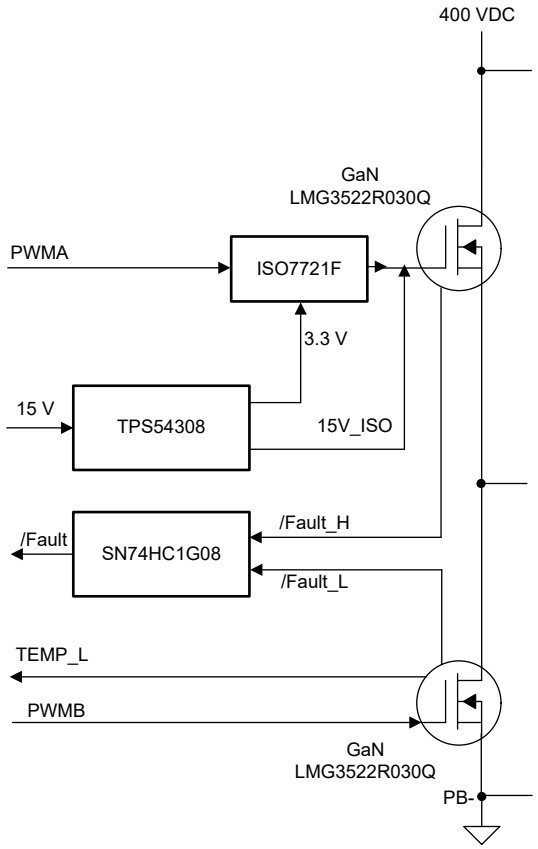


Figure 2-2. GaN Daughterboard Block Diagram

Figure 2-3 shows the filter board block diagram.

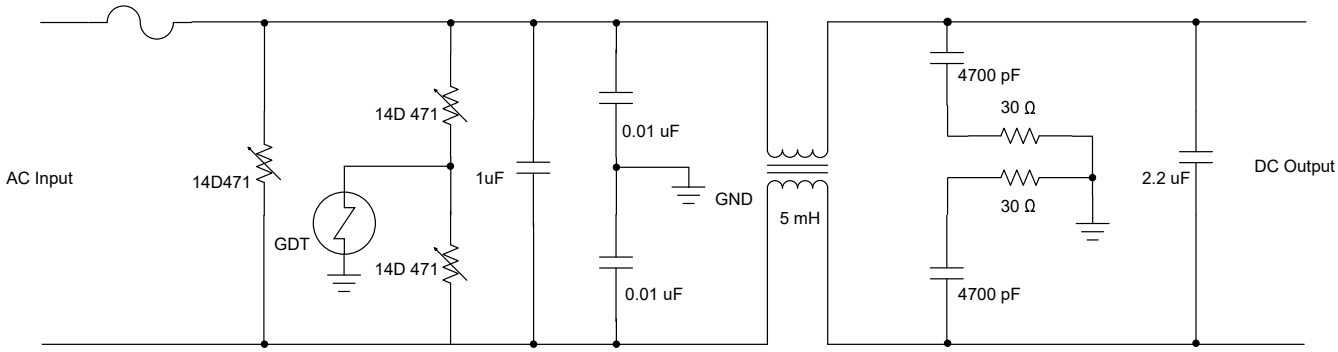


Figure 2-3. Filter Board Block Diagram

2.2 Design Considerations

The digital power design includes power stage and control stage. The power stage design in this design is similar to all other boost PFC designs. Figure 2-4 shows the power stage design parameters

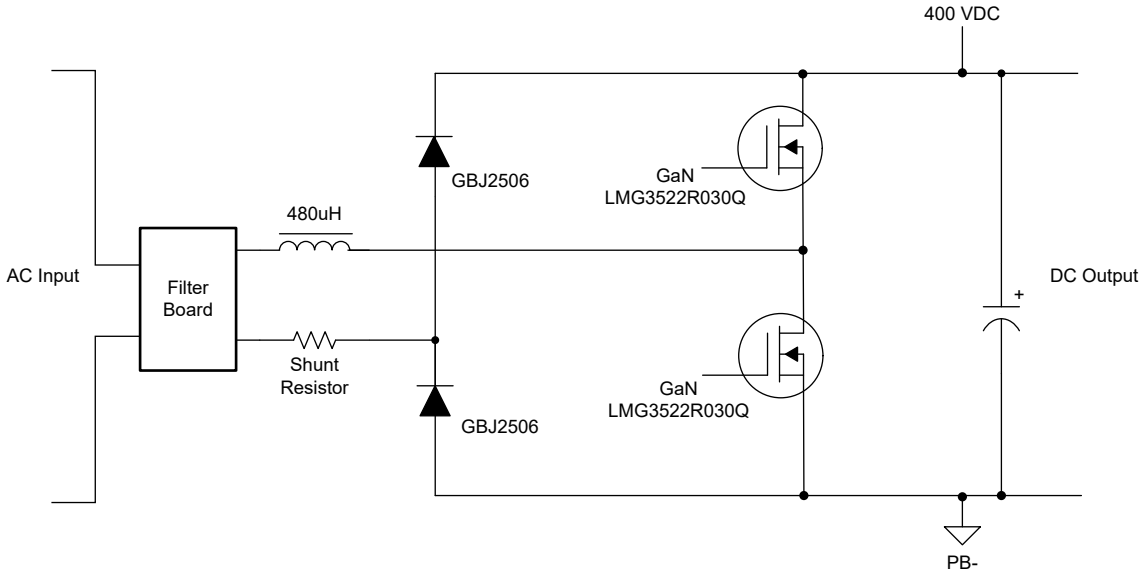


Figure 2-4. Power Stage Design Parameters

2.2.1 6-W Auxiliary Power Supply

A high-voltage buck supply with UCC28710 is implemented to provide 15-V voltage rail,no external auxiliary power supply is needed for this design. AC input can be 70–277 VAC, and output up to 400 mA.

2.2.2 AC Input Current Sensing

For appliance applications, usually *DC minus* is the reference point for the whole system, since Intelligent Power Module (IPM) for the compressor and fan motor inverter stay at the same reference point. However, there is a high common voltage for the AC current sensing of the PFC, so an isolated amplifier AMC3302 is implemented. AMC3302 has fixed gain of 41, and the input voltage range is ±50 mV. The typical common-mode output voltage is 1.44 V; however, since the ADC reference voltage is 3.3 V, the alternative signal has to move to be centered at 1.65 V, so an additional amplifier TLV9062 is implemented to provide this bias. The shunt resistors used are two 2512, 0.002 Ω in parallel. AMC3302 has a gain of 41, TLV9062 has a 0.72723 gain, so the total gain is 29.818. The final input current sense ratio is 0.029818 V/A, input current sensing rage is –55.34 A to +55.34 A.

2.2.3 DC Bus Voltage Sensing

Since DC minus is the system reference point, DC bus voltage sensing is very simple, just use resistors to attenuate high DC voltage to the 3.3-V range. In this design, the DC bus voltage sense ratio is 0.005125, and the voltage sensing range is 0 V to 644 V.

2.2.4 AC Input Voltage Sensing

To control system costs, use resistor networks for AC input voltage sensing. Both Line and Neutral are attenuated by resistors while referring to DC minus, then a subtraction of the two attenuated signals is the AC input voltage.

2.2.5 GaN Driving

This design has an independent half-bridge GaN daughterboard as the switching leg, which makes the design easy to mounted to the main heat sink. The bottom GaN interfaces to DSP directly, while the top GaN needs an isolator ISO7721F since the reference point is different from DSP. This isolator also provides an isolated GaN FAULT signal to the MCU to create a one-shot trigger protection.

To power on the top GaN, a flybuck auxiliary power supply with the TPS43208 device is implemented to provide an isolated 15-V rail to the top GaN. This power supply also generates a non-isolated 3.3-V rail to ISO7721F and an AND gate of the SN74AHC1G108, which collects FAULT signals from both the top and bottom GaN and then reports the information to DSP.

The temperature signal of the bottom GaN is also routed to the digital-signal processor (DSP) which gives the measure of the junction temperature.

2.2.6 Inrush Current Protection at Powering On

Two bulk capacitors on the DC bus lead to huge inrush current upon powering on. In this design, a 50-Ω PTC and relay work together to limit this inrush current. Software engages the relay within a specified delay after powering on.

Note

Do not heavily load the DC bus at power on, since the PTC carries all the load current at this time. A heavy DC load (< 800 Ω) triggers PTC protection. If a PTC protection is triggered, wait for the trigger release after cooling down.

2.2.7 Overcurrent Protection

There are three types of current protections in this design.

Cycle-By-Cycle current protection: TMS320F280025C has comparator subsystems (CMPSS), windowed comparators, which can protect overcurrent in both positive and negative half cycles. In this design, software set at 40-A current triggers CMPSS. CMPSS is configured as cycle-by-cycle protection.

GaN overcurrent protection: GaN pulls down the FAULT signals at overcurrent. The top and bottom FAULT signal are ANDed and reported to TMS320F280025C to create a trip zone (TZ) signal to stop PWM, this is a one-shot-trip protection. Typical drain overcurrent for LMG3522R030 is 70 A.

Overload current protection: software monitors AC input current and stops PFC if the load current is too high. In this design, overload current is set to 26 A_{RMS} in software.

2.2.8 AC Input Undervoltage Protection

Software does not start PFC if the input voltage is too low. The software is set to 170 VAC in this design.

2.2.9 DC Bus Overvoltage Protection

The CMPSS module is set for DC bus overvoltage protection. The trigger voltage is 440 VDC.

2.2.10 GaN Temperature Monitor and Protection

LMG3522R030 reports its temperature at the TEMP pin in pulse-width modulation (PWM) mode. An Enhanced Capture (eCAP) module in the TMS320F280025C is configured to monitor this PWM signal. Software captures this ratio, and determines the GaN overtemperature protection. In this design, PFC stops for GaN overtemperature at 125°C.

2.2.11 Heat Sink Temperature Monitor and Protection

An negative temperature coefficient (NTC) thermistor is attached to the heat sink to monitor the heat sink temperature. In this design, PFC stops for a heat sink temperature over 80°C.

2.2.12 UART Heartbeat Report

An isolated UART reports the *board working* status every second. The following information is reported:

- GaN temperature duty
- temperature
- heat sink temperature
- input voltage
- input current
- input power
- output voltage
- errors
- total working time
- firmware version

The UART baud rate is 115200bps, and in ASCII mode.

2.2.13 Motor Control Interface

TMS320F280025C has the ability to control a PFC and motor inverter at same time. In this design, motor signals are reserved at the two connectors, J10 and J11.

2.3 Highlighted Products

2.3.1 LMG352xR030

The LMG352xR030 GaN FET with integrated driver and protection enables designers to achieve new levels of power density and efficiency in power electronics systems.

The LMG352xR030 integrates a silicon driver that enables switching speed up to 150 V/ns. TI's integrated precision gate bias results in higher switching safety operation area (SOA) compared to discrete silicon gate drivers. This integration, combined with our low-inductance package, delivers clean switching and minimal ringing in hard-switching power supply topologies. Other features, including adjustable gate drive strength for EMI control, overtemperature, and robust overcurrent protection with fault indication, provide optimized BOM cost, board size, and footprint.

Advanced power management features include digital temperature reporting and TI's ideal diode mode. The temperature of the GaN FET is reported through a variable duty cycle PWM output, which enables the system to manage loading. Ideal diode mode maximizes efficiency by reducing third-quadrant losses by enabling adaptive dead-time control.

2.3.2 TMS320F28002x

The TMS320F28002x (F28002x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high-power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 100 MHz of signal processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Trigonometric Math Unit (TMU) and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems.

High-performance analog blocks are integrated on the F28002x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide real-time signal chain performance. Fourteen PWM channels, all supporting frequency-independent resolution modes, enable control of various power stages from a 3-phase inverter to advanced multilevel power topologies.

2.3.3 UCC2871x

The UCC2871x family of flyback power supply controllers provides isolated-output Constant-Voltage (CV) and Constant-Current (CC) output regulation without the use of an optical coupler. The devices process information from the primary power switch and an auxiliary flyback winding for precise control of output voltage and current.

The output drive interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley switching reduces switching losses. Modulation of switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges. The controllers have a maximum switching frequency of 100 kHz and always maintain control of the peak primary current in the transformer. Protection features help keep primary and secondary component stresses in check.

2.3.4 TLV906x

TLV906x operational amplifiers (op amps) with rail to-rail input- and output-swing capabilities. These devices are highly cost-effective designs for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the TLV906x is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the OPAx316 and TLVx316 devices.

2.3.5 TPS54308

The TPS54308 is a 4.5-V to 28-V input voltage range, 3-A synchronous buck converter. The device includes two integrated switching FETs, internal loop compensation, and 5-ms internal soft start to reduce component count. By integrating the MOSFETs and employing the SOT-23 package, the PS54308 achieves high power density and offers a small footprint on the PCB.

The TPS54308 operates in force continuous conduction mode (FCCM) during light load conditions. The switching frequency is maintained at an almost constant level over entire load range. This make the device an excellent choice for a flybuck topology, which we use in this design. Cycle-by-cycle current limit in both high-side MOSFETs protects the converter in an overload condition and is enhanced by a low-side MOSFET freewheeling current limit, which prevents current runaway. Hiccup mode protection is triggered if the overcurrent condition has persisted for longer than the present time.

3 Hardware, Software, Testing Requirements, and Test Results

This section details the hardware and explains the different sections on the board and how to set them up for the experiments as outlined in this design guide.

3.1 Hardware Requirements and Assembly

This design has 4 parts: heat sink, GaN daughterboard, main board, and filter board.Figure 3-1 shows the side view of the kit, Figure 3-2 shows relative position of the heat sink, GaN daughterboard, and main board. Two top-side cooled GaN LMG3522R030 devices are adopted on the bottom side of the GaN daughterboard so the devices can be cooled down with the heat sink and diode bridge. The kit is usually shipped fully-assembled; however, the assembly steps are provided in the following list.

1. Mount 5-pieces M3 × 10-mm standoffs (3-mm male end with outside thread and female on the other end with inner thread) to heat sink corners.
2. Adhere thermal interface materials (TIM), (0.5 mm thickness, Fujipoly GR80A-0H-050GY in this design) on heat sink underneath the GaN daughterboard, make sure TIM is big enough, at least 3 mm extended from any bottom pins and traces of the GaN daughterboard. But 4 pieces of the mechanical holes need 7-mm diameter keepout of TIM.
3. Locate the GaN daughterboard on the heat sink with 4 bottom side standoffs aligned to the four mechanical mounting holes on the heat sink. Fasten 4-pcs M3 × 6-mm from the GaN daughterboard to the heat sink.
4. Place thermal grease on the bottom side of the diode bridge.
5. Fix the heat sink temperature probe to the heat sink with an M3 × 4-mm screw.
6. Align J2 of the GaN daughterboard and J4 of main board, J2 can slide into J4 from the bottom side holes of J4.
7. Align the main board corner holes to 5-pcs standoffs on the heat sink, and fasten them with M3 × 8-mm screws.
8. Align the diode bridge holes to the corresponding holes on the heat sink, and fasten the diode bridge to the heat sink with an M3 × 8-mm screw.
9. Screw down 3-pcs M3 × 6-mm screws from the main board holes (HV, SW, and GND) to MP1, MP4, and MP7 standoffs on the GaN daughterboard. These 3-piece screws also act as high-current path between the GaN daughterboard and main board.
10. Connect the main board (J1,J2, and J3) to the filter board (J2, J4, and J10) with harness.
11. Connect the DC output cable at J5 and J7 on the main board.
12. Connect the AC input cable at J1, J3, and J5 on the filter board.

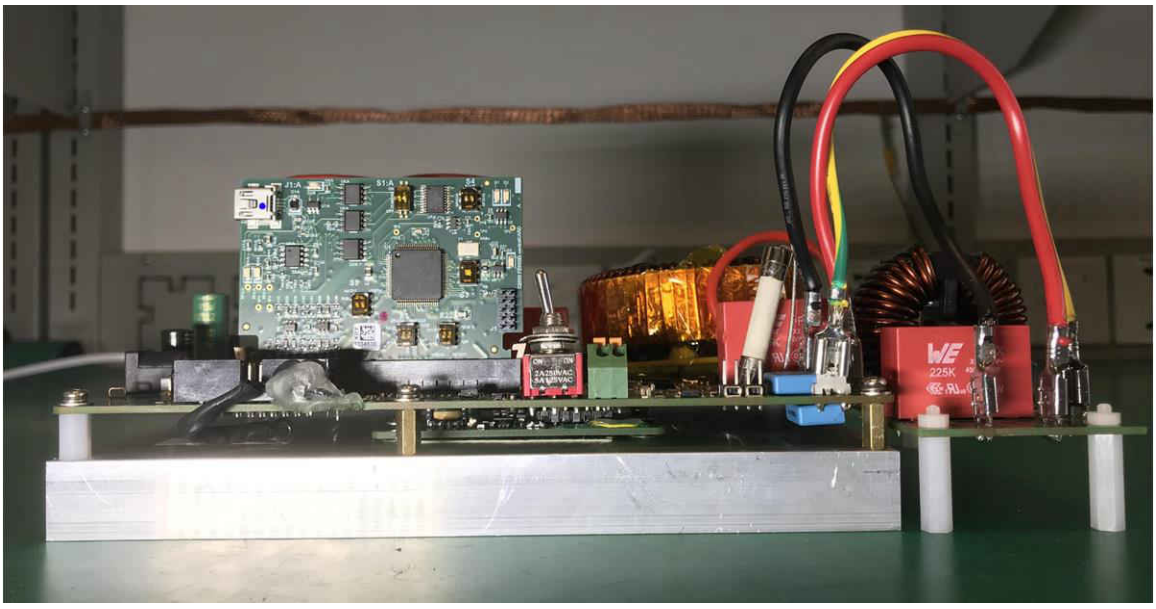


Figure 3-1. TIDA-010236 Reference Design Side View

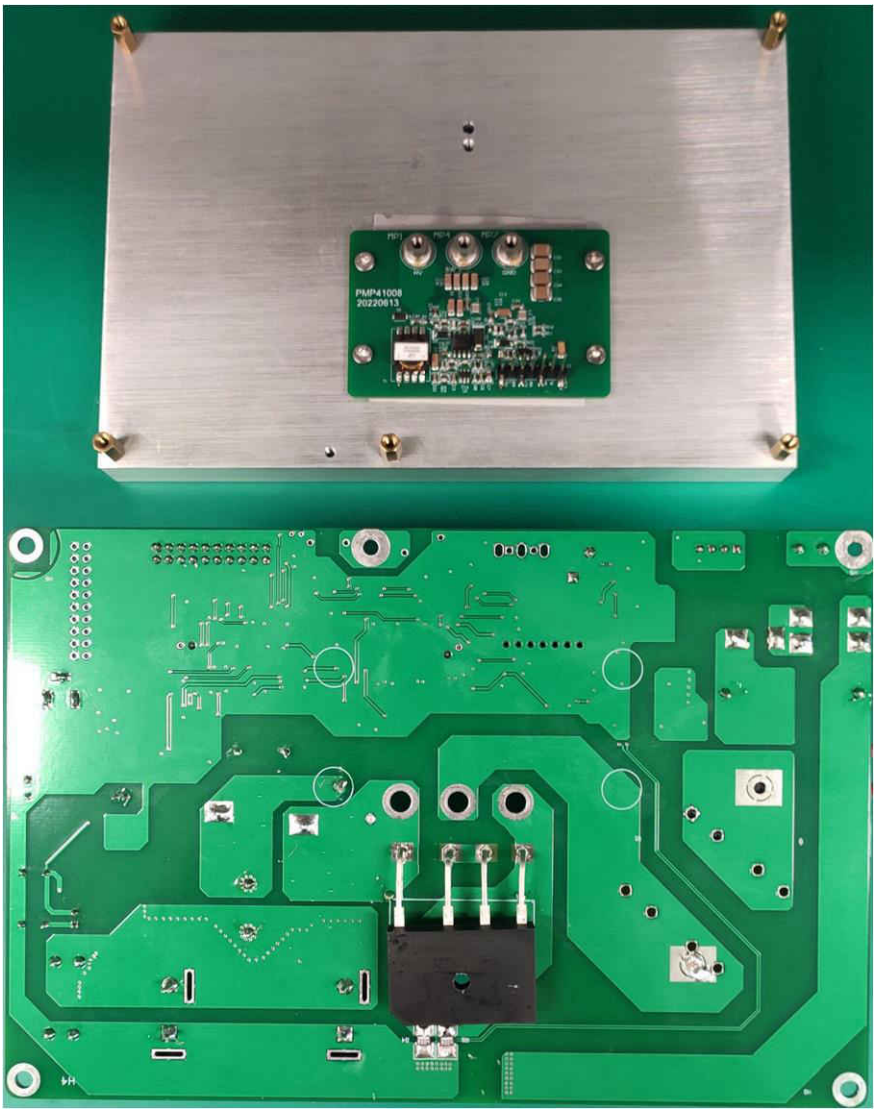


Figure 3-2. Heat Sink, GaN Daughterboard, and Main Board

3.1.1 Test Equipment Requirements

1. Programmable AC source (≥ 4 kVAC)
2. Isolated high-voltage electrical DC load (≥ 400 VDC, 4 kW)
3. Air cooling fan
4. Host PC or laptop with USB port

3.2 Software Requirements

This reference design has the following software requirements:

1. Flash TMS320F280025C controlCARD with firmware, TIDA-010236_FW_V1.01
2. UART terminal software on the host PC

3.3 Test Setup

Use the following steps to set up the test:

1. Make sure the TMS320F280025C controlCARD board is well inserted and locked at J9 on the main board
2. Connect the USB cable from TMS320F280025C controlCARD to the host PC
3. Run any UART terminal software on the PC, set the correct UART port at 115200bps, and in ASCII mode
4. Connect the AC source cable to the input terminals J1 and J3 on the main board, but *do not* power up

5. Connect the DC load to output terminals J5 and J7 (J5 is DC positive, J7 is DC negative, the load must be isolated with grid and PE line)
6. Use a forced-air cooling fan to cool down the heat sink
7. Connect current and voltage meters or power analyzer, if needed

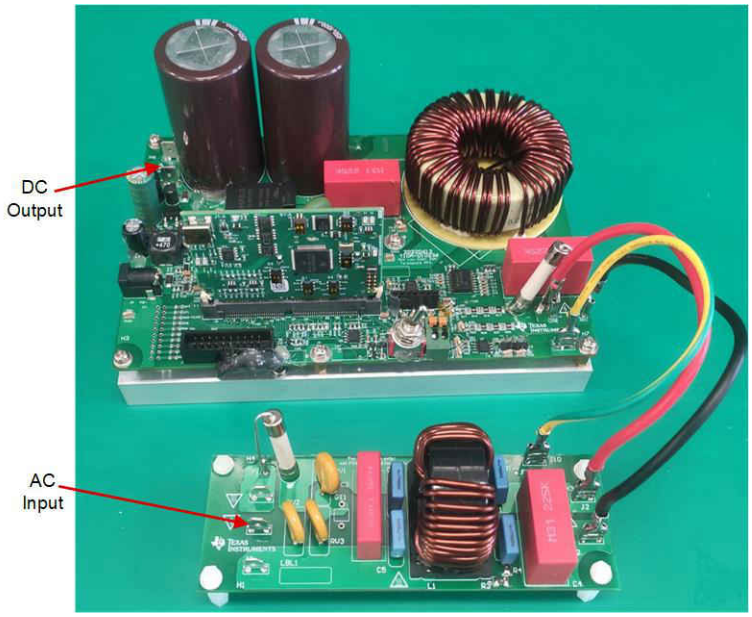


Figure 3-3. Test Setup

3.4 Test Results

3.4.1 Test Procedures

Figure 3-4 shows the equipment under test (EUT) setup.

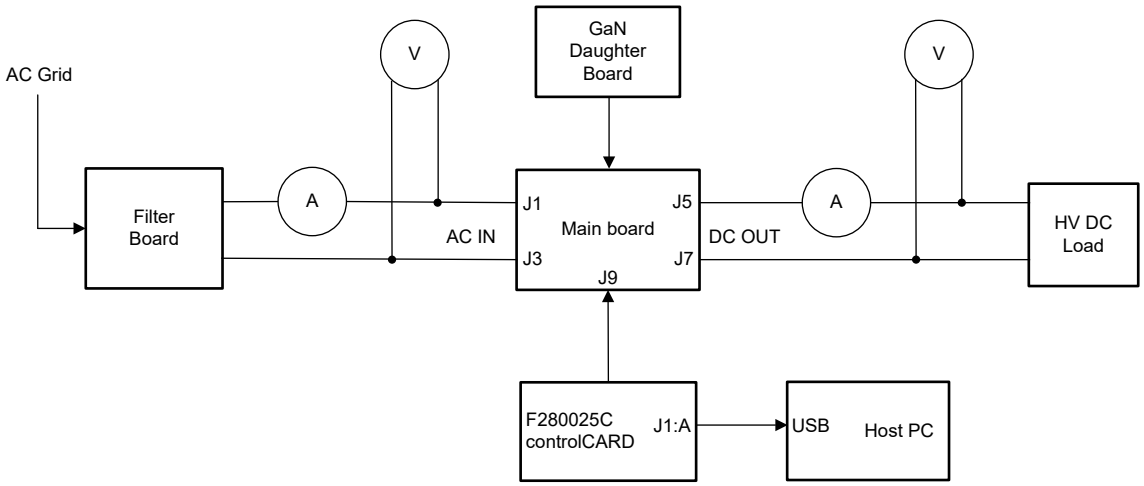


Figure 3-4. EUT Setup

3.4.1.1 Test Procedures Under 90 VAC

Use the following steps to set up the test under 90 VAC:

1. Load DC output with a greater than 800-Ω power resistor or with a less than 0.5-A load current
2. Set AC source at 90 VAC, 50 or 60 Hz, then power on.
3. Check the UART terminal software on the host PC. A heartbeat report needs to be detected. The board status needs to be undervoltage protection (UVP).
4. Power off AC source

3.4.1.2 Test Procedures Under 220 VAC

Use the following steps to set up the test under 220 VAC:

1. Load DC output with a greater than 800-Ω power resistor or with a less than 0.5-A load
2. Set AC source at 220 VAC, 50 or 60 Hz, then power on. PFC starts, DC output voltage is 400 VDC.
3. Check UART terminal software, UART information and waveforms
4. Increase the load step by step until 4 kW is reached
5. Power off AC sources

3.5 Performance Data: Efficiency, iTHD, and Power Factor

Figure 3-5 shows the related 230 VAC efficiency curve.

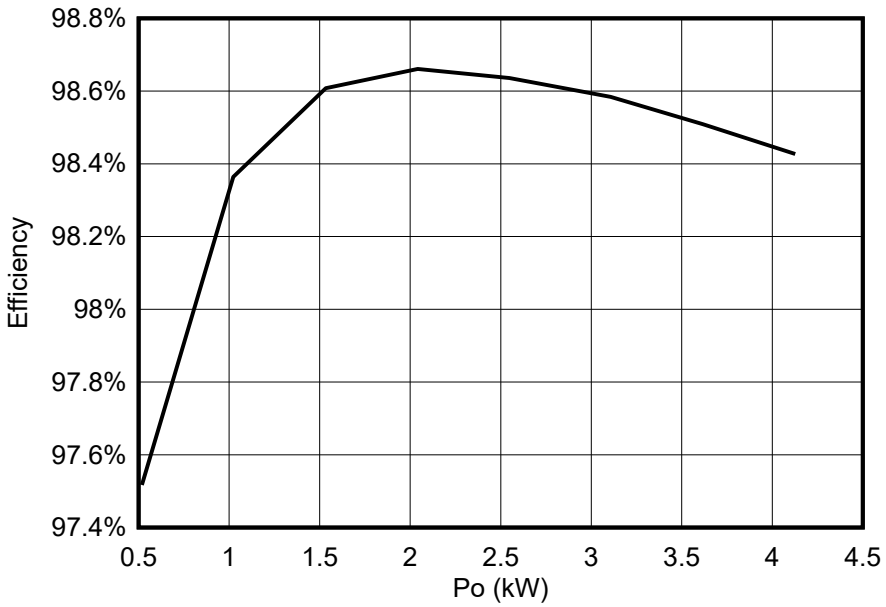


Figure 3-5. Efficiency Curve, 230 VAC

Table 3-1 shows the efficiency, iTHD, and power factor data with 230-VAC input, without including the control and driving power loss.

Table 3-1. Efficiency, iTHD, and Power Factor Data Under 230-VAC Input

V_{IN}/V	I_{IN}/A	P_{IN}/kW	V_{OUT}/A	I_{OUT}/A	P_{OUT}/kW	EFFICIENCY	iTHD	PF
229.71	2.3875	0.5179	399.37	1.2643	0.5050	97.517%	18.383%	0.9443
229.45	4.5206	1.0230	399.44	2.5190	1.0063	98.364%	9.420%	0.9863
229.18	6.7310	1.5339	399.41	3.7863	1.5125	98.608%	6.125%	0.9943
228.91	8.9450	2.0415	399.44	5.0417	2.0142	98.661%	4.379%	0.9970
228.64	11.1670	2.5486	399.43	6.2920	2.5138	98.636%	3.375%	0.9982
228.34	13.6240	3.1073	399.45	7.6670	3.0663	98.584%	2.739%	0.9988
228.06	15.8710	3.6163	399.47	8.9160	3.5624	98.509%	2.353%	0.9991
227.78	18.1300	4.1267	399.47	10.1650	4.0618	98.427%	2.000%	0.9993

Figure 3-6 shows 200 VAC and 277 VAC efficiency curves.

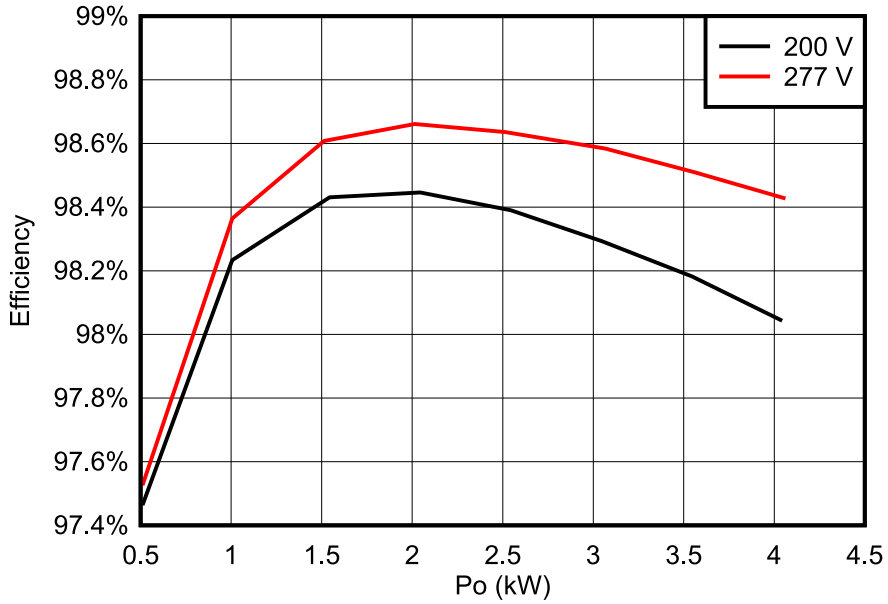


Figure 3-6. Efficiency Curve, 200 VAC and 277 VAC

Table 3-2 and Table 3-3 show the efficiency with 200-V and 277-V input, respectively, without including the control and driving power.

Table 3-2. Efficiency With 200-VAC Input

P_{IN}/kW	V_{OUT}/V	I_{OUT}/A	P_{OUT}/kW	EFFICIENCY
0.5165	399.48	1.2598	0.5033	97.452%
1.0240	399.48	2.5177	1.0059	98.233%
1.5679	399.47	3.8630	1.5433	98.431%
2.0767	399.49	5.1170	2.0433	98.446%
2.5858	399.49	6.3680	2.5442	98.390%
3.0998	399.49	7.6250	3.0469	98.293%
3.6121	399.50	8.8750	3.5464	98.182%
4.1243	399.50	10.1190	4.0436	98.043%

Table 3-3. Efficiency With 277-VAC Input

P_{IN}/kW	V_{OUT}/V	I_{OUT}/A	P_{OUT}/kW	EFFICIENCY
0.5167	399.44	1.2630	0.5046	97.657%
1.0217	399.35	2.5206	1.0068	98.538%
1.5302	399.36	3.7850	1.5116	98.787%
2.0353	399.30	5.0390	2.0125	98.877%
2.5401	399.30	6.2900	2.5121	98.898%
3.0892	399.24	7.6490	3.0545	98.876%
3.5941	399.18	8.8970	3.5524	98.839%
4.0985	399.17	10.1410	4.0490	98.794%

3.6 Functional Waveforms

3.6.1 Test Under 90 VAC, 800-Ω Load

Figure 3-7 shows the waveform under 90 VAC, 800-Ω load at DC output. Channel 2 is the AC input voltage, channel 3 is the DC output voltage, Channel 4 is the AC input current (same scope channels configure hereinafter unless specified). Since input voltage is less than 170 V, PFC does not start.

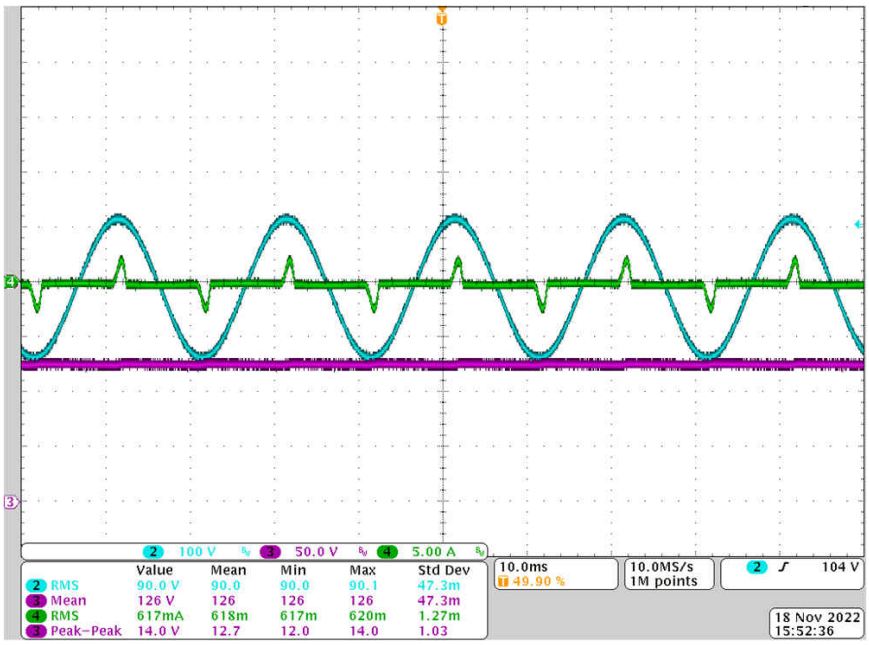


Figure 3-7. Waveform Under 90 VAC, 800-Ω Load

3.6.2 Power-On Sequence Test Under 220 VAC

Figure 3-8 shows the power-on sequence under 220 VAC. Power on starts from the PTC inrush current limit step, then the relay engages. PFC starts softly at the last step.

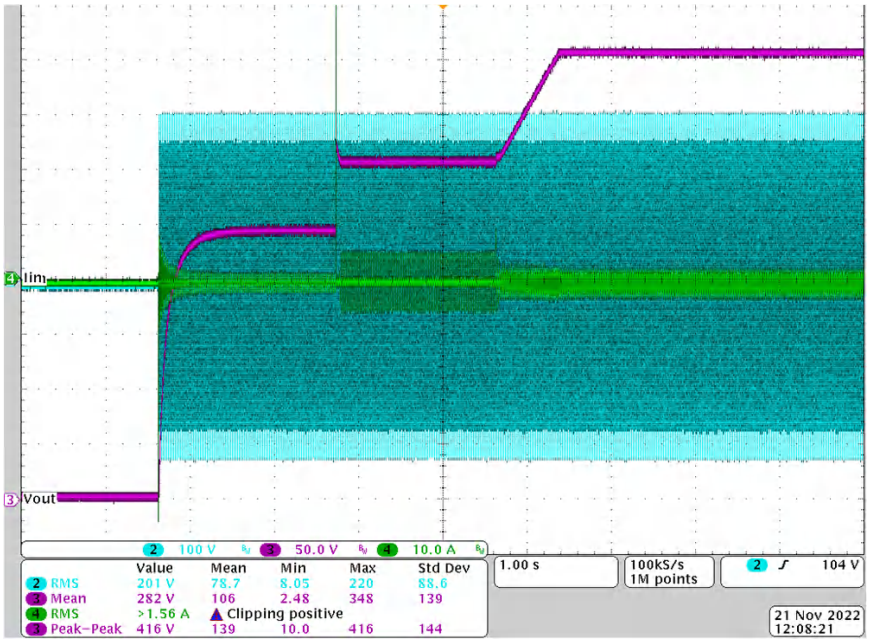


Figure 3-8. Power-On Sequence Under 220-VAC Input

3.6.3 Waveform With Heavy Load

Figure 3-9 shows the waveform with 2-kW load under 220-VAC input.

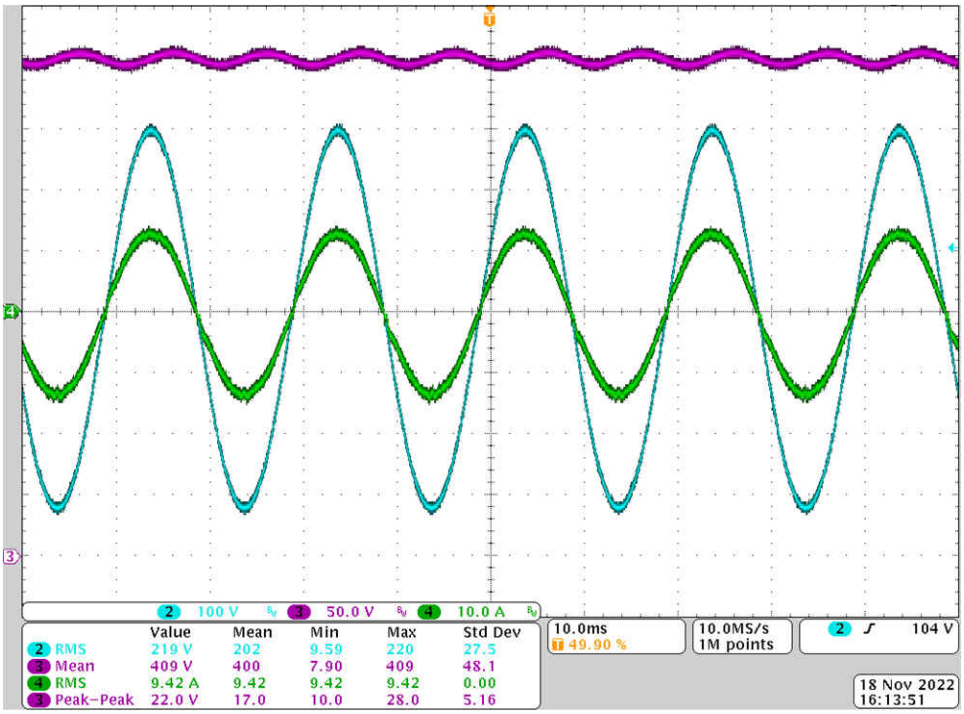


Figure 3-9. Waveform Under 220 VAC, 2 kW

Figure 3-10 shows the waveform with 4-kW load under 220-VAC input.

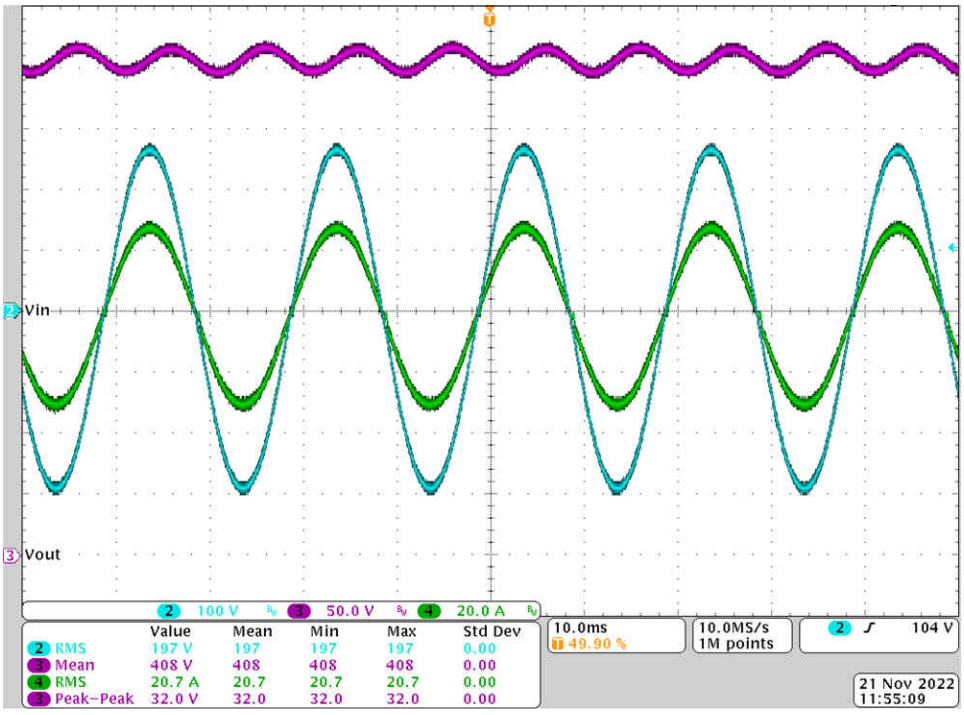


Figure 3-10. Waveform Under 220 VAC, 4 kW

3.6.4 Buck Auxiliary Power Supply Tests

Figure 3-11 shows buck power supply waveforms. Channel 1 is 15-V voltage rail, channel 3 is the switching node at pin 4 of UCC28710.

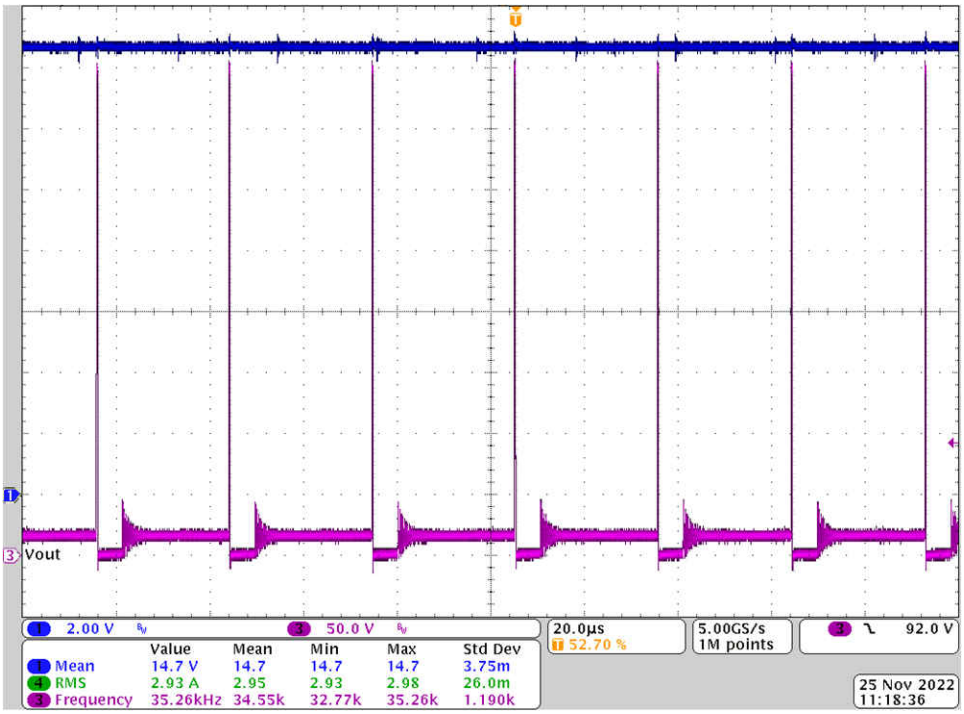


Figure 3-11. Buck Power-Supply Waveforms

Figure 3-12 shows the buck inductor temperature rising at 15 V, 400 mA.

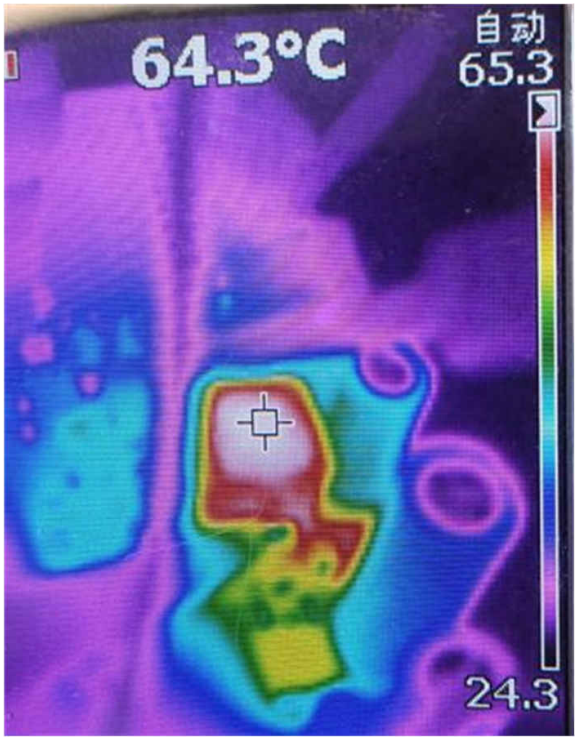


Figure 3-12. Temperature Rising of Buck Inductor L8

3.6.5 AC Drop Test

Figure 3-13 shows the AC drop at 90°, 10-ms duration, after AC voltage recover. PLL still needs time to be in the same phase with AC input, so there is an inrush current since the DC bus voltage drops a lot and PLL is out of phase, then cycle-by-cycle current protection starts to work at this time to protect GaN from overcurrent (40 A in this design).

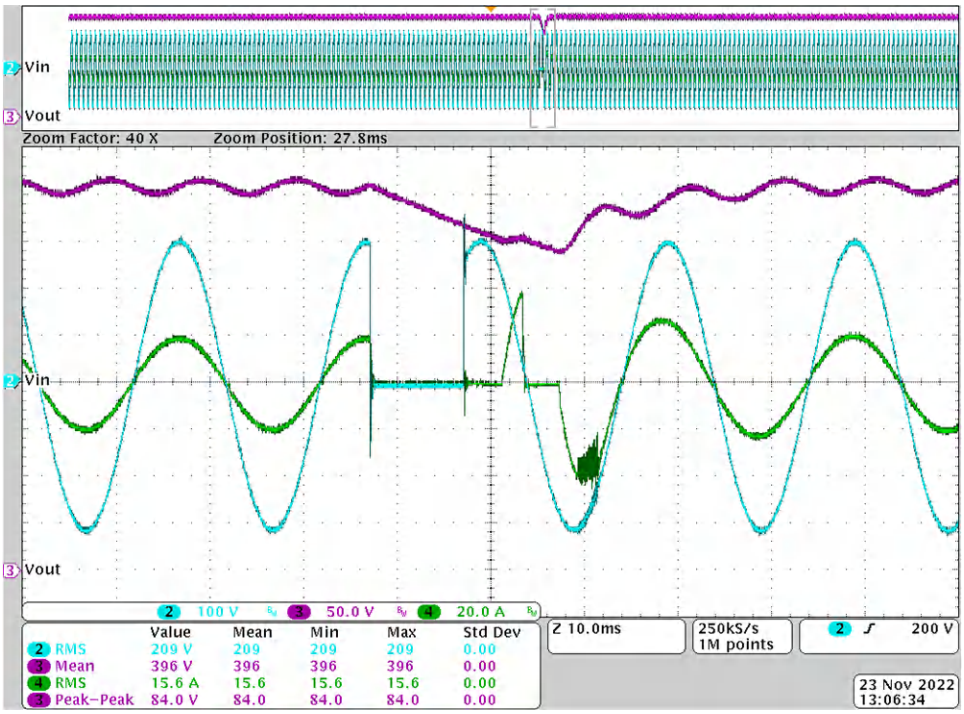


Figure 3-13. AC Drop at 90°, 10-ms Duration

Figure 3-14 shows the AC drop at 45°, 10-ms duration. Cycle-by-cycle current protection also works.

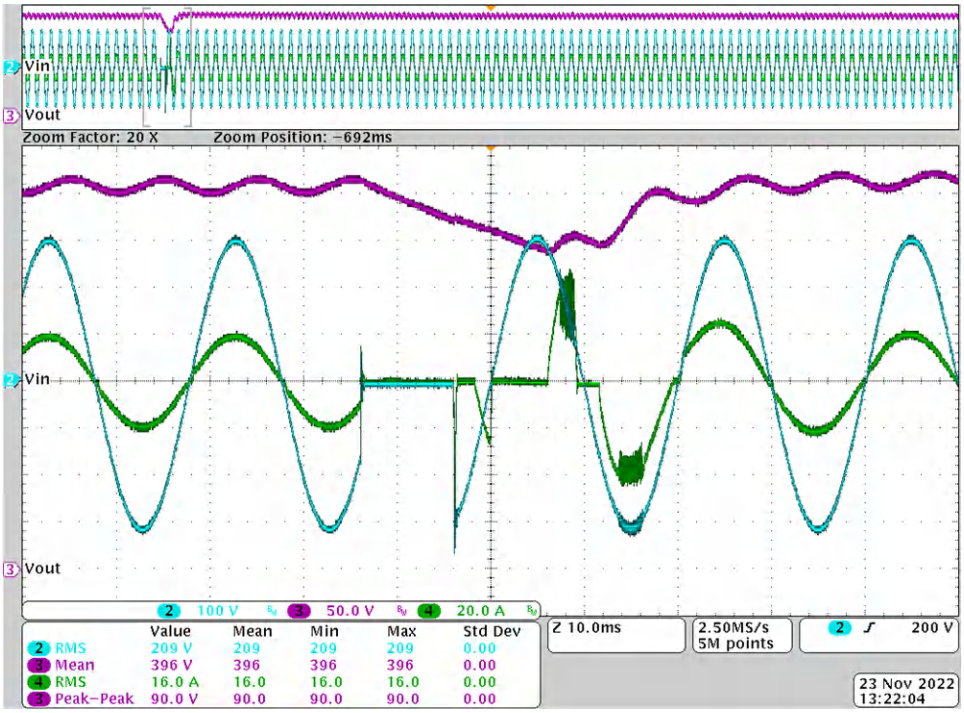


Figure 3-14. AC Drop at 45°, 10-ms Duration

3.6.6 GaN Switching Performance

Figure 3-15 shows GaN rising edge under 400 VDC, 2.5-kW load.

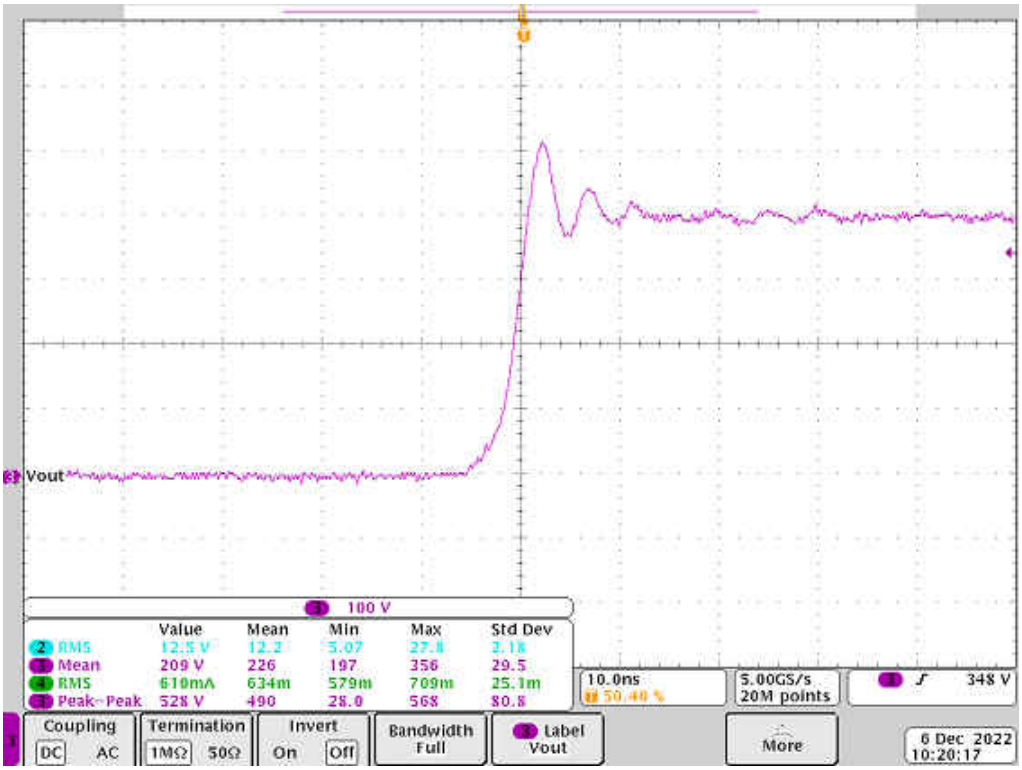


Figure 3-15. VDS, GaN Rising Edge Under 2.5-kW Load

Figure 3-16 shows GaN falling edge under 400 VDC, 2.5-kW load.

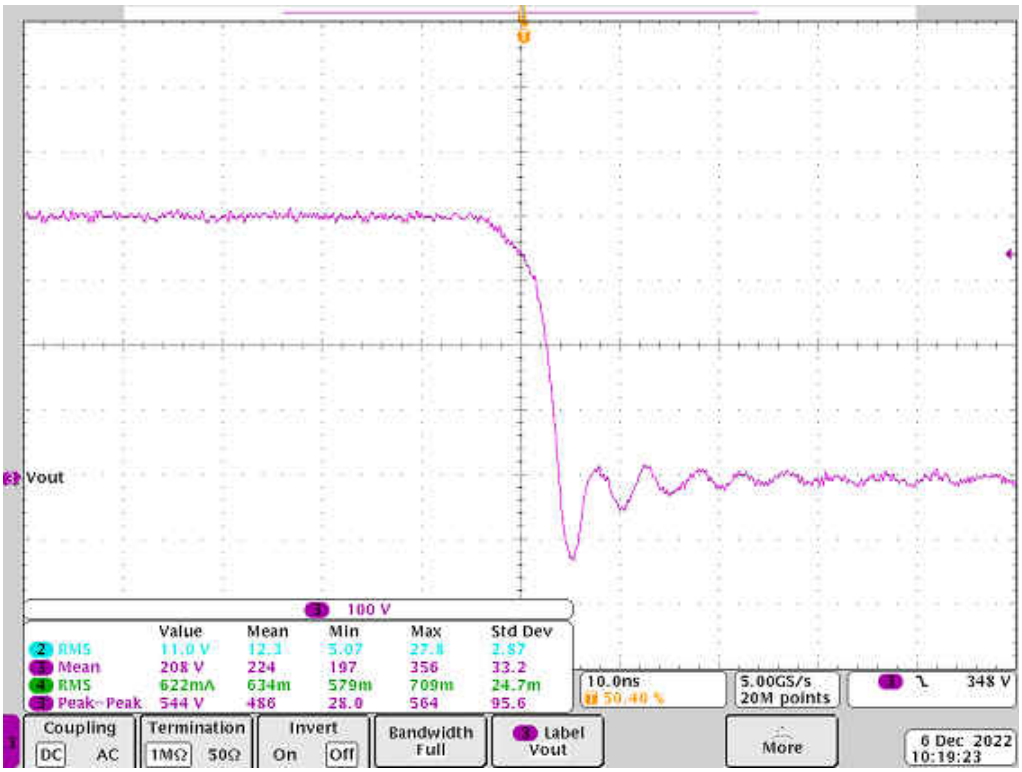


Figure 3-16. VDS, GaN Falling Edge Under 2.5-kW Load

3.6.7 Thermal Test

Thermal performance is validated in this design. The conditions are as shown in the following list:

- 200 VAC with 4-kW load
- Cooling fan: 27CFM, 24 V, 2.64 W
- Thermal balanced after 15 minutes
- Ambient temperature is 25°C

Figure 3-17 shows the test setup for the temperature rising test.

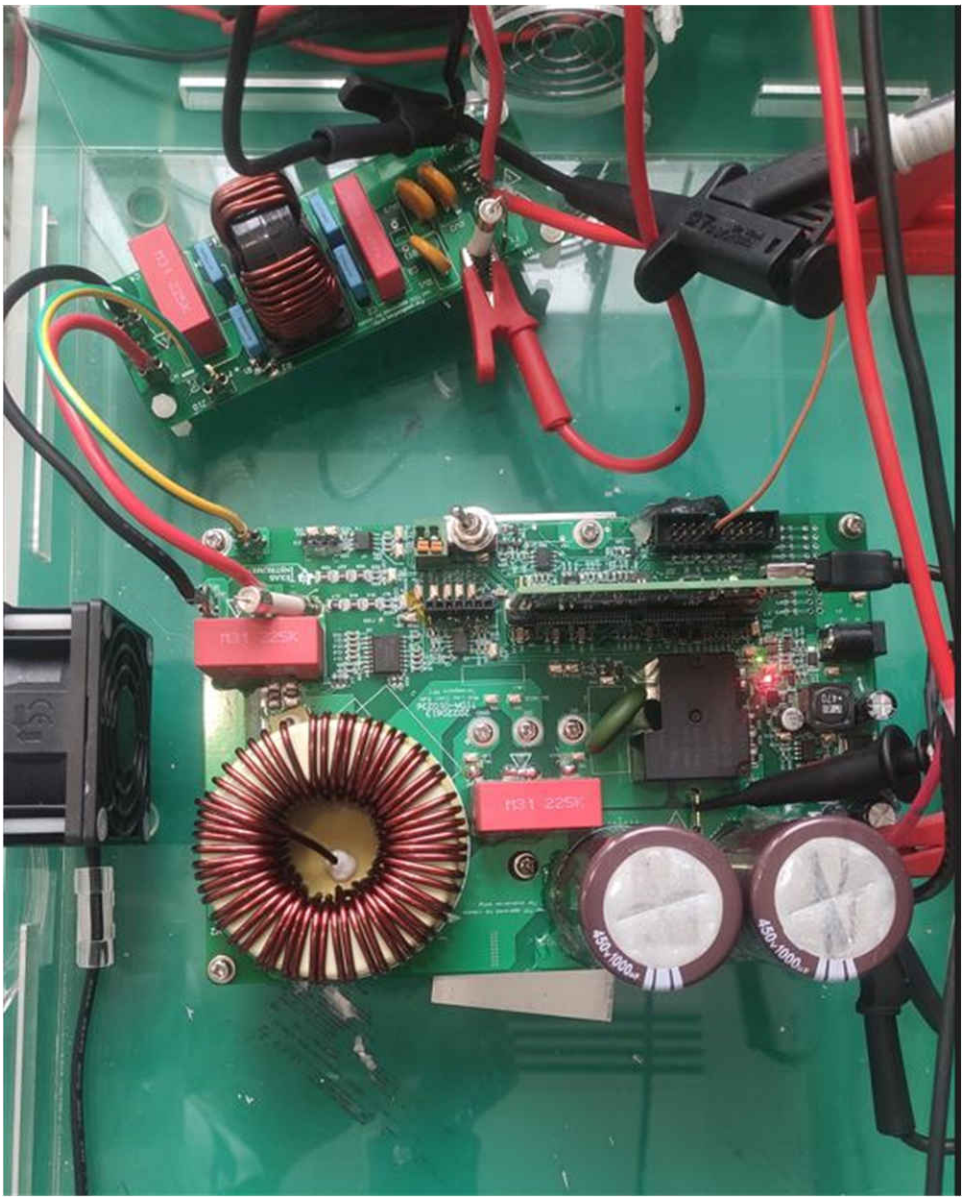


Figure 3-17. Thermal Test setup

Figure 3-18 shows boost inductor temperature at 200 VAC, 4 kW, temperature rising is 69.6°C – 25°C = 44.6°C.

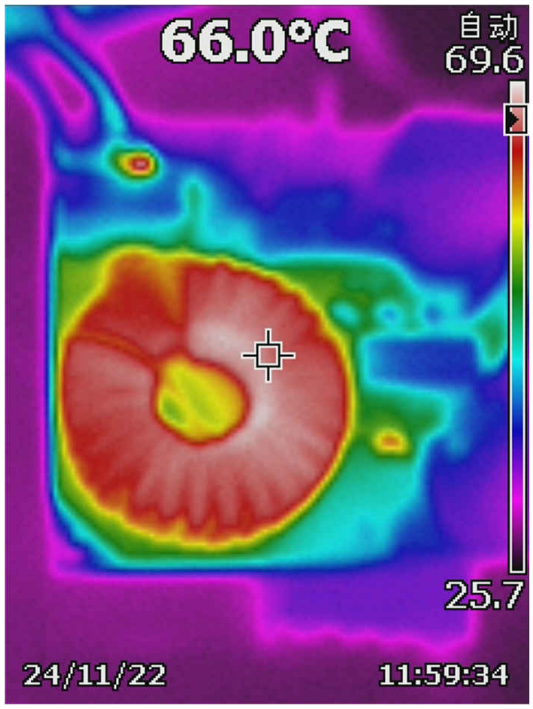


Figure 3-18. Boost Inductor Temperature

Since the GaN daughterboard is underneath the main board, measuring the GaN temperature rising with a thermal imager is difficult. However, GaN reports the temperature at the TEMP pin in PWM mode, and the PWM duty ratio represents temperature. Firmware monitors the PWM duty ratio, and calculates temperature, and reports this information to the host PC through the UART port. Figure 3-19 is the heartbeat report on the UART terminal. The temperature of GaN can be read in the report.

For some applications with even lower AC input voltage, the input current is higher, so temperature rising of GaN, diode bridge, and boost inductor is even higher. Users must fully evaluate temperature rising of those devices, to make sure the devices have enough temperature rising margin.

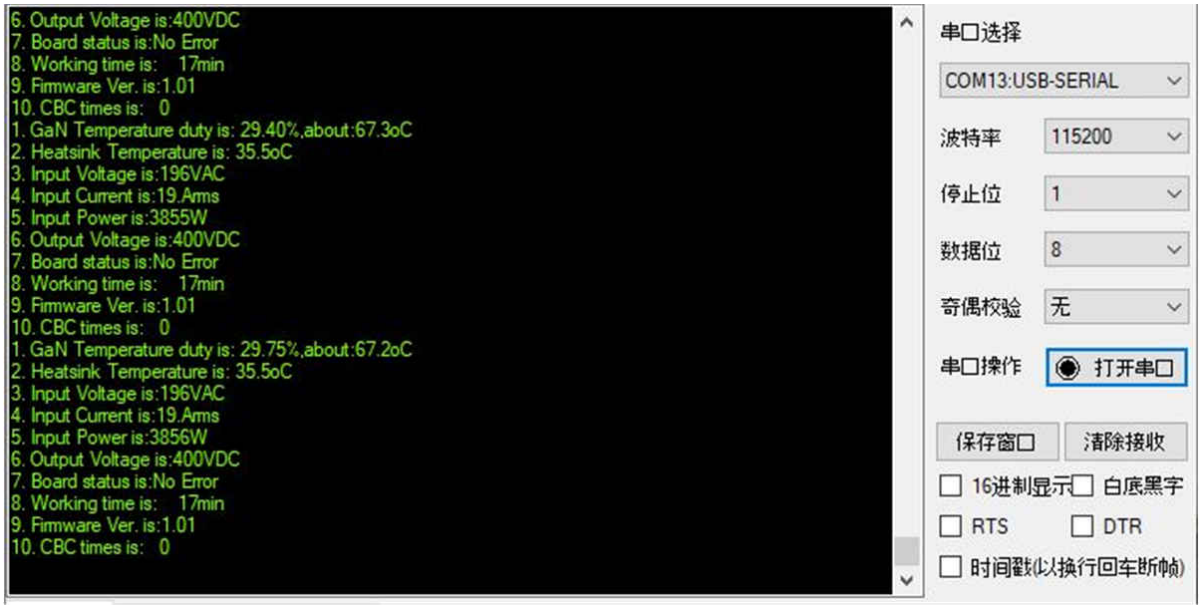


Figure 3-19. GaN Temperature Rising on Heartbeat Report

3.6.8 Power-Off Sequence

Figure 3-20 shows power-off waveform at 200 VAC, 4 kW.

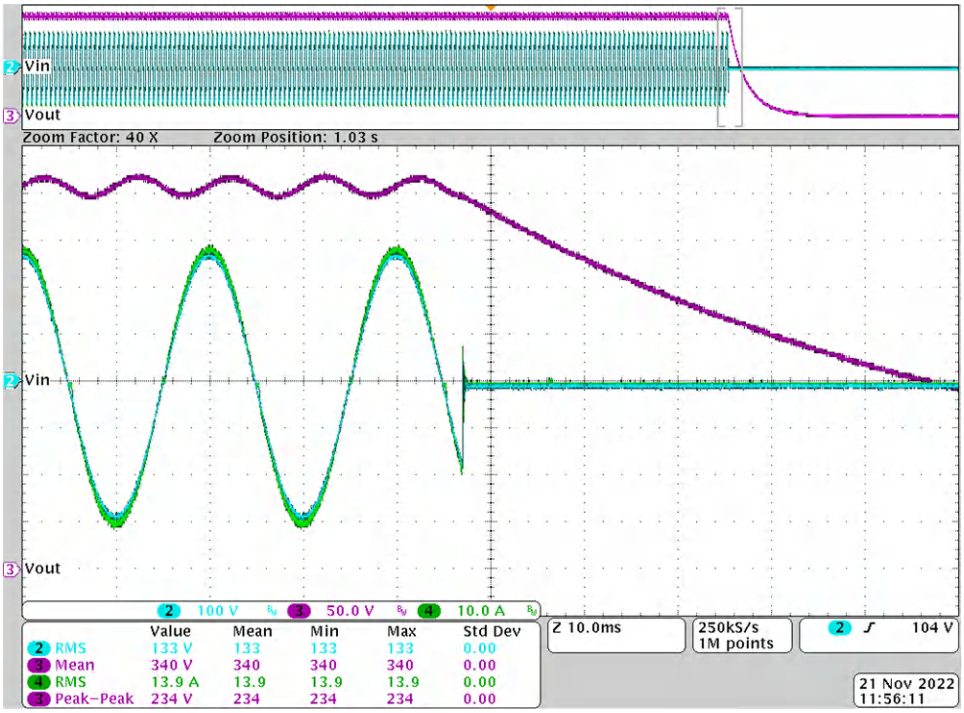


Figure 3-20. Power-Off Waveform

3.6.9 Surge Test

A lighting surge test between *line* and *neutral* was evaluated. The design can survive a 4-kV surge test. A surge causes a one-shot-trigger interrupt, if the firmware stops PFC at OST interrupt, the surge test is Grade C since PFC stops and does not start automatically. If firmware does not stop PFC at OST interrupt, PFC keeps working, and the surge test result is Grade A. Figure 3-21 shows the 4-kV line to neutral surge voltage waveform.

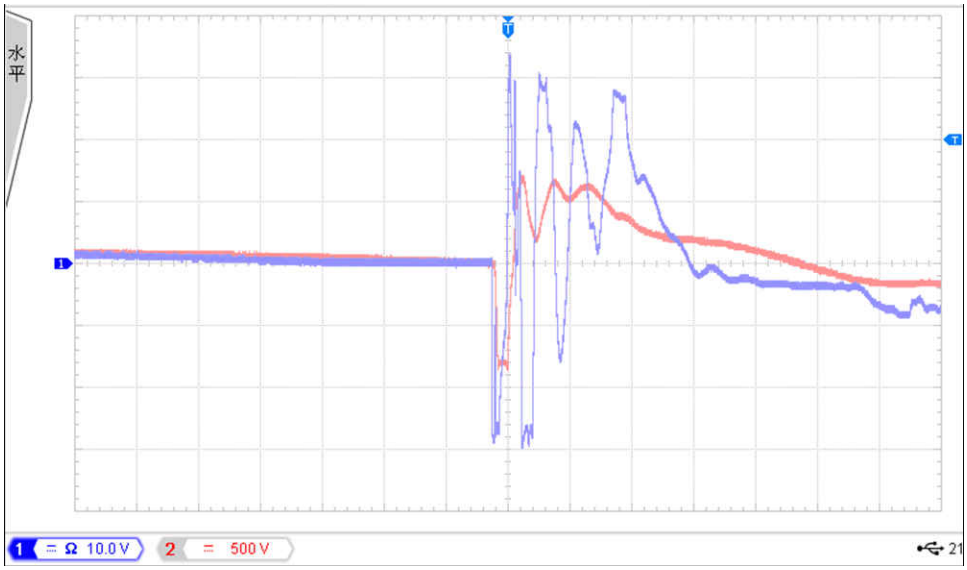


Figure 3-21. Surge Test Under 4 kV

3.6.10 Conducted Emission Test

Figure 3-22 shows the conducted Emission test result with a 1.6-kw load. The board was tested with an additional CM choke at DC output (to overcome a long load cable and a large resistor load), and a shield layer for the boost inductor. The result shows the board can pass the Class B limit of EN55032. Noise level at 11.42 MHz is 59.17 (54.17 dBµV+5 dBµV of calibration), margin is a little small as usually 6 dB is needed; however, housing (the outdoor unit of air conditioner usually has a metal housing) and a short load cable further reduces noise to Line Impedance Stabilization Network (LISN), and gives much more margin.

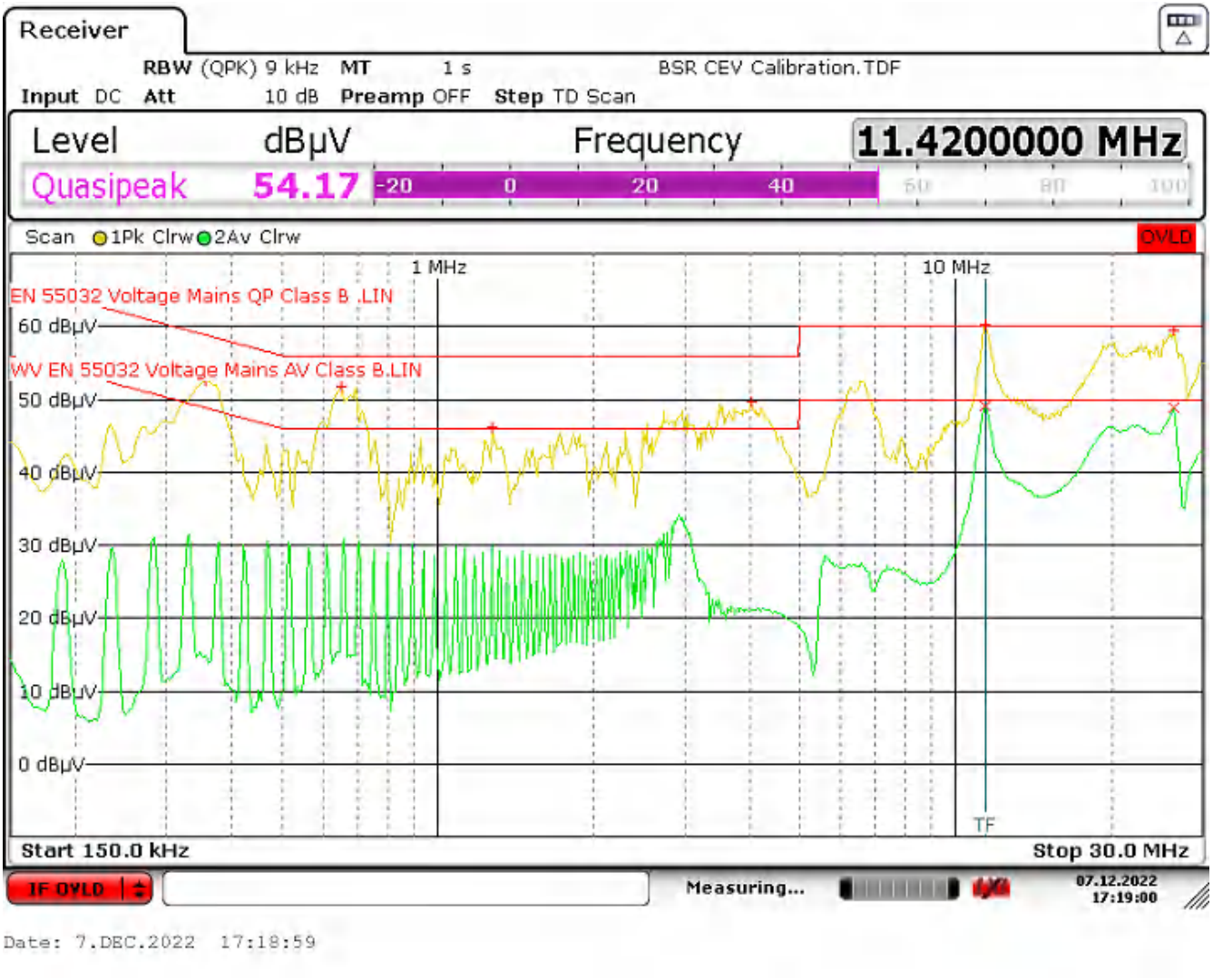


Figure 3-22. Conducted Emission Test, EN55032 Class B

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010236.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010236.

4.2 Documentation Support

1. Texas Instruments, *LMG352xR030-Q1 650-V 30-mΩ GaN FET with Integrated Driver, Protection, and Temperature Reporting* data sheet
2. Texas Instruments, *TMS320F28002x Real-Time Microcontrollers* data sheet
3. Texas Instruments, *AMC3302 High-Precision, ±50-mV Input,Reinforced Isolated Amplifier With Integrated DC/DC Converter* data sheet
4. Texas Instruments, *UCC2871x Constant-Voltage, Constant-Current Controller With Primary-Side Regulation* data sheet
5. Texas Instruments, *UCC2871x Constant-Voltage, Constant-Current Controller With Primary-Side Regulation* data sheet
6. Texas Instruments, *ISO772x High-Speed, Robust EMC, Reinforced and Basic Dual-Channel Digital Isolators* data sheet

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

HELY ZHANG is a System Application Engineer at Texas Instruments, where he is responsible for developing home appliance related power delivery and motor inverters. Hely earned his masters degree from Anhui University of Science and Technology with Power electronics in 2002, and worked in SolarEdge and General Electric before joining TI.

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