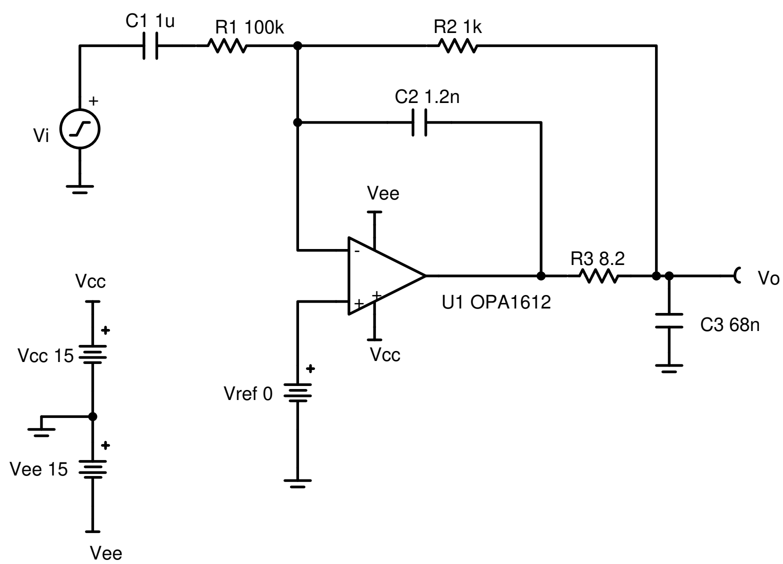
Band Pass Filtered Inverting Attenuator Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
100 mV_{pp}	50 V_{pp}	1m V_{pp}	500 mV_{pp}	15 V	–15 V	0 V

Design Description

This tunable band-pass attenuator reduces signal level by –40 dB over the frequency range from 10 Hz to 100 kHz. It also allows for independent control of the DC output level. For this design, the pole frequencies were selected outside the pass band to minimize attenuation within the specified bandwidth range.



Design Notes

1. If a DC voltage is applied to V_{ref} be sure to check common mode limitations.
2. Keep R_3 as small as possible to avoid loading issues while maintaining stability.
3. Keep the frequency of the second pole in the low-pass filter (f_{p3}) at least twice the frequency of the first low-pass filter pole (f_{p2}).

Design Steps

1. Set the passband gain.

$$\text{Gain} = -\frac{R_2}{R_1} = -0.01\ \frac{V}{V}\left(-40\text{dB}\right)$$

$$R_1 = 100\text{k}\Omega$$

$$R_2 = 0.01 \times R_1 = 1\ \text{k}\Omega$$

2. Set high-pass filter pole frequency (f_{p1}) below f_l.

$$f_l = 10\text{Hz}, f_{p1} = 2.5\ \text{Hz}$$

3. Set low-pass filter pole frequency (f_{p2} and f_{p3}) above f_h.

$$f_h = 100\text{kHz}$$

$$f_{p2} = 150\text{kHz}$$

$$f_{p3} \geq 2 \times f_{p2} = 300\text{kHz}$$

$$f_{p3} = 300\text{kHz}$$

4. Calculate C_1 to set the location of f_{p1}.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_{p1}} = \frac{1}{2\pi \times 100\text{k}\Omega \times 2.5\text{Hz}} = 0.636\ \mu\text{F} \approx 1\ \ \mu\text{F (Standard Value)}$$

5. Select components to set f_{p2} and f_{p3}.

$$R_3 = 8.2\Omega\ \text{(provides stability for cap loads up to 100nF)}$$

$$C_2 = \frac{1}{2\pi \times \left(R_2 + R_3\right) \times f_{p2}} = \frac{1}{2\pi \times 1008.2\Omega \times 150\text{kHz}}$$
$$= 1052\text{pF} \approx 1200\text{pF (Standard Value)}$$

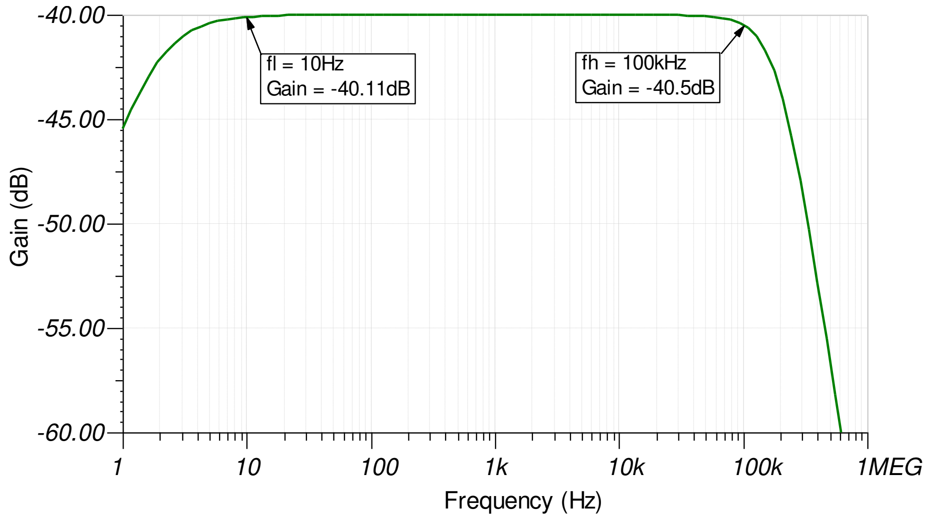
$$C_3 = \frac{1}{2\pi \times R_3 \times f_{p3}} = \frac{1}{2\pi \times 8.2\Omega \times 300\text{kHz}} = 64.7\ \text{nF} \approx 68\text{nF (Standard Value)}$$

Design Simulations

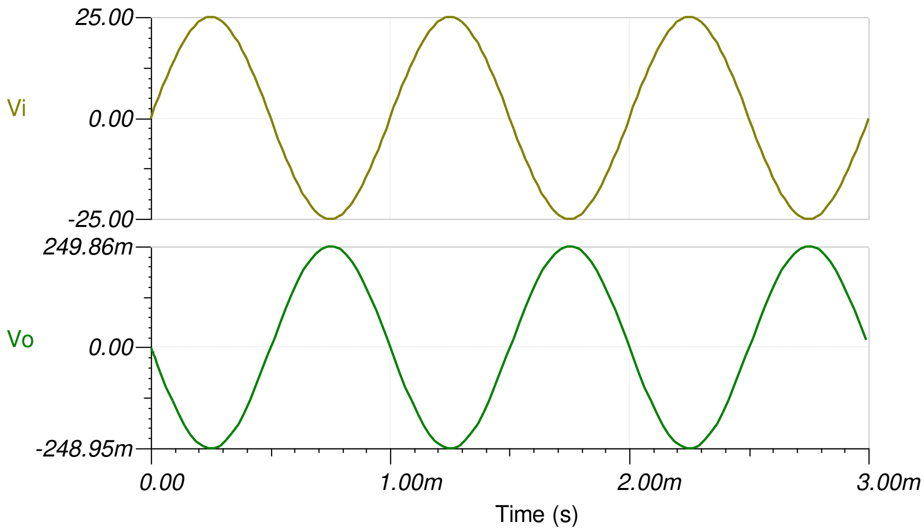
DC Simulation Results

The amplifier will pass DC voltages applied to the noninverting pin up to the common mode limitations of the op amp (±13 V in this design)

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC503.

See TIPD118.

Design Featured Op Amp

OPA1612	
V_{ss}	4.5 V to 36 V
V_{inCM}	V_{ee}+2 V to V_{cc}–2 V
V_{out}	V_{ee}+0.2 V to V_{cc}–0.2 V
V_{os}	100 µV
I_q	3.6 mA/Ch
I_b	60 nA
UGBW	40 MHz
SR	27 V/µs
#Channels	1 and 2
OPA1612	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5 V to 36 V
V_{inCM}	V_{ee}–100 mV to V_{cc}–2 V
V_{out}	Rail-to-rail
V_{os}	200 µV
I_q	1.6 mA/Ch
I_b	8 pA
UGBW	10 MHz
SR	10 V/µs
#Channels	1, 2, and 4
OPA172	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from July 31, 2017 to February 1, 2019	**Page**
• Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.............	1