Analog Engineer's Circuit

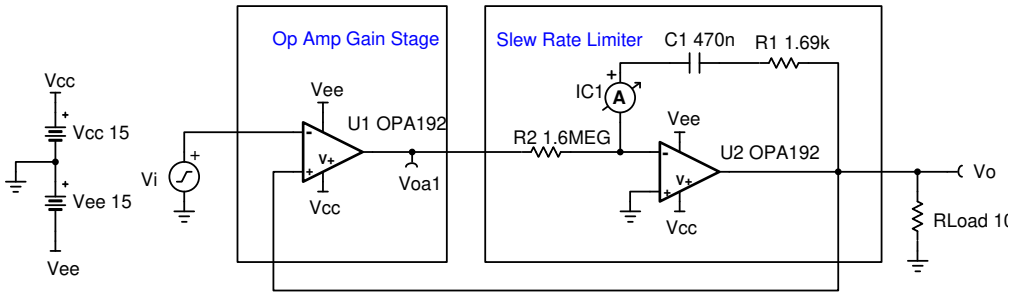
Slew Rate Limiter Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–10 V	10 V	–10 V	10 V	15 V	–15 V	0 V

Design Description

This circuit controls the slew rate of an analog gain stage. This circuit is intended for symmetrical slew rate applications. The desired slew rate must be slower than that of the op amp chosen to implement the slew rate limiter.



Design Notes

1. The gain stage op-amp and slew rate limiting op amp should both be checked for stability.
2. Verify that the current demands for charging or discharging C_1 plus any load current out of U_2 will not limit the voltage swing of U_2.

Design Steps

1. Set slew rate and choose a standard value for the feedback capacitor, C_1.

$$C_1 = 470\text{nF}$$

$$SR = 20\frac{V}{s}$$

2. Choose the value of R_2 to set the capacitor current necessary for the desired slew rate.

$$SR = \frac{I_{C_1}}{C_1}$$

$$20\frac{V}{s} = \frac{I_{C_1}}{470\text{nF}} \text{ where } I_{C_1} = 9.4\ \mu A$$

$$\text{Gain stage op amp } V_{sat} = \pm 14.995 \text{ (typical)}$$

$$I_{C_1} = \frac{V_{sat}}{R_2}$$

$$9.4\ \mu A = \frac{14.995V}{R_2}, \text{ so } R_2 = 1.595\ M\Omega \approx 1.6M\Omega \text{ (Standard Value)}$$

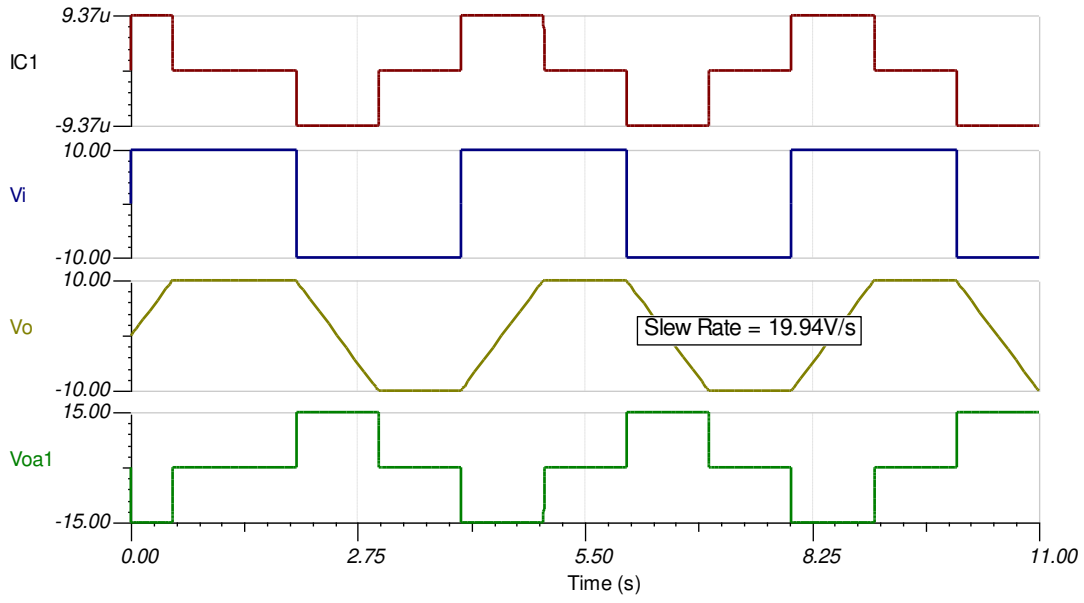
3. Compensate feedback network for stability. R_1 adds a pole to the 1/β network. This pole should be placed so that the 1/β curve levels off a decade before it intersects the open loop gain curve (200 Hz, for this example).

$$f_p = \frac{1}{2\pi \times R_1 \times C_1} = 200\text{Hz}$$

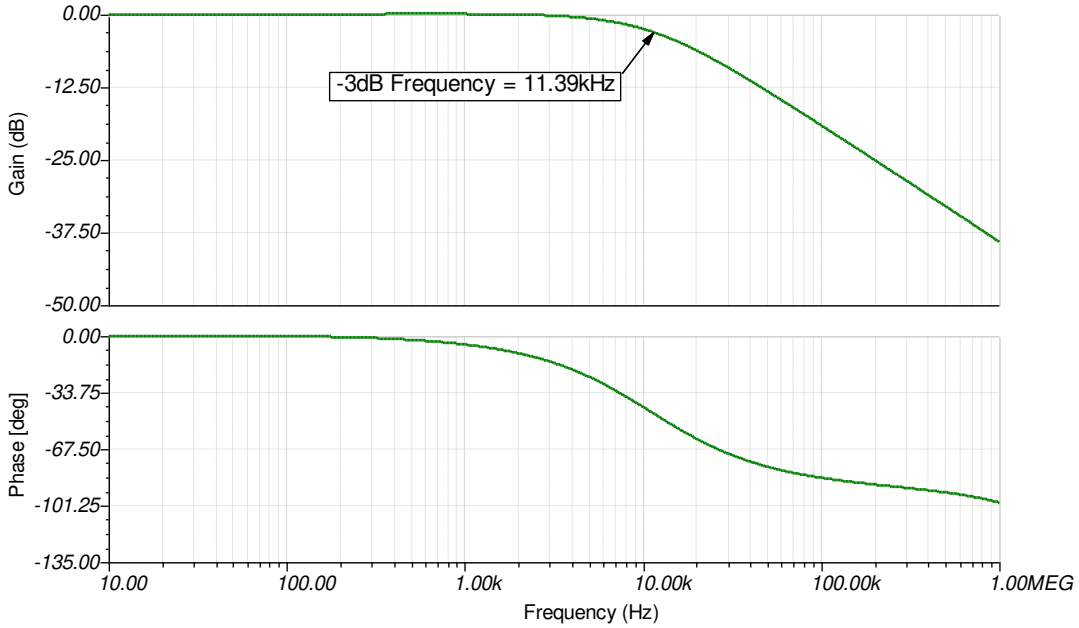
$$200\text{Hz} = \frac{1}{2\pi \times R_1 \times 470\text{nF}}, \text{ so } R_1 = 1.693\ k\Omega \approx 1.69k\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC508.

See TIPD140.

Design Featured Op Amp

OPA192	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA192	

Design Alternate Op Amp

TLV2372	
V_{cc}	2.7 V to 16 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2 mV
I_q	750 µA/Ch
I_b	1 pA
UGBW	3 MHz
SR	2.1 V/µs
#Channels	1, 2, and 4
TLV2372	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file	1

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