Analog Engineer's Circuit

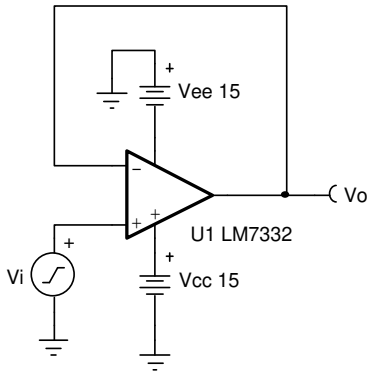
Buffer (Follower) Circuit

Design Goals

Input		Output		Freq.	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
–10 V	10 V	–10 V	10 V	100 kHz	15 V	–15 V

Design Description

This design is used to buffer signals by presenting a high input impedance and a low output impedance. This circuit is commonly used to drive low-impedance loads, analog-to-digital converters (ADC) and buffer reference voltages. The output voltage of this circuit is equal to the input voltage.



Design Notes

1. Use the op-amp linear output operating range, which is usually specified under the A_{OL} test conditions.
2. The small-signal bandwidth is determined by the unity-gain bandwidth of the amplifier.
3. Check the maximum output voltage swing versus frequency graph in the data sheet to minimize slew-induced distortion.
4. The common mode voltage is equal to the input signal.
5. Do not place capacitive loads directly on the output that are greater than the values recommended in the data sheet.
6. High output current amplifiers may be required if driving low impedance loads.
7. For more information on op-amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the *Design References* section.

Design Steps

The transfer function for this circuit follows:

$$V_o = V_i$$

1. Verify that the amplifier can achieve the desired output swing using the supply voltages provided. Use the output swing stated in the A_{OL} test conditions. The output swing range of the amplifier must be greater than the output swing required for the design.

   $$-14V \le V_o \le 14V$$

   - The output swing of the LM7332 using ±15 V supplies is greater than the required output swing of the design. Therefore, this requirement is met.
   - Review the Output Voltage versus Output Current curves in the product data sheet to verify the desired output voltage can be achieved for the desired output current.
2. Verify the input common mode voltage of the amplifier will not be violated using the supply voltage provided. The input common mode voltage range of the amplifier must be greater than the input signal voltage range.

   $$-15.1\ \ V \le V_{icm} \le 15.1\ \ V$$

   - The input common-mode range of the LM7332 using ±15 V supplies is greater than the required input common-mode range of the design. Therefore, this requirement is met.
3. Calculate the minimum slew rate required to minimize slew-induced distortion.

   $$SR > 2 \times \pi \times Vp \times f = 2 \times \pi \times 10V \times 100kHz = 6.28V/\mu s$$

   - The slew rate of the LM7332 is 15.2 V/µs. Therefore, this requirement is met.
4. Verify the device will have sufficient bandwidth for the desired output signal frequency.

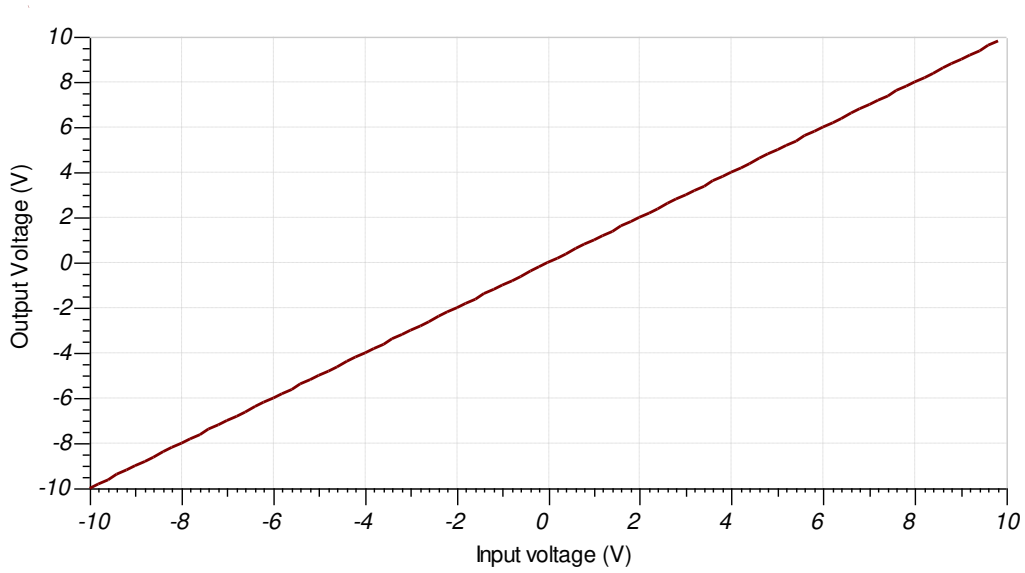
   $$f_{signal} < f_{unity}$$

   $$100kHz\ \ < 7.5MHz$$

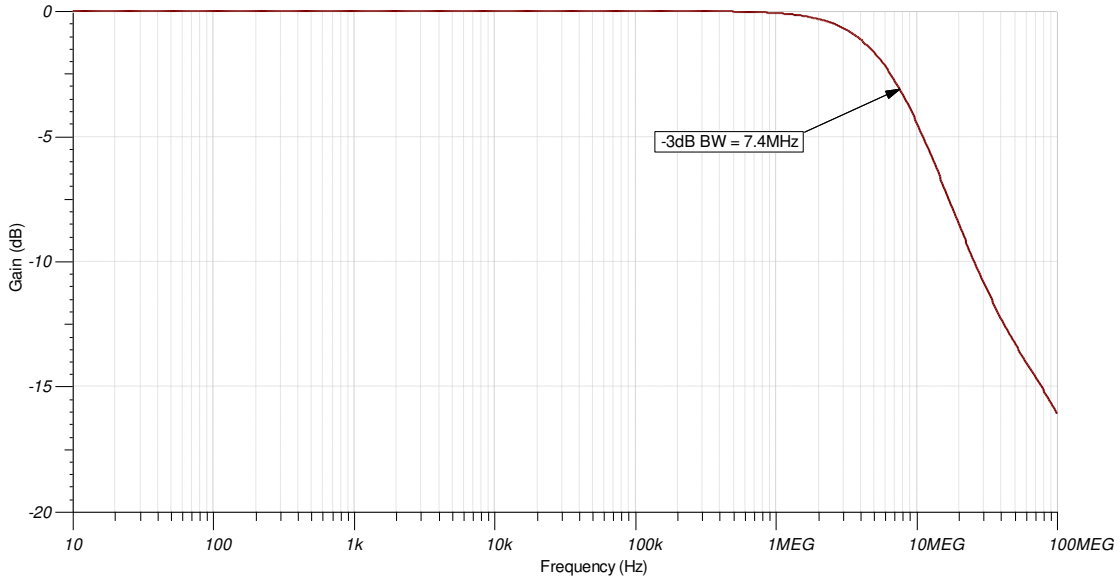
   - The desired output signal frequency is less than the unity-gain bandwidth of the LM7332. Therefore, this requirement is met.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

For more information, see the *Capacitive Load Drive Verified Reference Design Using an Isolation Resistor* TI Design.

See the circuit SPICE simulation file SBOC491.

For more information on many op amp topics including common-mode range, output swing, bandwidth, slew rate, and how to drive an ADC, see *TI Precision Labs*.

Design Featured Op Amp

LM7332	
V_{ss}	2.5 V to 32 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.6 mV
I_q	2 mA
I_b	1 µA
UGBW	7.5 MHz (±5 V supply)
SR	15.2 V/µs
#Channels	2
LM7332	

Design Alternate Op Amp

OPA192	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	1 mA
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA192	

The following device is for battery-operated or power-conscious designs outside of the original design goals described earlier, where lowering the total system power is desired.

LPV511	
V_{ss}	2.7 V to 12 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.2 mV
I_q	1.2 µA
I_b	0.8 nA
UGBW	27 KHz
SR	7.5 V/ms
#Channels	1
LPV511	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 14, 2019 **Page**

- Downscale title. Added LPV511 table in the *Design Alternate Op Amp* section.....1

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