Analog Engineer's Circuit

Closed-Loop TEC Control Circuit Using a Voltage-Output Smart AFE and DC/DC Converter

Nathan Ayres, Illia Volkov

Data Converters

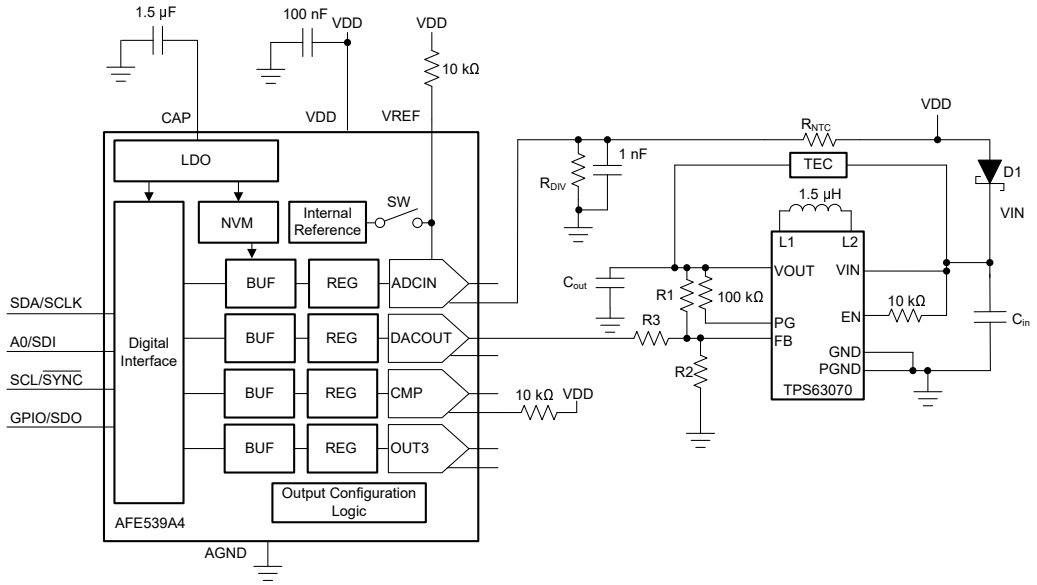
Design Goals

Key Input Parameter	Key Output Signal	Recommended Device
Temperature measured through NTC thermistor by ADC input	Voltage output from DC/DC converter, 2.5 V to 9 V	AFE539A4

Objective: Design a closed-loop system controlled by a smart AFE to control the temperature of a TEC by modifying the power output of a buck-boost converter.

Design Description

This design uses the AFE539A4, smart analog front end (AFE) with an integrated state machine and analog-to-digital converter (ADC) to control a thermoelectric cooler (TEC) with a buck-boost (DC/DC) converter. A TEC is a resistive element and is current controlled. The temperature of the TEC element is altered by the magnitude and direction of the current. The TEC element is connected across the VIN and VOUT pins of the DC/DC converter, and the temperature of the element changes as the voltage on the VOUT pin of the DC/DC converter is modified. A resistive network of three resistors is connected to the VFB pin of the DC/DC and the VOUT pin of the AFE539A4 to modify the output voltage of the DC/DC converter. The voltage drop across the TEC element changes as the voltage at the VOUT pin of the buck-boost converter changes, which allows current to flow through the resistive TEC element. The integrated state machine on the AFE539A4 is configured as a proportional-integral (PI) controller that senses the temperature with the internal ADC and adjusts the DAC output to maintain the desired temperature on the load being heated or cooled by the TEC element. This circuit can be used in automotive cooling, portable refrigeration, laser diode cooling, and electronics component cooling.



TEC DC/DC Control Diagram

Design Notes

Device Selection

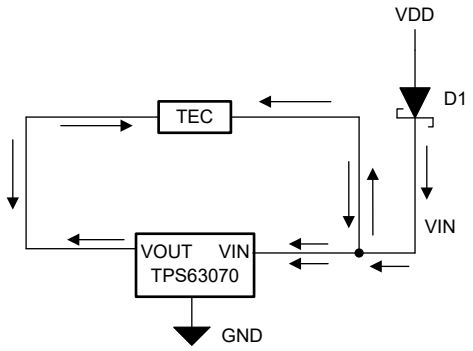
The AFE539A4 is capable of controlling DC/DC converters: for this reference design the TPS63070 buck-boost converter is selected. The TPS63070 has an input voltage range of 2 V to 16 V and an output range of 2.5 V to 9 V with the ability to drive up to 2 A of current.

General Overview

The *AFE539A4 Smart Analog Front End (AFE) With Quad-Channel, 10-Bit DAC and ADC for Proportional-Integral (PI) Control With I2C and SPI* data sheet recommends using a 100-nF decoupling capacitor for the VDD pin, and a 1.5 µF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal low-dropout (LDO) linear regulator. Place these capacitors close to the device pins.

Due to the bidirectional current flow in a TEC module, a diode can be connected between the TPS VIN pin and the supply to protect the supply from any back-current flow. TEC Control DC/DC Protection Diode Diagram shows the flow of current with the red arrows representing the current flow from the supply, and the blue arrows representing the reverse current which can be harmful to the supply. This diode can be ignored if current sinking to the source is not a concern.

Diodes exhibit a turn-on voltage that needs to be accounted for. The voltage supply must be offset by the diode turn-on voltage, which in the case of this design is 500 mV. Conversely, the nominal output of the TPS63070 can be set to 4.5 V instead of raising the supply voltage. Regardless of which voltage is offset, track any changes that can affect the calculations of the biasing resistor network (R1, R2, R3). The diode is bypassed in this design and the 500-mV offset is ignored for resistors calculations.



TEC Control DC/DC Protection Diode Diagram

The comparator input (pin FB2) on the AFE539A4 can be used along with a current-sense amplifier for overcurrent detection. Connect the comparator input to VDD or to GND when the comparator is not in use. This design does not use the comparator and the input is connected to VDD. Register SRAM-DATA-36 sets the comparator threshold and SRAM-DATA-39 sets the safe output setting.

The pin FB2 on the TPS63070 is used for scaling the voltage output. Typically, this pin has a resistor connected between pins FB2 and FB on the TPS63070 to change the voltage-divider ratio on the FB pin to control the output voltage. The FB2 pin is not used for this configuration and is grounded. The TPS63070 PG pin is an open-drain, power-good output. A 100-kΩ resistor is recommended for the PG pin.

Nominal Value Selection

The voltage across the TEC is bipolar, where the polarities are used to describe the direction of the current flow. The VOUT pin of the DC/DC converter is set to operate in the range of 2.5 V to 7.5 V, where 2.5 V yields negative voltage across TEC and 7.5 V yields positive voltage.

The positive voltage of the TPS63070 is calculated by the difference between the VOUT maximum (7.5 V) and the input voltage, VIN (5 V). Similarly, the negative voltage is calculated by the difference between the minimum VOUT (2.5 V) and VIN. These voltage values are selected to create a 500-mA current with the resistive TEC element.

Resistor Network Design

The resistive network is designed to set a margin on the VOUT pin of the DC/DC converter to three different desired output voltages.

- Case 1: VDAC = 0, VOUT is set to output maximum voltage (VHIGH), which is 7.5 V
- Case 2: VDAC = 800 mV = VNOMINAL, VOUT is set to 5 V
- Case 3: VDAC is set to maximum value, VOUT is set to minimum voltage (VMIN), which is 2.5 V

Using a nominal current of 5 µA, the following equations are used to determine the resistor values to produce the respective voltage output. Set the nominal current for the resistor to be significantly larger than the 100-nA leakage current on the FB pin of the TPS63070.

$$R_1 = \frac{V_{NOMINAL} - V_{FB}}{I_{NOMINAL}} = 840\ k\Omega$$

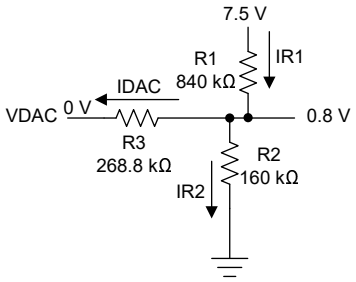
$$R_2 = \frac{R_1 \times V_{FB}}{V_{NOMINAL} - V_{FB}} = 160\ k\Omega$$

$$R3 = \frac{V_{FB} - V_{DAC}}{I_{R1}}$$

To calculate the value for R3, the current through R1 must first be obtained. This equation demonstrates how to calculate the current through R1 using Case 1, where VDAC = 0 V and VOUT = 7.5 V.

$$I_{R1} = \frac{V_{OUT} - V_{FB}}{R1} = \frac{6.7\ V}{840\ k\Omega} = 7.98\ \mu A.$$

The following figure illustrates the flow of current across resistors R1 and R2, as well as the flow of current towards the DAC.



TEC Control DC/DC Resistor Divider Calculation Using Case 1

The current through R1 is the total current between the branches of R2 and R3, which is calculated using Ohm's law. For this case, the DAC has a 0-V output.

$$R3 = \frac{V_{FB} - V_{DAC}}{I_{R1}} = \frac{0.8\ V - 0\ V}{2.98\ \mu A} = 268.8\ k\Omega.$$

The 5-V nominal voltage of the TPS63070 is the same as VIN, so there is zero current through the TEC. With no voltage drop, there is no temperature change in the TEC due to the lack of current. The following resistor values are derived with a nominal voltage of 5 V, nominal current of 5 µA, and a feedback voltage of 800 mV.

$$R_1 = \frac{5\ V - 0.8\ V}{5\ \mu A} = 840\ k\Omega$$

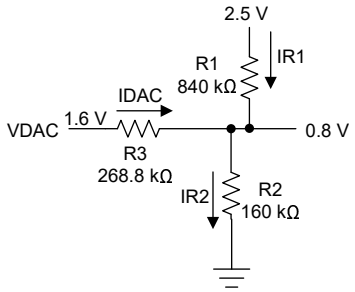
$$R_2 = \frac{840\ k\Omega \times 0.8\ V}{5\ V - 0.8\ V} = 160\ k\Omega$$

With a VOUT of 2.5 V on the TPS63070, the VMIN case, the voltage output of the DAC on the AFE539A4 is calculated based on the V_{min} of 5.2 V and the calculated resistor value R3.

$$I_1 = \frac{2.5\ V - 0.8\ V}{840\ k\Omega} = 2.02\ \mu A$$

The DAC VOUT is then calculated using the following equation.

$$V_{DAC} = 0.8\ V + (2.98\ \mu A \times 268.8\ k\Omega) = 1.6\ V$$



TEC Control DC/DC Resistor Divider Calculation Using VMIN Case

Selecting the Thermistor Value

A negative temperature coefficient (NTC) thermistor increases in resistance as temperature decreases. The data sheet for the thermistor defines the temperature versus resistance relationship. A voltage divider is created with the R_{DIV} resistor to get a voltage output from the NTC. Selecting the right R_{DIV} value determines the input voltage range (and therefore the temperature). Using a 12-kΩ resistor provides the ADC input with a voltage that is within the range of –25°C to 100°C. With the resistor divider, this temperature range is equivalent to the range of 0 to 5 V. This voltage divider can be calculated with the 5-V VDD and 10-kΩ thermistor used in this circuit. Using the equation for a voltage divider, the resistor divider value is calculated with the ADC input range of 0 V to 5 V over the given temperature range.

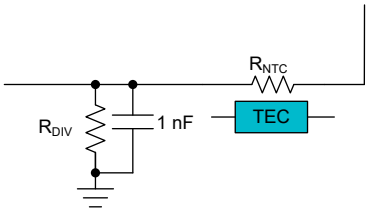
Relation of Component Temperatures to R_{NTC} Resistor Values

Component Temperature	R_{NTC} Resistance
–25°C	105 kΩ
25°C	10 kΩ
100°C	700 Ω

Table 1-1. Relation of Component Temperatures to V_{OUT} Outputs

Component Temperature	VOUT
–25°C	0.512 V
25°C	2.72 V
100°C	4.72 V

An additional 1-nF capacitor, parallel to R_{DIV}, is used for filtering noise. The following figure shows R_{DIV} and R_{NTC} in relation to the TEC.



TEC Control DC/DC Decoupling Capacitor Placement

PI Controller Setup

The AFE539A4 has an internal state machine that is factory-programmed to function as a proportional integral (PI controller). The two main components of a PI controller are the proportional and integral gains. The proportional gain (KP) is multiplied with the instantaneous error. The higher the KP value, the faster the loop corrects, but the loop is more prone to higher overshoot and can take longer to settle. The integral gain (KI) is multiplied to the accumulated error. KI can lower the steady state error but can lead to larger oscillations if too small of a value is used. The proportional and integral gains are programmed in the 16-bit registers. SRAM-DATA-35 is the register for proportional gain. SRAM-DATA-38 is the register for integral gain. The KP and KI selected for this system are: KP = 2048 and KI = 15. These gains are derived by iteratively testing the KP and KI values based on a response from the TEC component to maintain a speedy response that minimizes any ripple on the temperature of the TEC.

In addition to configuring the PI gains, the setpoint value (SRAM-DATA-37) must be configured. The PI controller compares the setpoint with the ADC input. With a setpoint value of 0x02DA, the AFE539A4 adjusts VDAC until the ADC input of 3.46 V or 40°C is achieved. The following equation shows how a value of 3.46 V is obtained for the setpoint value.

$$V_{SETPOINT} = VDD \times \frac{R_{DIV}}{R_{NTC} + R_{DIV}} = 5 \times \frac{12\ k\Omega}{12\ k\Omega + 5356\ k\Omega} = 3.46\ V$$

The value of 5.356 kΩ in the preceding equation is based on the temperature to resistance conversion from the data sheet of the NTC thermistor at 40°C.

The polarity of the loop is configurable. For this reference design, the loop polarity is left at the default (0 in SRAM-DATA-39). Additionally, the ADC mode can be configured in this register. The ADC0-MODE bit determines the impedance of the ADC. If the bit is low, the ADC on the AFE539A4 has an infinite impedance, resulting in the ADC_{Code} equation calculation using a K value of 3. If the bit is low, the impedance is finite and the K value is 1. For this design, the ADC0 has a finite impedance and the safe output is used. In failure scenarios, safe output can be used as a backup to test device functionality.

Register SRAM-DATA-36 configures the threshold of comparator 2. A comparator threshold of 0x8000 is used for this design.

ADC and DAC Code Calculations

Both the ADCs and the DACs on the AFE539A4 are 10 bits. The DAC and ADC code are calculated using the following equations.

$$DAC_{Code} = \frac{V_{DAC}}{V_{REF} \times GAIN} \times 2^N$$

$$ADC_{Code} = \frac{V_{IN} \times K}{V_{FS}} \times 2^N - 1$$

N is the total number of bits. This design configures the DAC VOUT channel to use the internal 1.21 V reference with a gain of 1.5 ×, and the ADC input to use the internal 1.21-V reference with a gain of 4 ×. The K value for the ADC is an attenuation factor and has a value of 1 to set the ADC to infinite impedance.

To calculate the ADC setpoint, use the following equation.

$$ADC_{SETPOINT} = \frac{V_{IN} \times K}{V_{FS}} \times 2^N - 1 = \frac{4.72 \times 1}{1.21 \times 4} \times 1023 = 997$$

Setting the ADC common-mode value is also important for achieving fluid control of the PI controller.

The system uses 0.8 V as a threshold value to reach the programmed setpoint for the controller when the setpoint (SRAM-DATA-34) for the DAC code is set to 0.8 V. Using the DAC range of 0 V to 1.6 V, the following decimal values are derived for the minimum (SRAM-DATA-33) and maximum (SRAM-DATA-32) DAC values for this design:

$$\mathrm{DAC_{MAX}Code} = \frac{1.6\ \mathrm{V}}{1.21\ \times\ 1.5} \times 2^{10} = 903\ \mathrm{d}$$

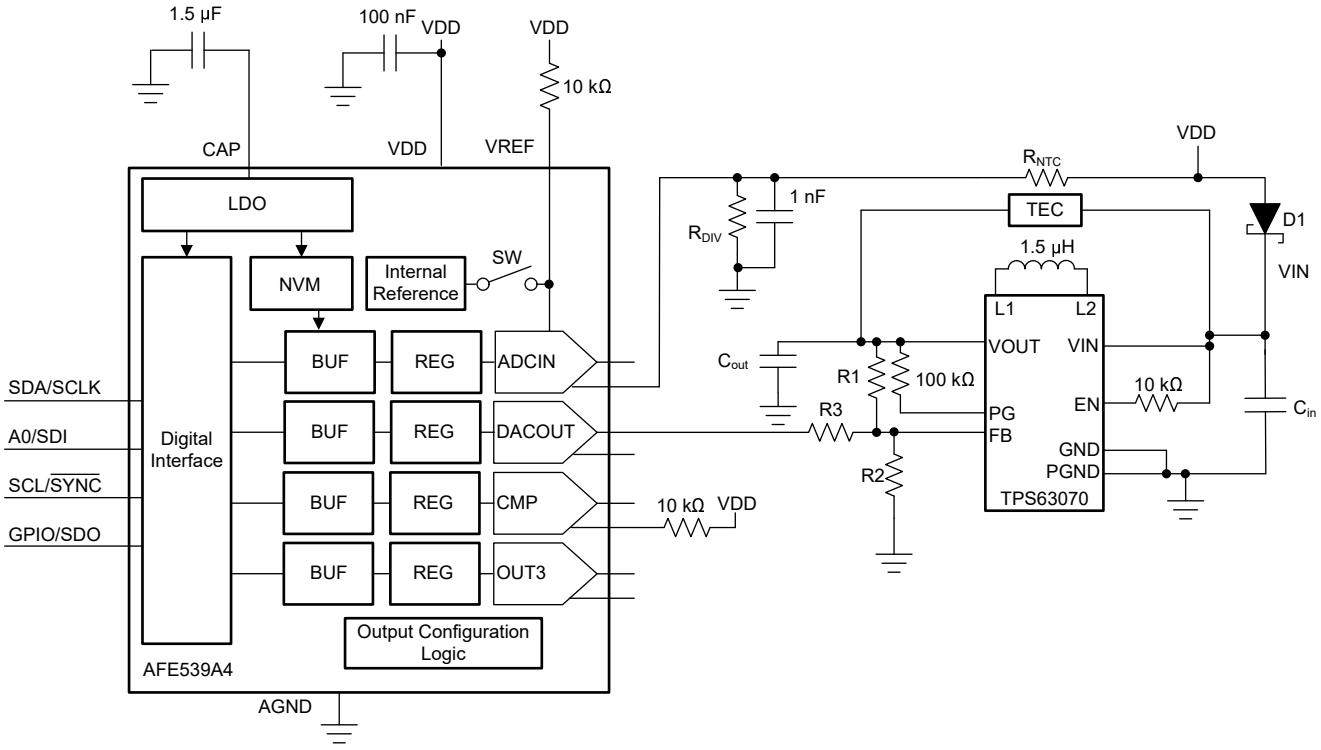
$$\mathrm{DAC_{MIN}Code} = \frac{0.8\ \mathrm{V}}{1.21\ \times\ 1.5} \times 2^{10} = 451\ \mathrm{d}$$

Note

The common mode value selected is the same value as the DAC minimum code.

Testing Results

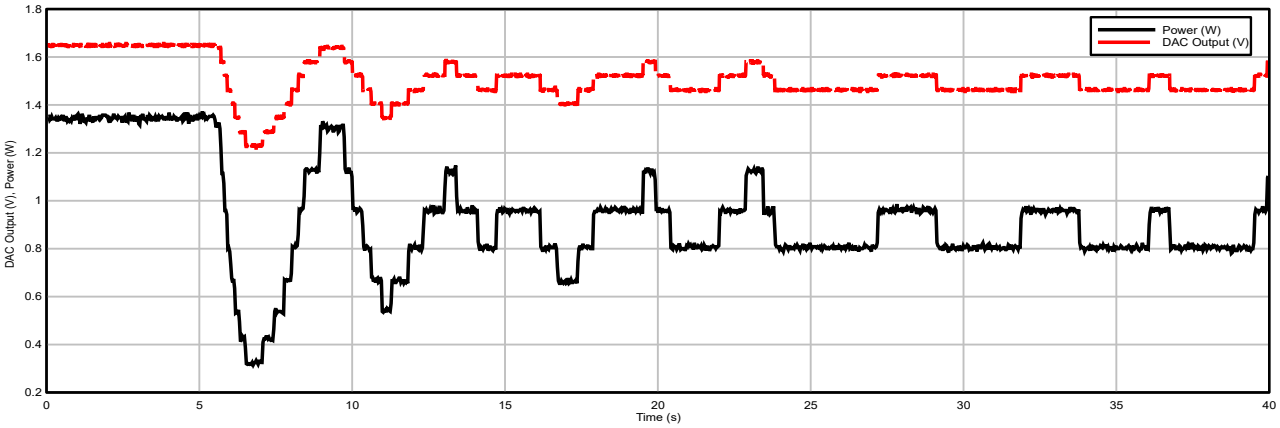
The evaluation board tests the functionality of the AFE539A4 with a power resistor as the TEC element. A 5-Ω power resistor is used to model the TEC since a TEC element is resistive.



TEC DC/DC Control Diagram

Measured Design Characteristics

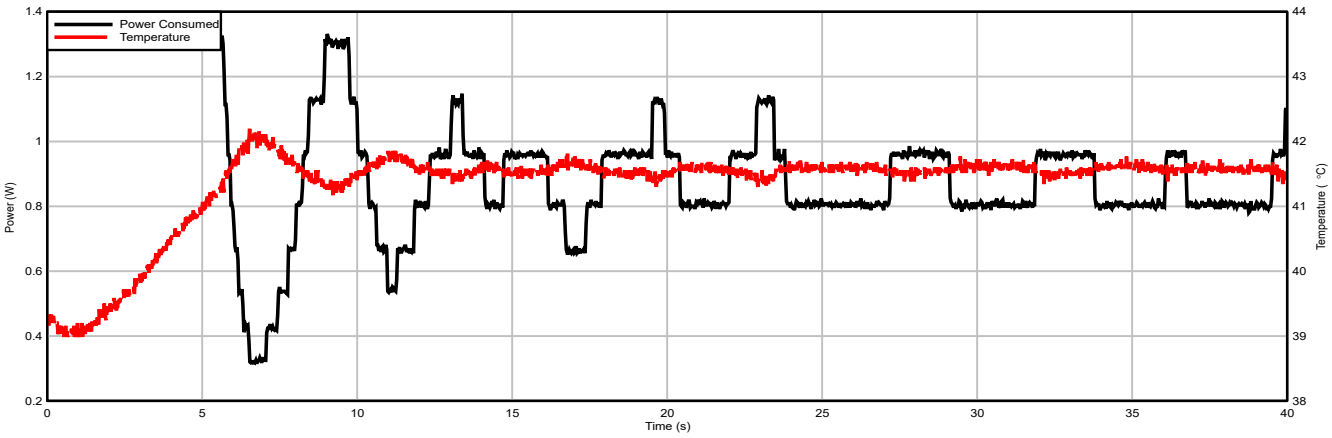
TEC DAC Output Voltage vs Power showcases the power consumption of the TEC element when testing the sensing of the thermistor. The device is initially turned on, then the power resistor is heated through the use of an external heat source. The power of the TEC lowers when the thermistor senses a temperature increase on the TEC, causing the ADC voltage to change. As the heat is removed, the PI controller on the device changes the voltage output of the DAC to modify the power consumption and return to the setpoint for the ADC.



TEC DAC Output Voltage vs Power

The preceding plot compares the relationship between the DAC voltage and the same power output of the TPS63070. Since the DAC voltage (and the resistor network) bias the voltage of the TPS63070, the DAC voltage has a proportional relationship to the power output of the TPS63070.

Measured Temperature of the TEC Versus DAC Power highlights the inverse relationship of the power on the TPS63070 and the temperature of the TEC. As the TEC (power resistor) heats up, the power consumption of the TEC lowers. Inversely, an increase in the power consumption results in the TEC cooling. As the PI controller approaches the setpoint, there is a ripple of approximately ±0.2°C.



Measured Temperature of the TEC Versus DAC Power

Register Settings

General Register Settings

Register Address	Register Name	Value	Description
0x27	STATE-MACHINE-CONFIG0	0x0003	[15:3] 0x0 Don't care
			[2] 0b0: Do not abort state machine
			[1] 0b1: Start state machine. Must be enabled in bit 0 as well
			[0] 0b1: Enable state machine. Note: State machine must be disabled when configuring registers; enable state machine before saving to NVM.
0x1F	COMMON-CONFIG	0x1249	[15] 0b0: Write 0b1 to set window-comparator output to a latching output
			[14] 0b0: Write 0b1 to lock device. Unlock by writing 0b0101 to DEVUNLOCK field in the COMMON-TRIGGER register
			[13] 0b0: Write 0b1 to set fault-dump read enable at address 0x01
			[12] 0b0: Write 0b1 to enable the internal reference
			[11:10] 0b11: Power down VOUT3
			[9] 0b1: Power down IOUT3
			[8:7] 0b11: Power down VOUT2
			[6] 0b1: Power down IOUT2
			[5:4] 0b11: Powers-down VOUT1
			[3] 0b1: Power down IOUT1
			[2:1] 0b11: Power down VOUT0
			[0] 0b0: Power up IOUT0
0x02	COMMON-TRIGGER	0x0002	[15:12] 0b000: Write 0b0101 to unlock the device
			[11:8] 0b0000: Write 0b1010 to trigger a POR reset
			[7] 0b0: Write 0b1 to trigger LAFE operation if the respective SYNCCONFIG-X bit in the AFE-X-FUNC-CONFIG register is 1
			[6] 0b0: Write 0b1 to set the AFE registers and outputs to zero-code or mid-code based on the respective CLR-SEL-X bit in the AFE-XFUNC-CONFIG register
			[5] 0b0: Don't care
			[4] 0b0: Write 0b1 to trigger fault-dump sequence
			[3] 0b0: Write 0b1 to trigger PROTECT function
			[2] 0b0: Write 0b1 to read one row of NVM for fault-dump
			[1] 0b1: Write 0b1 to store applicable register settings to the NVM
			[0] 0b0: Write 0b1 to reload applicable registers with existing NVM settings

AFE Output Configuration

Register Address	Register Name	Value	Description
0x03	DAC-0-VOUT-CMP-CONFIG	0x1405	[15:13] 0x0: Don't care
			[12:10] 0b101: Set gain to 4 ×, use internal reference
			[9:5] 0x0: Don't care
			[4] 0b0: Set OUTx pin to push-pull
			[3] 0b0: Generate comparator output but consume internally
			[2] 0b1: FB pin input has finite impedance
			[1] 0b0: Do not invert the comparator output
			[0] 0b1: Enable comparator mode. Current-output must be in power down
0x09	DAC-1-VOUT-CMP-CONFIG,	0x800	[15:13] 0x0: Don't care
			[12:10] 0b010: Set gain to 1.5 ×, use internal reference
			[9:5] Don't care
			[4] 0b0: Set OUTx pin to push-pull
			[3] 0b0: Generate comparator output but consume internally
			[2] 0b0: FB pin has high impedance
			[1] 0b0: Do not invert the comparator output
			[0] 0b0: Disable comparator mode.
0x0F	DAC-2-VOUT-CMP-CONFIG	0x0403	[15:13] Don't care
			[12:10] 0b001: Set gain to 1 ×, use VDD as reference
			[9:5] 0x0: Don't care
			[4] 0b0: Set OUTx pin to push-pull
			[3] 0b0: Generate comparator output but consume internally
			[2] 0b0: FB pin has high impedance
			[1] Invert comparator output
			[0] 0b1: Enable comparator mode. Current-output must be in power down
0x15	DAC-3-VOUT-CMP-CONFIG	0x1405	[15:13] 0x0: Don't care
			[12:10] 0b101: Set gain to 4 ×, use internal reference
			[9:5] Don't care
			[4] 0b0: Set OUTx pin to push-pull
			[3] 0b0: Generate comparator output but consume internally
			[2] 0b1: FB pin has finite impedance
			[1] 0b0: Do not invert comparator output
			[0] 0b1: Enable comparator mode. Current-output must be in power down

SRAM Configuration

Register Address	Register Name	Value	Description
0x20	SRAM_DATA_32	0xE1C0	[15:6] 0b1110000111: Input the maximum voltage output for the AFE. Value provided is for 1.6 V
			[5:0] 0x0: Don't care
0x21	SRAM_DATA_33	0x70C0	[15:6] 0b:0111000011: Configure the minimum output of the AFE
			[5:0] 0x0: Don't care
0x22	SRAM_DATA_34	0x02DA	[15:10] 0x0: Don't care
			[9:0] 0b:001011011010: Configure the setpoint value. Setpoint is the value the ADC is compared to by the PI controller
0x23	SRAM_DATA_35	0x007F	[15:0] 0b:0000000001111111 Configure the proportional gain (KP) value for the PI controller
0x24	SRAM_DATA_36	0x8000	[15:6] 0b1000000000000000: Set the threshold value of comparator channel 2
			[5:0] 0x0: Don't care
0x25	SRAM_DATA_37	0x2FF	[15:12] 0x0: Don't care
			[11:2] 0b0010111111: Configure the common-mode value. The common-mode value is present at the PI output when KP and KI are zero
			[1:0] 0x0: Don't care
0x26	SRAM_DATA_38	0x0007	[15:0] 0b0000000000000011: Select the integral gain value for the PI Controller. Setting this value to 0 disables KI
0x27	SRAM_DATA_39	0x0002	[15:6] 0b0000000000: Safe-Output value
			[5:2] 0x0: Don't care
			[1] 0b1: Select a finite-impedance input for ADC0
			[0] 0b0: Configure the loop polarity of the PI controller

Pseudo Code Example

Pseudo Code Example for Voltage Output Configuration

```
//Stop the state machine.
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x00
//Enable all AFE channels
WRITE COMMON-CONFIG(0x1F), 0x0F, 0xF9
//Select the desired voltage reference, output range, and comparator    settings for each AFE.
Channels 0, 2, and 3 are configured as comparators.
//set AFE 0...
WRITE DAC-0-VOUT-CMP-CONFIG(0x03), 0x14, 0x05
//set AFE 1...
WRITE DAC-1-VOUT-CMP-CONFIG(0x09), 0x80, 0x00
//set AFE 2...
WRITE DAC-2-VOUT-CMP-CONFIG(0x0F), 0x04, 0x03
//set AFE 3...
WRITE DAC-3-VOUT-CMP-CONFIG(0x15), 0x14, 0x05
//Calculate the voltage range for AFE1 using the equation in the data sheet, and configure the
minimum and maximum output.
//Using a maximum of 1.6V
WRITE SRAM-DATA-32(0x20), 0xE1, 0xC0
//Using a minimum of 0.8V.
WRITE SRAM-DATA-33(0x21), 0x70, 0xC0//Set the configuration parameters LOOP-POLARITY, ADC0-MODE,
CMP2-THRESHOLD, and SAFEOUTPUT as appropriate for the system
//Loop polarity, ADC0 mode, and Safe-output can be configured in SRAM-DATA-39
WRITE SRAM-DATA-34(0x22), 0x02, 0xDA
//CMP_2 Threshold is configured in SRAM_DATA_36
WRITE SRAM-DATA-36(0x23), 0x80, 0x00
//Program the initial values of KP and KI
//Note a higher KP is bad for systems with a fast response.
WRITE SRAM-DATA-35(0x24), 0x00, 0x01
//Note a higher KI can mean worse steady state response; KI can be disabled if set to 0
WRITE SRAM-DATA-38(0x25), 0x00, 0x00
//Calculate a desired common mode value using the
WRITE SRAM-DATA-37(0x26), 0x02, 0xFF
//Set the loop polarity, ADC impedance, and safe output value
WRITE SRAM-DATA-39(0x20), 0x00, 0x02
//Start the state machine
WRITE STATE-MACHINE-CONFIG0(0x27), 0x00, 0x03
//Tune the KI and KP values to achieve the best steady-state and transient response.
WRITE SRAM-DATA-35(0x24), 0x80, 0x00
WRITE SRAM-DATA-38(0x25), 0x00, 0x0F
//Store the register settings
WRITE COMMON-TRIGGER(0x20) 0x00, 0x02
```

Design Featured Devices

Device	Key Features	Link
AFE539A4	Four-channel 10-bit smart AFE with PI and TEC control with built-in ADC and AFE	AFE539A4
TPS63070	Wide input voltage (2 V–16 V) buck-boost converter	TPS63070
TPS63802	2-A, high-efficient buck-boost in QFN package	TPS63802

Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, AFE539A4 Evaluation Module product page
- Texas Instruments, TPS63802 product page
- Texas Instruments, AFE539A4EVM EVM User's Guide
- Texas Instruments, *PMP9796 5-V Low-Power TEC Driver Reference Design* design guide
- Texas Instruments, Smart AFE for TEC Control video
- Texas Instruments, [FAQ] Where can I find more information about smart AFEs?
  - What is a smart AFE?
  - How smart AFEs offer an integrated analog solution for thermoelectric cooling control

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