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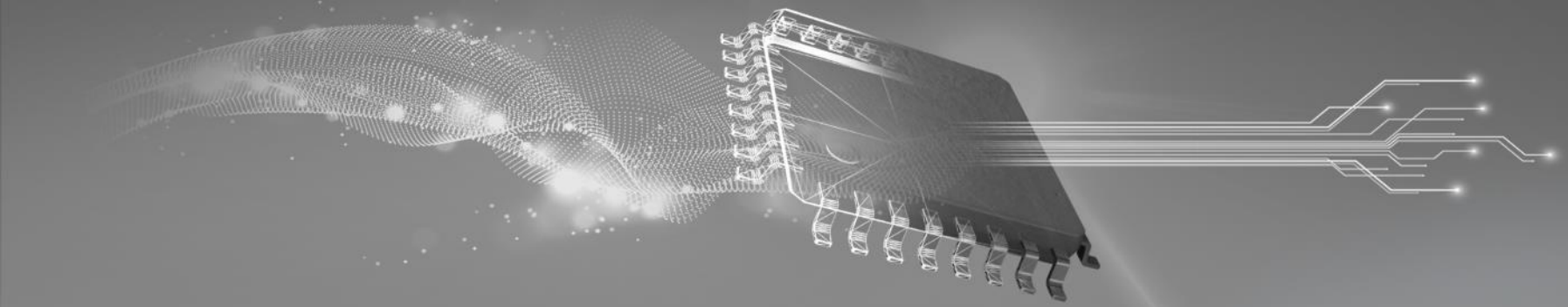

FPD-Link™ high speed design and channel requirements

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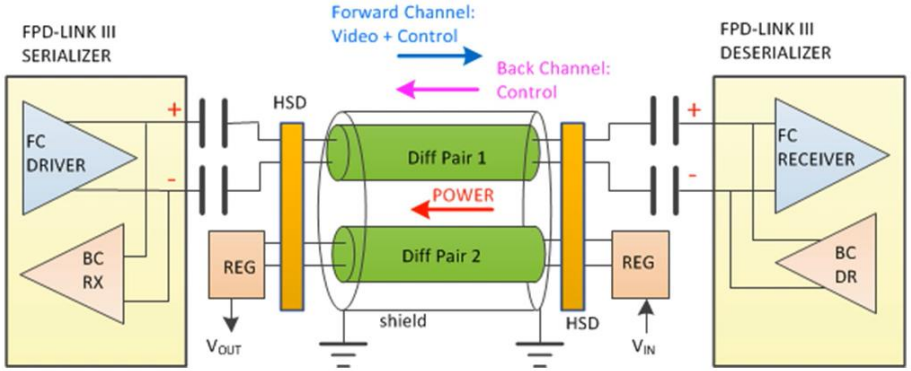
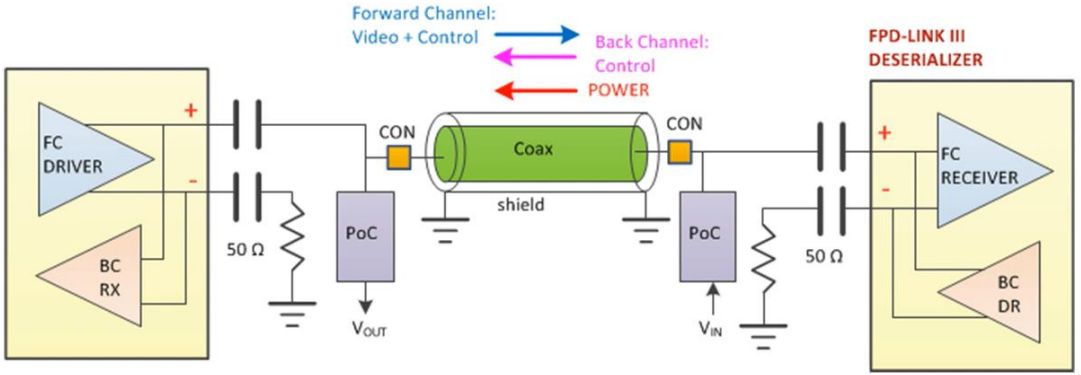
Overview

- FPD-Link™ channel requirements
  - Signaling topologies
  - PCB elements and transmission loss characteristics
  - Key channel parameters
- High speed design
  - Connectors and cables
  - PCB dielectrics
  - Layout considerations

FPD-Link III signal topologies



Differential Signaling

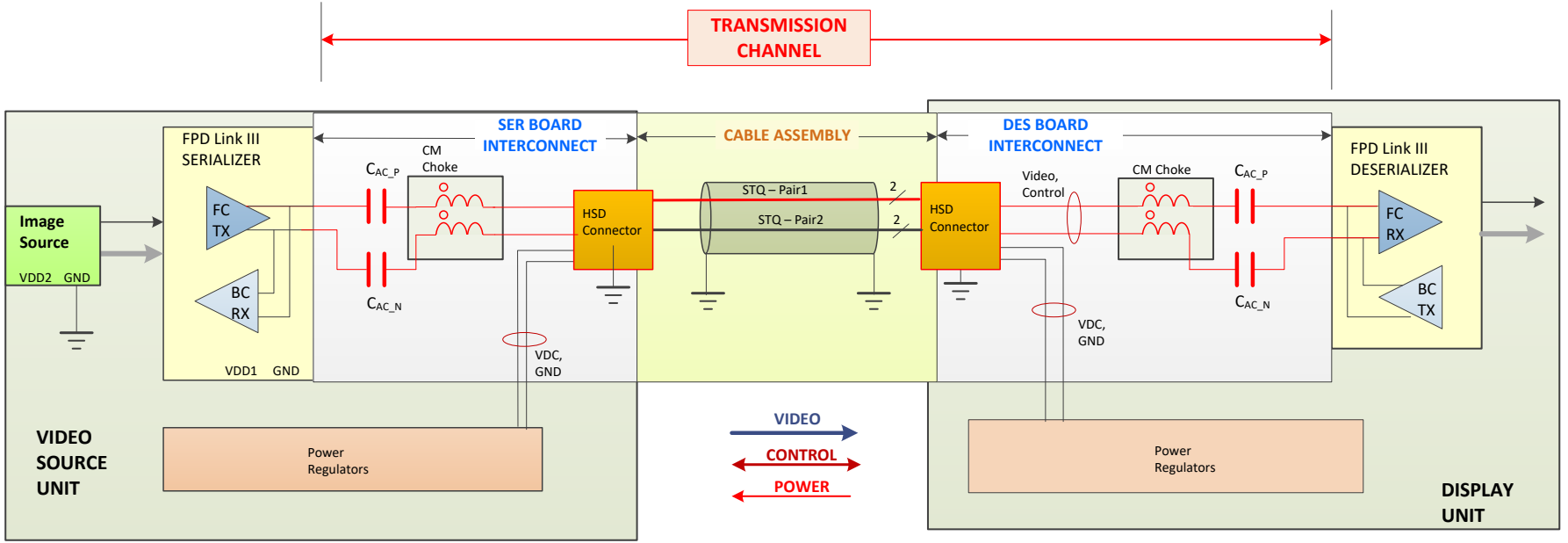


Single-End Signaling

FPD-Link III transmission channel

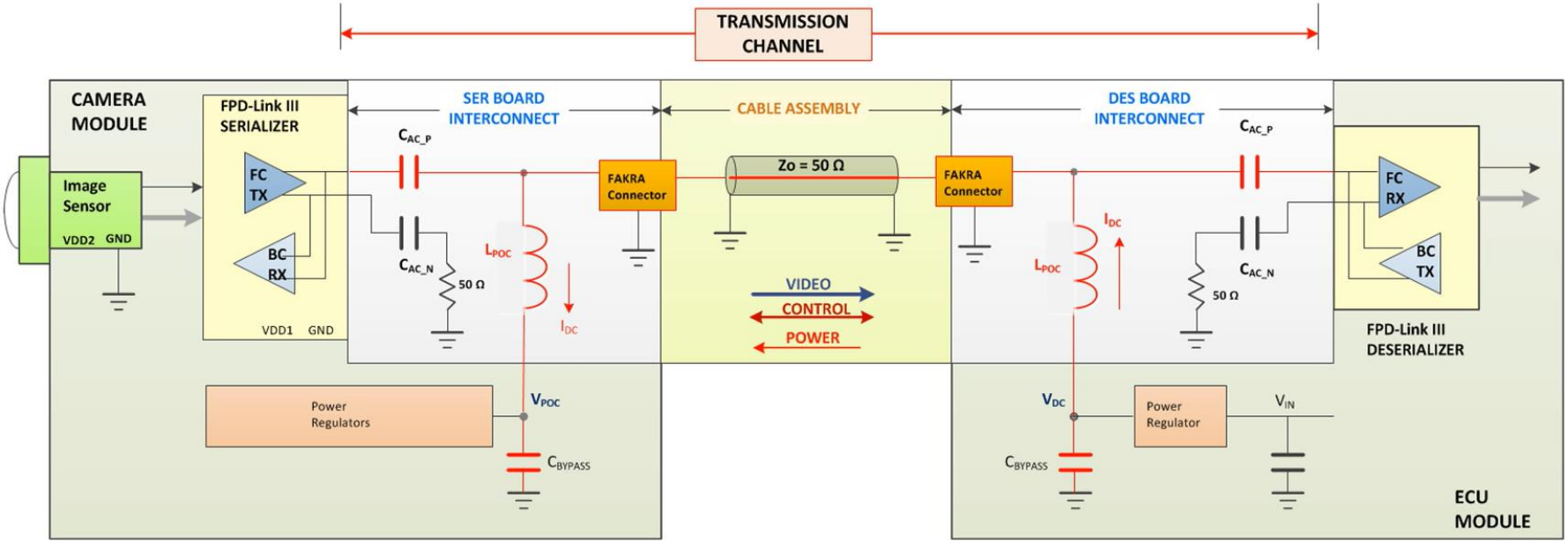
- Transmission channel refers to the transmission media that connects a Serializer to a Deserializer integrated circuit
- It is not just the cable harness, but includes board traces, components and board parasitic in the Serializer and Deserializer boards
- In a typical SER or DES board, channel in the SER or DES boards include
  - AC coupling capacitors
  - Common mode choke
  - PCB traces
  - PCB parasitic
- Cable harness includes connectors, cable and in-line connectors

Transmission channel: differential signaling



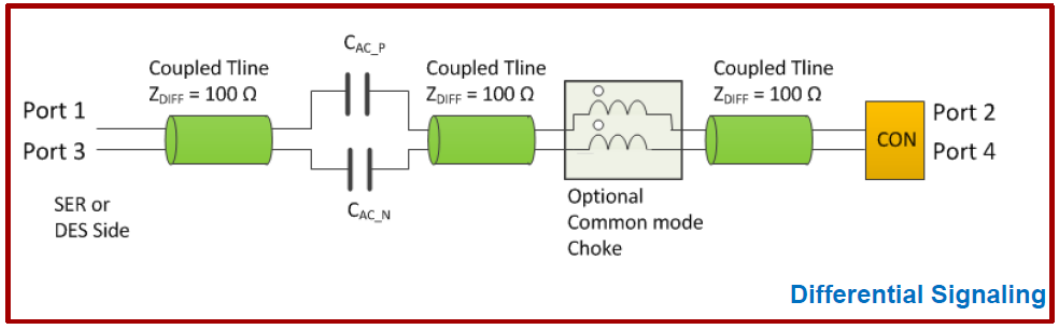
- Transmission Channel for FPD-Link III refers to the interconnecting elements from a Serializer to a Deserializer
- Includes PCB differential traces, AC Coupling capacitors, common mode choke (optional), connector, and cable
- Transmission Channel = SER Board + Cable Assembly + DES Board

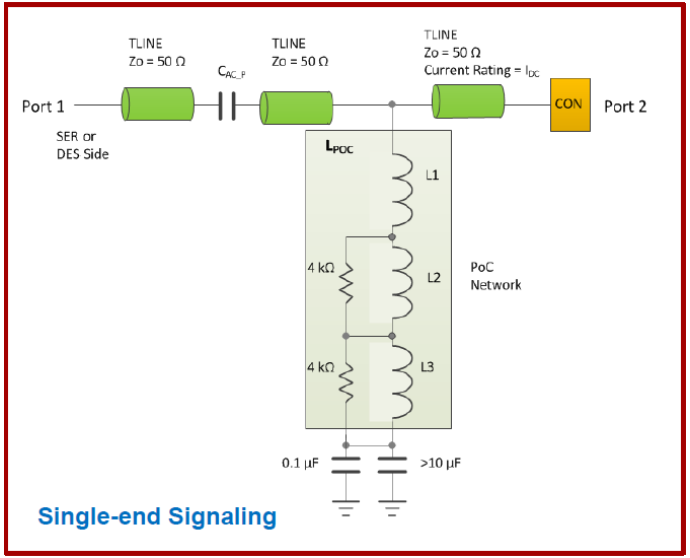
Transmission channel: single-ended signaling



- Transmission Channel for FPD-Link III refers to the interconnecting elements from a Serializer to a Deserializer
- Includes PCB trace, AC Coupling capacitor, PoC network (optional), connector, and cable
- Transmission Channel = SER Board + Cable Assembly + DES Board

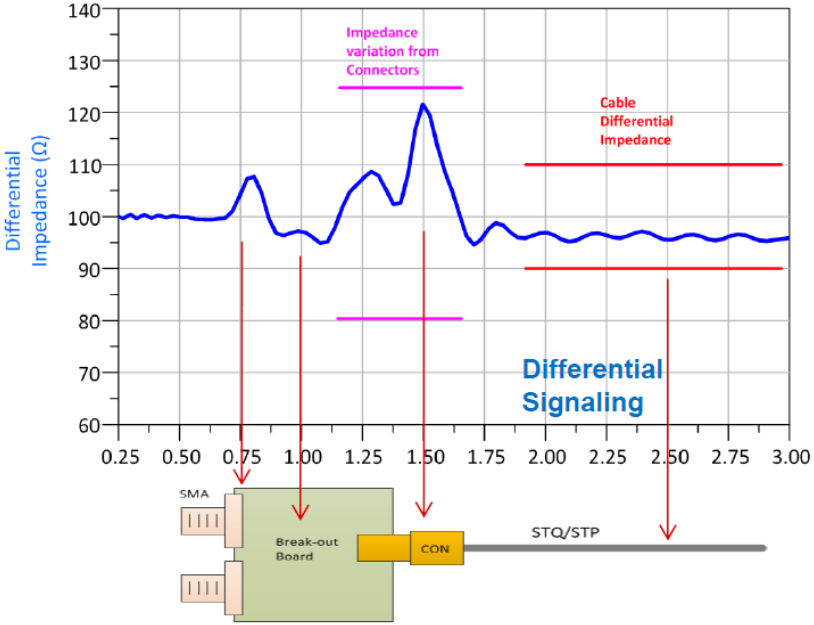
SER-board and DES-board elements

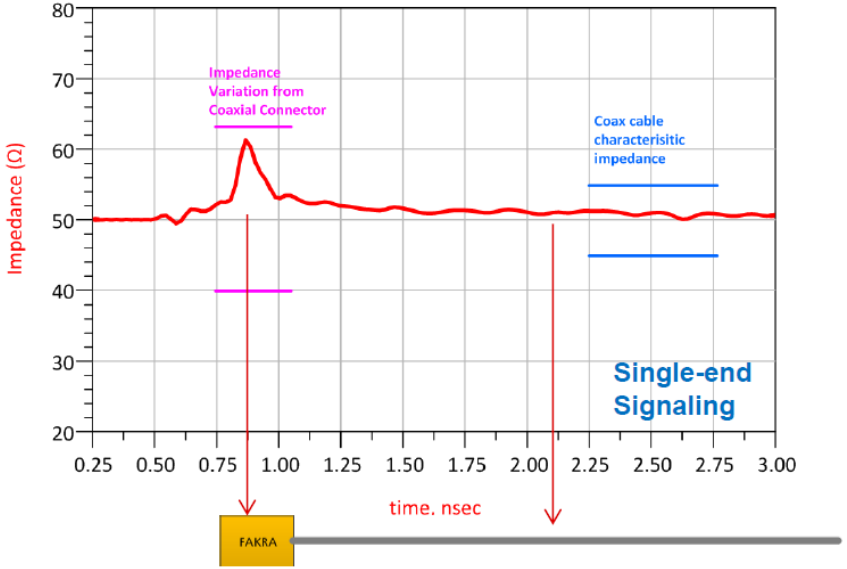




- Channel Transmission Loss = IL (SER-Board) + IL (Cable) + IL (DES-Board)
- Transmission loss of SER-Board and DES-Board are usually small compared with that of cable
- Maintain good impedance, minimize impedance mis-match
- For PoC, choose PoC network that will not impact the board's impedance

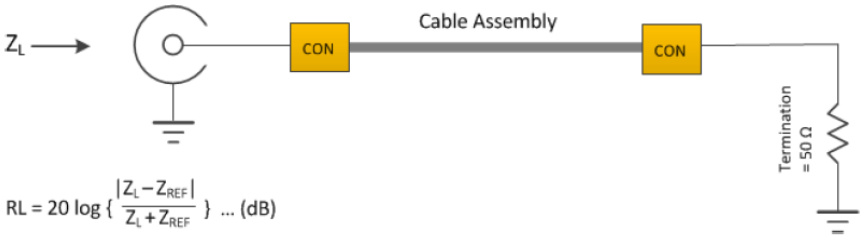
Characteristic impedance



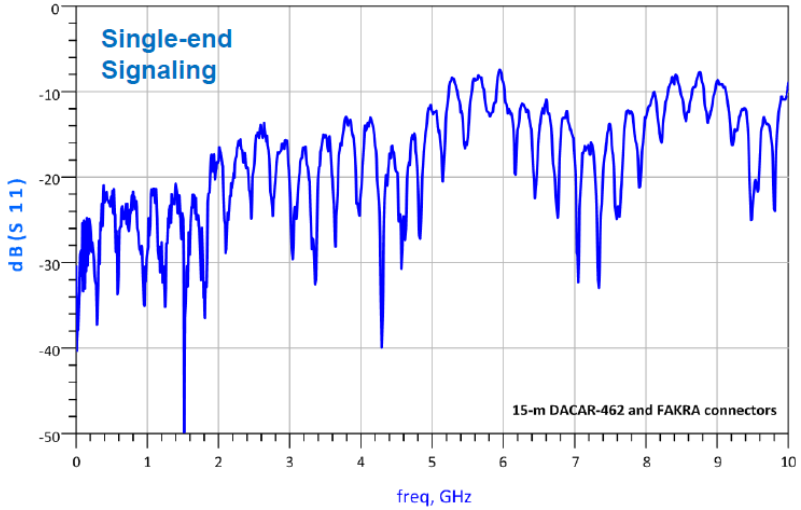


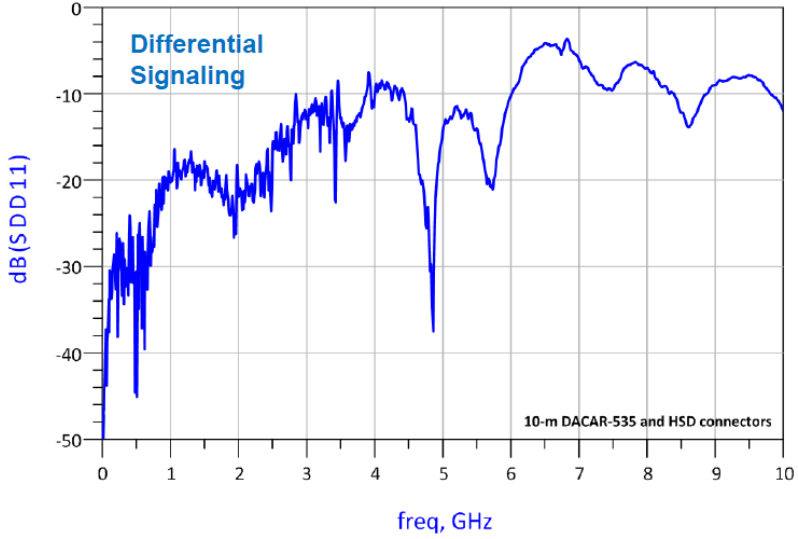
- PCB and Cable Impedance designed to match with termination impedances of SER and DES
- Differential signaling: 100 Ω ± tolerance
- Single-end signaling: 50 Ω ± tolerance
- Excessive impedance mis-match causes reflection that degrades signal quality

Return loss

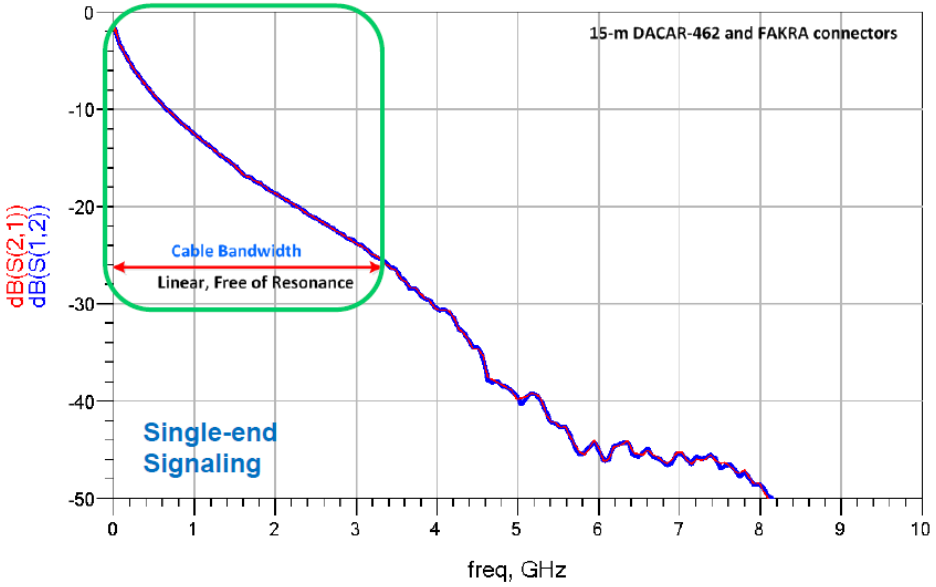


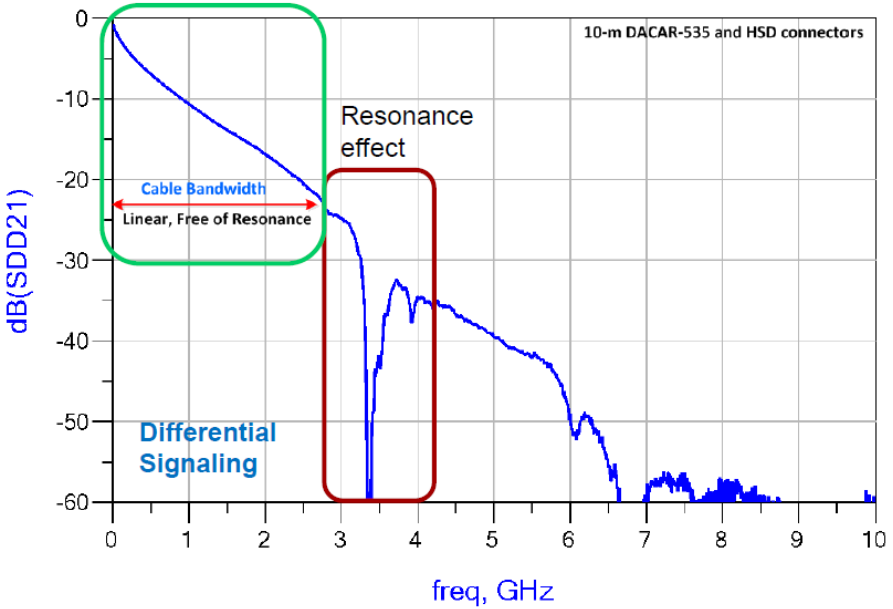
- Return loss measures impedance matching versus frequency
- Indicative on how well device's impedance matches a reference impedance (100 Ω for differential, 50 Ω for single-end)
- Indicative on signal reflection and echo due to impedance mis-match





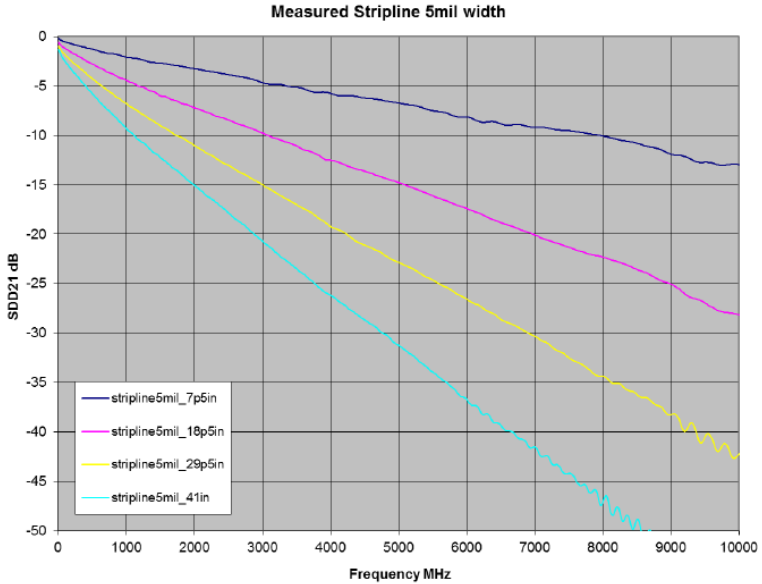
Insertion loss

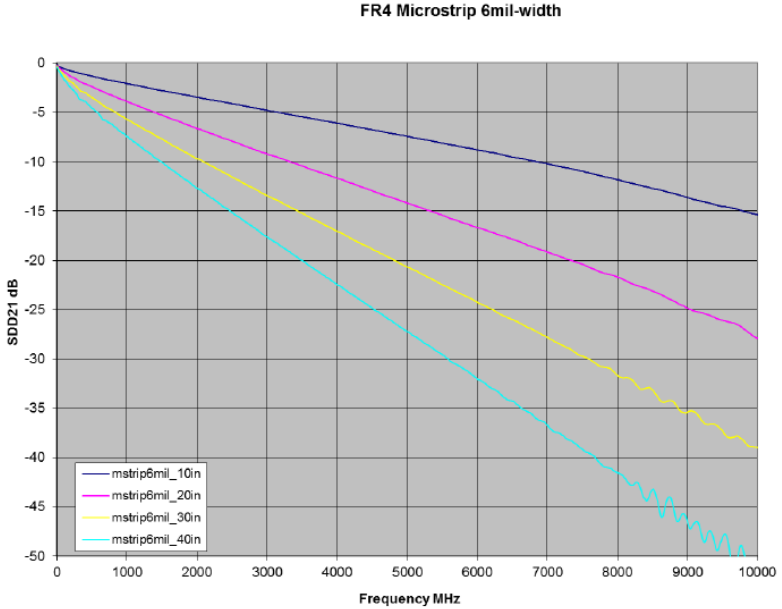




- Channel behaves as a Low-pass-filter: higher signal attenuation at higher frequencies
- Channel Useable bandwidth depends on:
  - Linear region, free of resonance
  - Insertion loss within the range that a SER and DES can compensate

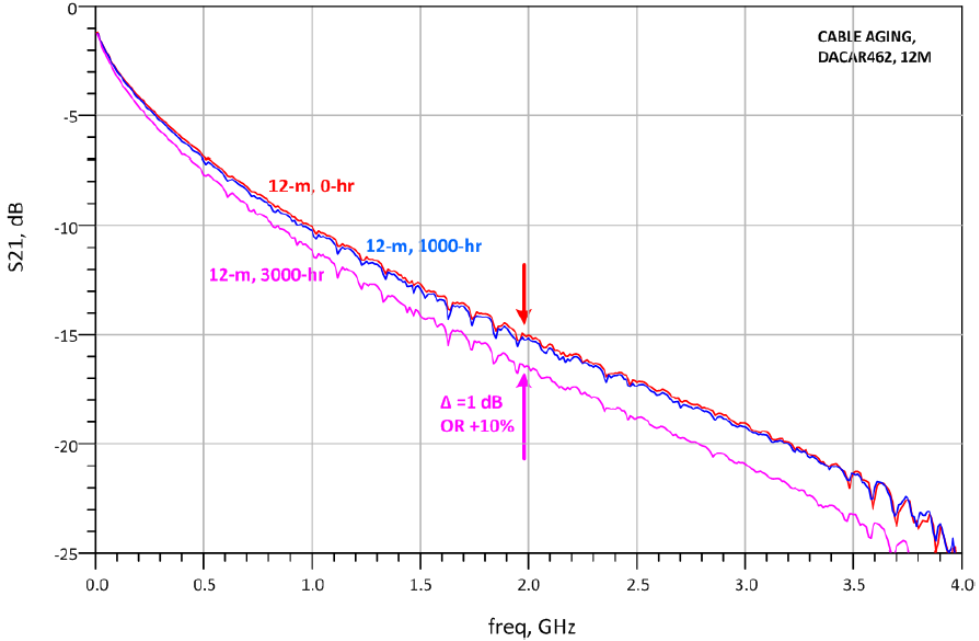
Insertion loss from PCB traces





- PCB board trace contributes a small portion of the Transmission Channel's loss
- A 5-mil FR4 stripline has about 0.37 dB/inch at 2 GHz
- A 6-mil FR4 microstrip has about 0.31 dB/inch at 2 GHz

Cable aging and mechanical stress



- Insertion loss changes due to cable aging
- Return loss will also change due to bending or dynamic movement of a cable segment (eg flip-display)
- Temperature cycling and mechanical stress tests are usually done during cable qualification to assess possible impact to link robustness

FPD-Link IV High Speed Design

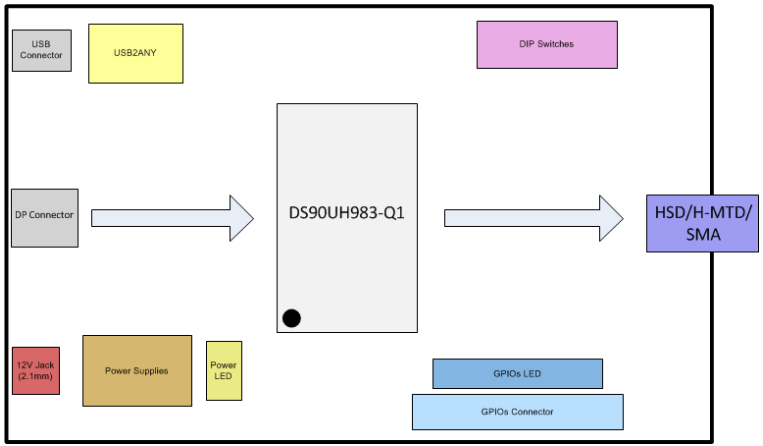
- Connectors and cables
- PCB dielectrics
- Layout considerations

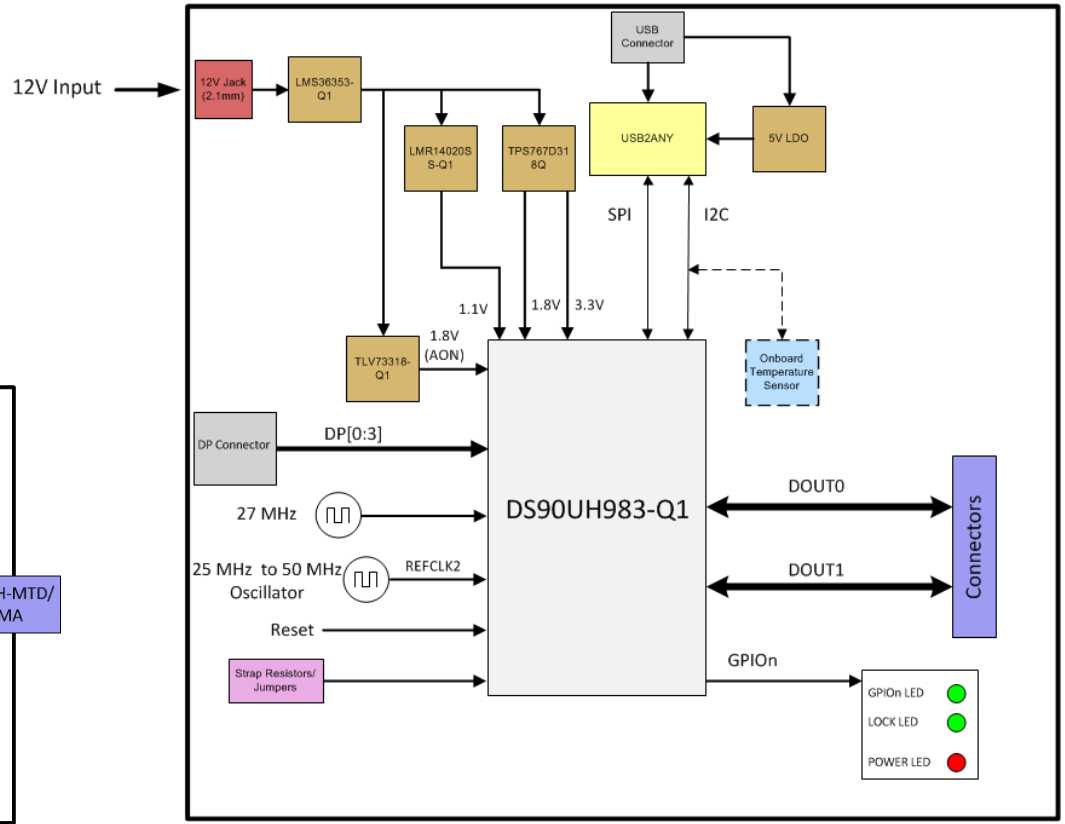
High-speed PCB design goals

- Tight impedance control (eg 100Ω ±5%)
- Minimize impedance mis-match (eg 100Ω ±10%)
- Minimize use of via and via stub
- Minimize insertion loss (typical -1.9dB)
- Minimize differential return loss (typical -12dB)
- Minimize mode conversion
  - Intra-pair skew matching (50 ps of t_{RX} HBR3)
  - Inter-pair skew matching
- Minimize crosstalk

Planning high-speed PCB design

- Placement
- Signal speed
- Power supply
- Sensitive signals
- Component selection



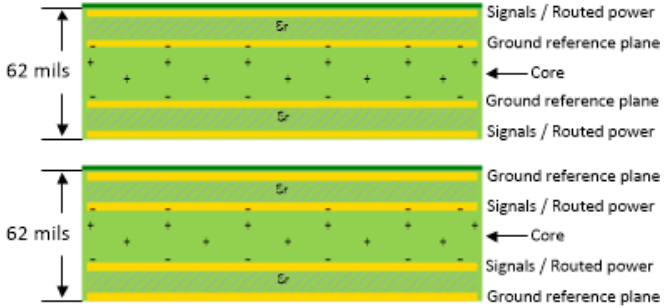


PCB design for low EMI

- Each signal trace needs an adjacent return path (plane or trace)
- Every power trace or plane needs an adjacent return path (plane or trace)
- Return path through layers
  - Ground vias
  - Stitching capacitors

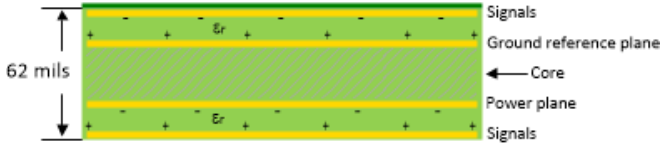
Good versus poor four-layer design

Good



- Low EMI
- Power return plane is closer.
- Both internal or external signals has immediately return path.

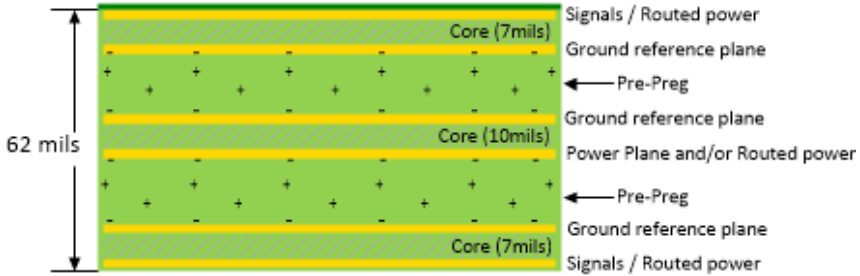
Poor



- Poor stack-up is likely in high EMI risk.
- Power and ground return plane are too far apart from the ground reference and power plane ~20 – 30mils.
- Signals on layer 4 are referenced to power instead of signals return path.

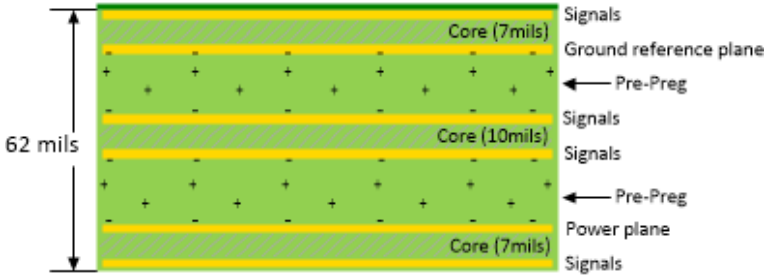
Low EMI six-layer stackup

Good



- Each signal layer has adjacent return path
- Power immediately return path to ground plane

Poor



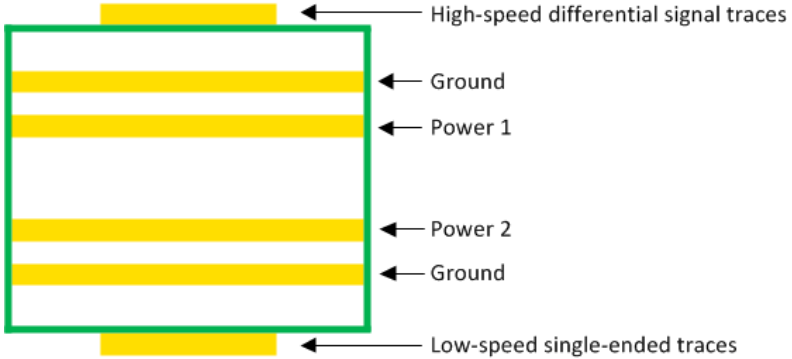
- Common stack-up
- Signal referenced to power
- Power and return plane too far separated
- Power transients couple to inner signal layers

Multi-layer stack up using microstrip

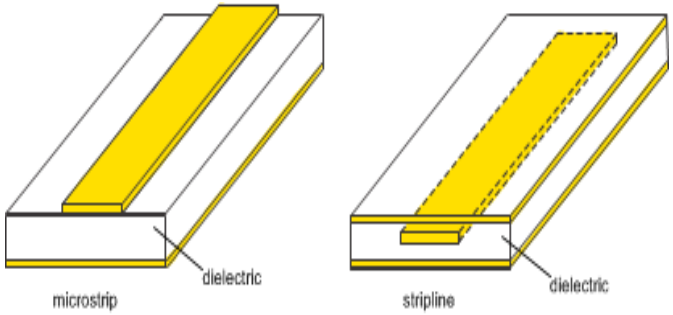
Hybrid Board

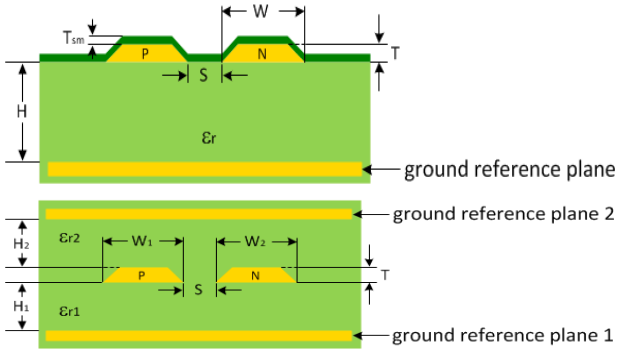
- Planning for stack up
- Material selection
- Cost saving

Layer	Layer Information		Thickness
	Soldermask		
TOP →			0.5 Oz
	Core	RO4350B	← 4.016 mils
L2_GND1 →			0.5 Oz
	Prepreg	IT-180A	← 12.946 mils
L3_PWR1 →			1 Oz
	Core	IT-180A	← 20.078 mils
L4_PWR2 →			1 Oz
	Prepreg	IT-180A	← 13.509 mils
L5_GND2 →			0.5 Oz
	Core	RO4350B	← 4.016 mils
BOT →			0.5 Oz
	Soldermask		



Structures of microstrip and stripline





- **microstrip**
  - Simple routing and easy to construct
  - Cheap to fabricate
  - Easy for assembly
  - Reliability

- **stripline**
  - More complex to fabricate
  - Manufacturing drives the cost
  - Signal path discontinuities
  - Harder for troubleshooting
  - Very low impedance
  - Require multiple layers

Examples of uniform board structures

Microstrips

Solder mask

Buried Microstrips

Coplanar

If GND-fill is used, it may create a co-planar structure

Edge Coupled Striplines

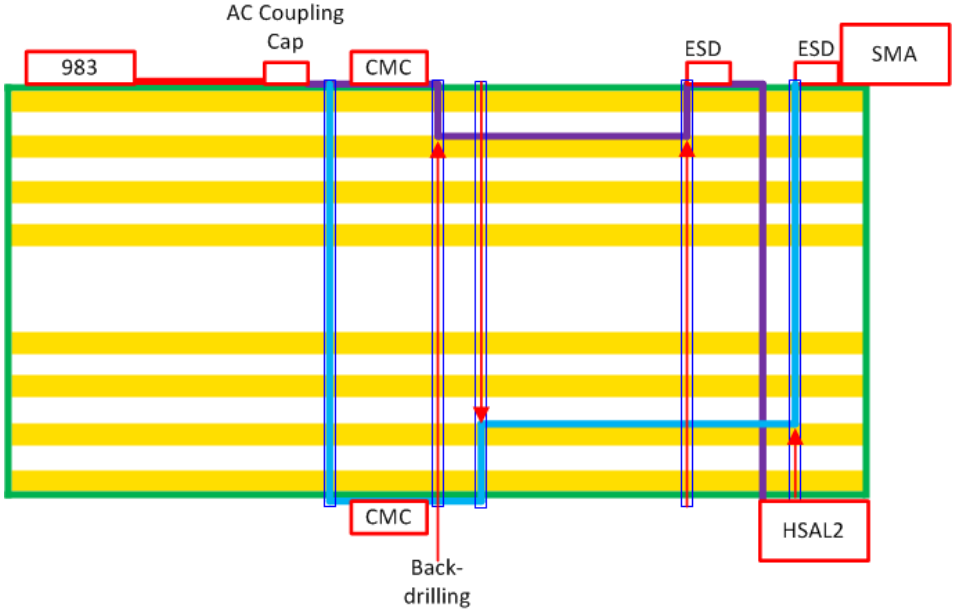
Broad-side Coupled Striplines

NI: TX Line:
Link to Free Download

✓ Estimate impedance with an Impedance Calculator

Eight layer stack up for stripline

- Microstrip routing from 983 to AC coupling caps
- Split routing can be done at the AC coupling caps
- Requires additional CMC and ESD



Material data rate, dielectric constant, loss tangent

Material	Supported Data Rate (GHz)	εr	Tan (δ)
Isola 370HR	1	4.17	0.016
Isola FR408HR	1	3.69	0.009
Isola I-Speed	1	3.65	0.0058
Megatron 6	1	3.71	0.002
Nelco 4800-20	2	3.70	0.007
Rogers 4350B	10	3.48	0.0037

Normalized material cost comparison

Material Group	Vendors Specific	FR4 Relative Cost Factor
High Tg	Isola 370HR	1.1
High Frequency	Isola FR408HR	1.8
High Frequency	Isola I-Speed	3.3
High Frequency	Nelco 4800-20	4.2
High Frequency	Megtron 6	5
High Frequency	Rogers 4350B	5.6

Discontinuous return path

- Common PCB problems can be traced to discontinuous signal. When design PCB for the FPD-Link frequencies used for 98x family device, this is becoming more of an issue.
- Often, the return path is disconnected by most error
  - Discontinuity such as gap or slot in the return plane or power plane
  - Changing reference planes

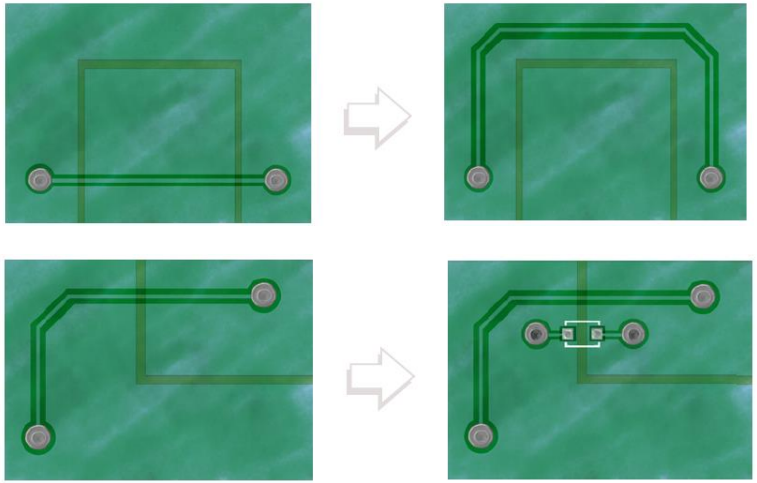
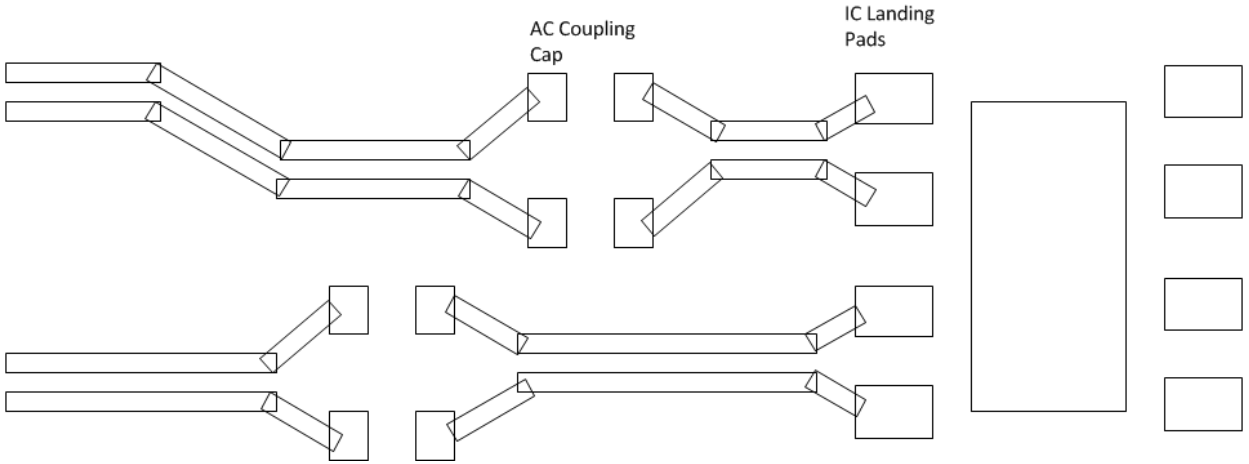


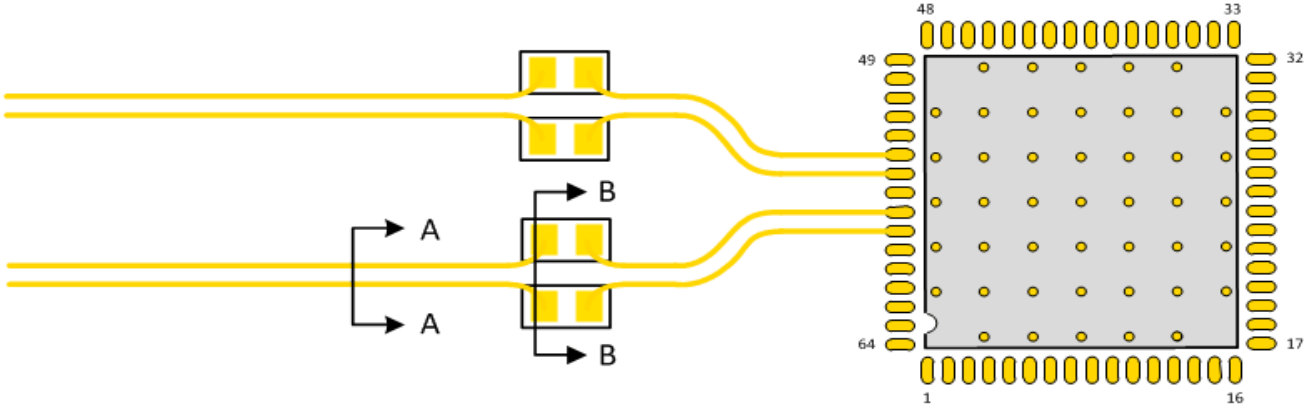
Image Source: Sierra

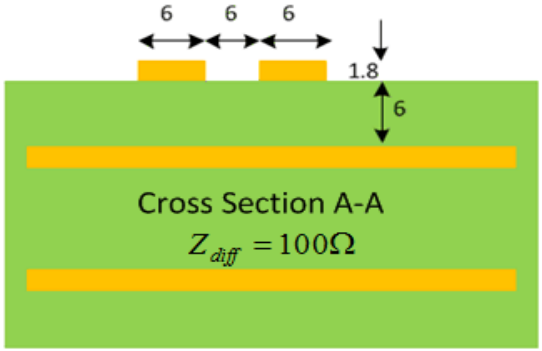
Differential traces

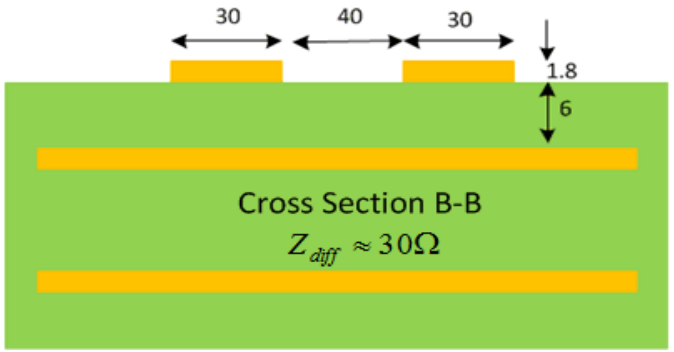


- Symmetry: Uniform Width, Uniform Gap
- Bends: 45º or Radial (smooth angle routing)
- Tightly coupled traces to minimize inter-pair crosstalk
  - If only P-signal is used, loosely couple traces should be used
- Minimize impedance discontinuity: due to trace branching out
- Minimize impedance discontinuity: due to large landing pads
- Manage Intra-pair skew matching
- Manage Inter-pair skew matching

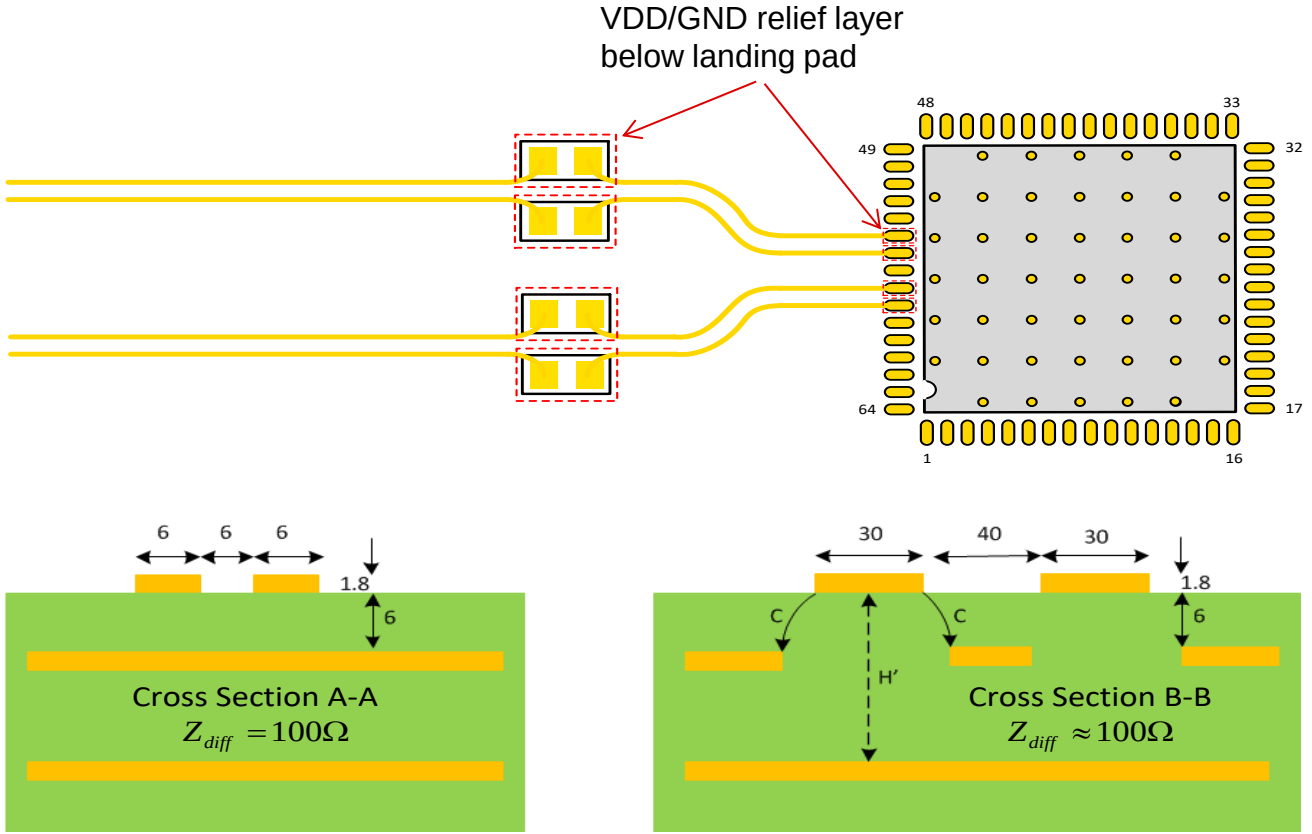
Impedance mis-match from landing pads



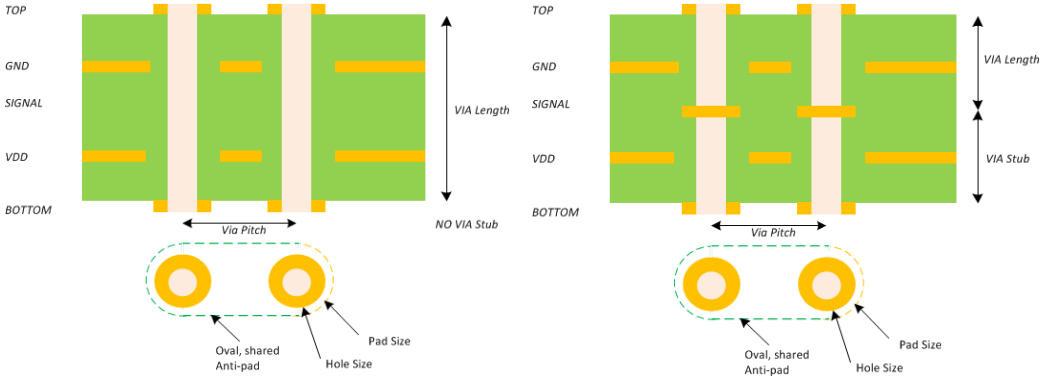


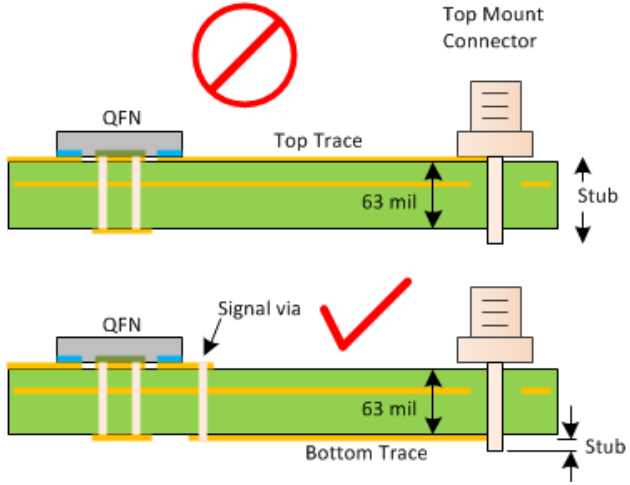


Controlled-impedance landing pads

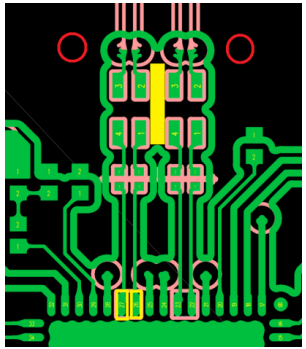


Avoid via stub



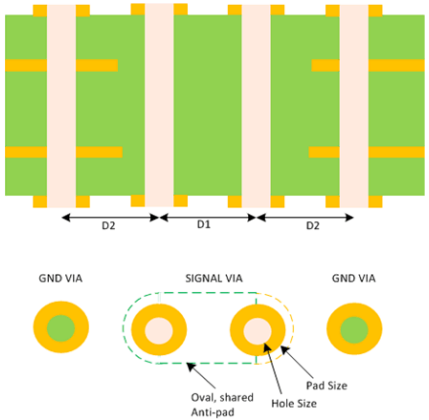


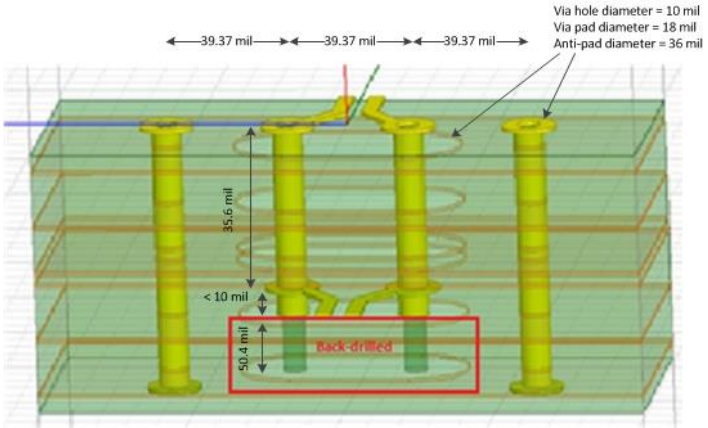
- Via Stub introduce capacitive effect to signal, increase signal loss
- Place signal layer toward bottom side of the board -> minimize Via Stub (<15 mil)
- Top-mount through-hole component -> use bottom trace routing to avoid Via Stub
- Use back-drill to remove via stub for very high speed applications (> 10 Gbps)

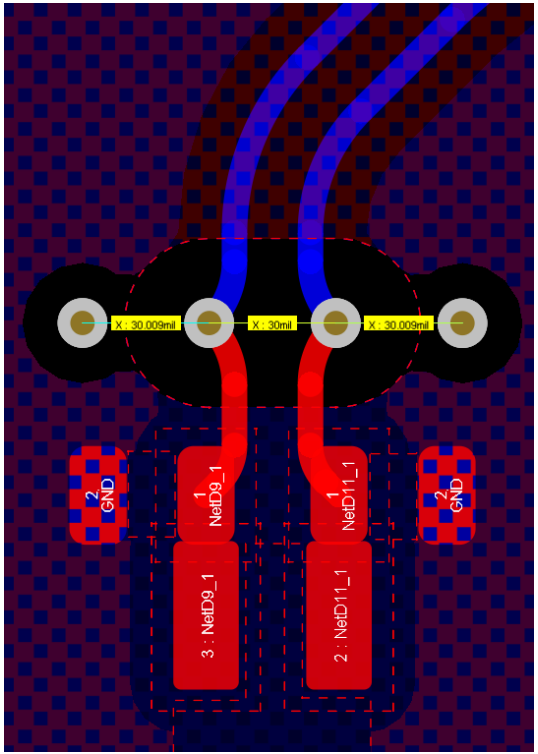


Differential via

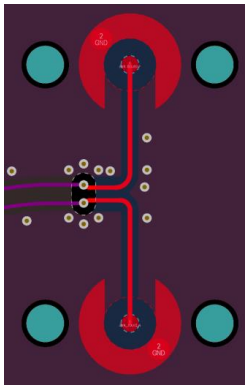
- Stripline method normally introduces signal via
- Two differential vias must be maintained close proximity between the two conductor vias
- Anti-pad clearance applies to all layers
- Use back drilling method to remove unused via cylinder (copper barrel) for all high speed routing signal path

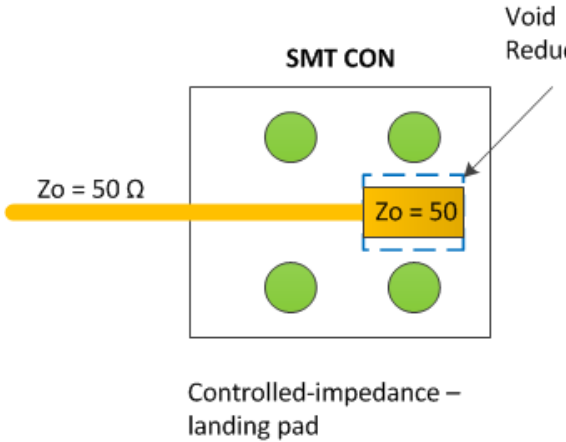


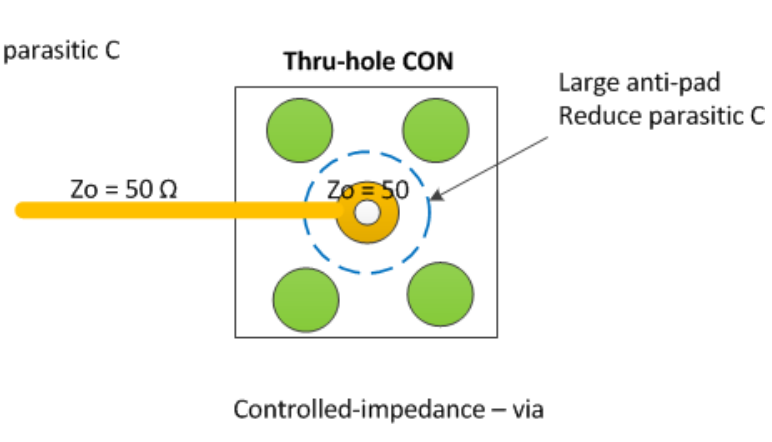


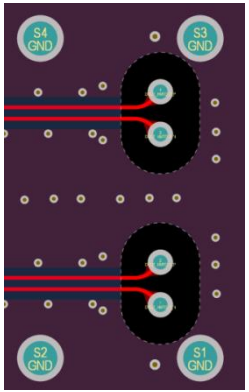


Controlled impedance footprint for connectors







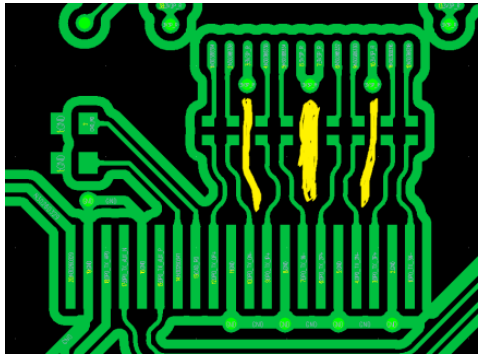


- Use PWR/GND VOID under landing pad
- Keep landing pad impedance same as trace
- Consult connector vendor for optimize footprint

- Use large anti-pad around via
- Keep via impedance same as trace
- Consult connector vendor for optimize footprint

Minimize crosstalk

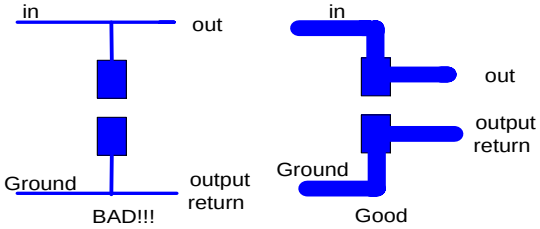
- Use coupled differential pairs
  - eg. 5-5-5, 5 mil air gap w/ 5 mil trace widths
- Maximize separation between adjacent pairs (S > 5W)
  - Use alternate layer routing if too many pairs on one layer
- Use staggering via or components (eg AC coupling capacitors) to keep separation between adjacent pairs
- Use G-S-S-G to minimize via crosstalk
- No rule of thumb, layout decision based on simulation result

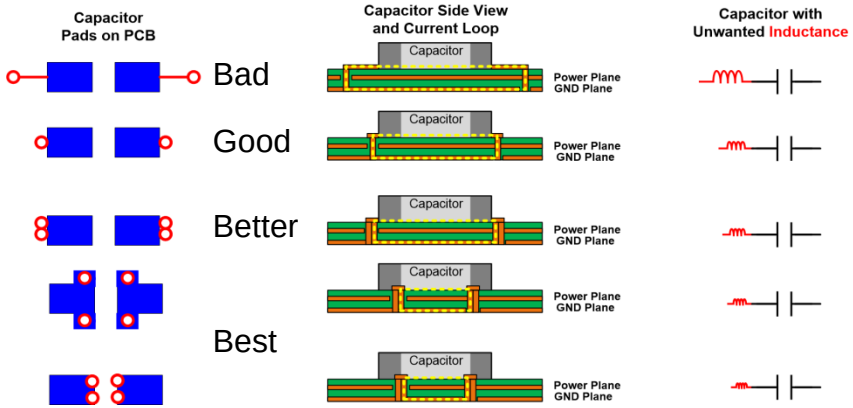


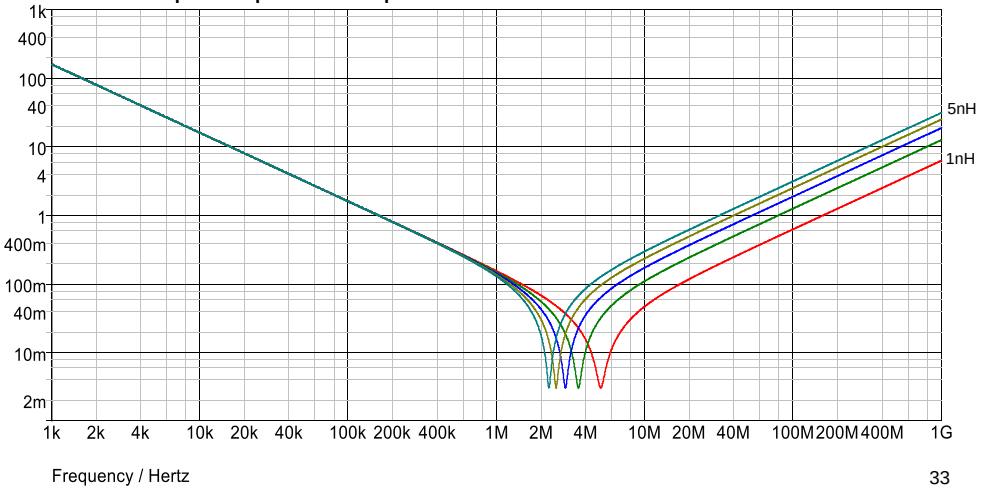
Bypass capacitor routing

example

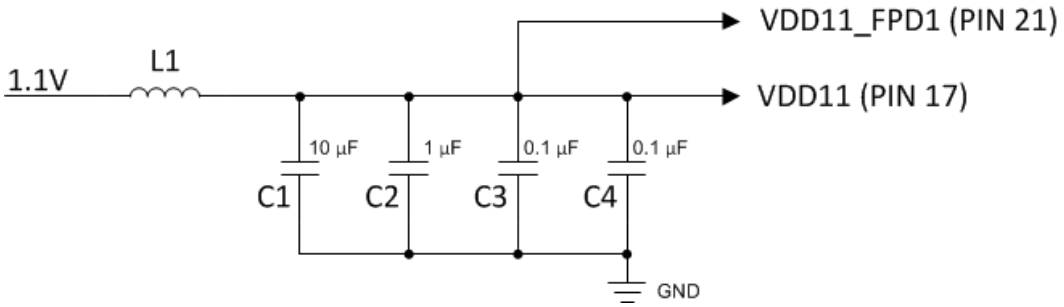
- Place bypass capacitors on same side of board as component being decoupled or underneath the device
- Locate as close to pin as possible
- Keep trace width thick and short

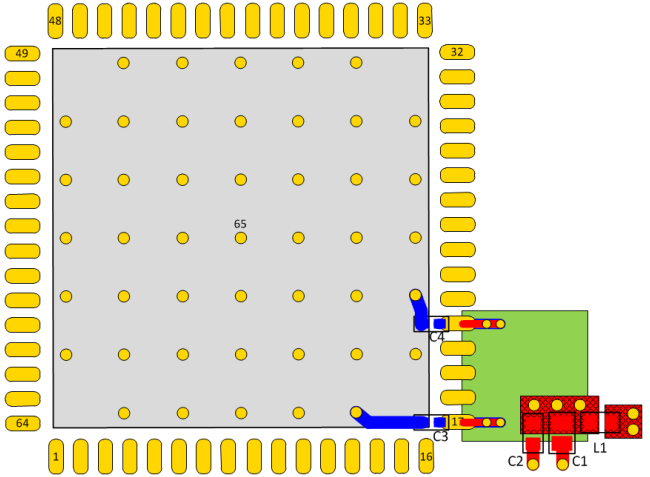






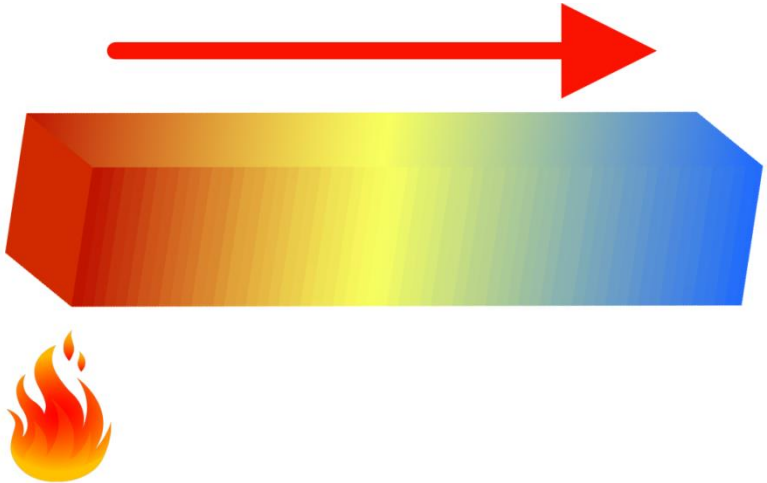
VDD-GND bypass - QFN





- Use low inductance path to VDD and GND planes
  - Via tangent from pin to plane, no trace
  - >1 VDD via if space allows
  - Larger via hole size if space allows
  - Use small physical size low inductance bypass capacitor, 0402 or smaller
  - Bypass capacitors placed on bottom layer sharing DAP GND via array
  - Bypass capacitor via straight to planes, no trace
- Use sandwiched VDD-GND layers to build a good RF bypass capacitor
- Use as small a package as possible for best decoupling performance

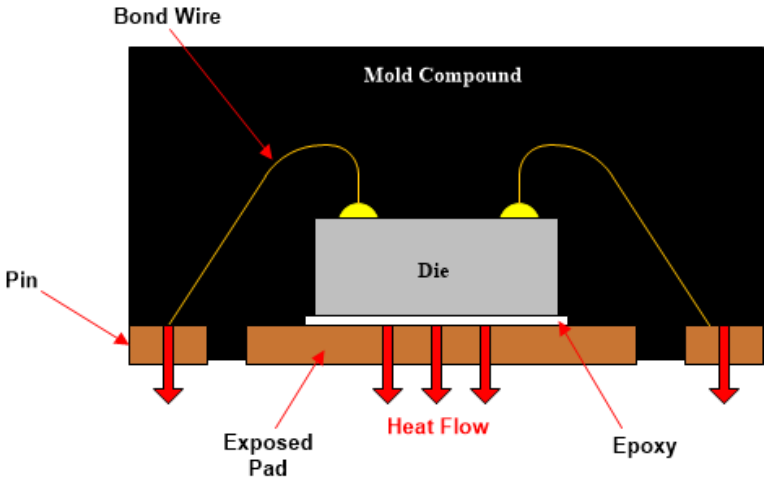
Heat transfer

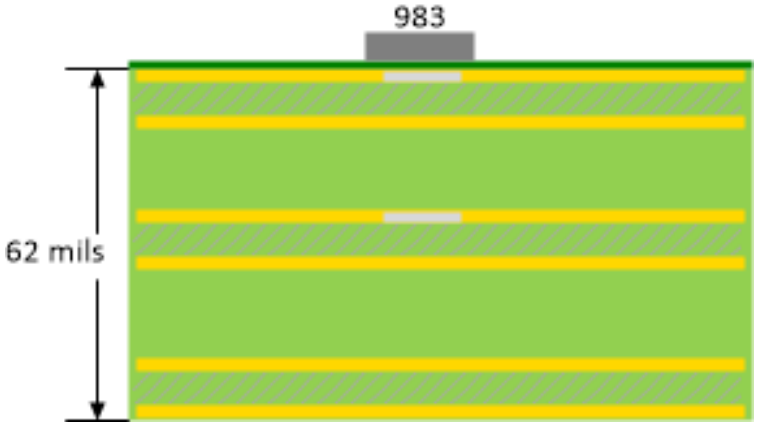


- There are three methods of heat transfer: heat conduction through solids, heat convection through fluids and gases, and heat generated by radiation.
- Heat transfer occurs when there is a temperature difference between two objects or between different areas of an object, and its rate depends on the geometry, thickness, and material of the object.
- Heat transfers from a hotter body to a colder body until the whole system reaches final equilibrium

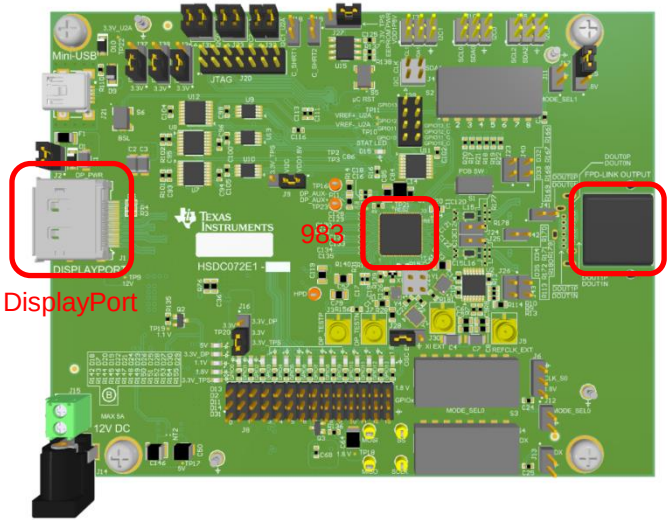
Thermal relief

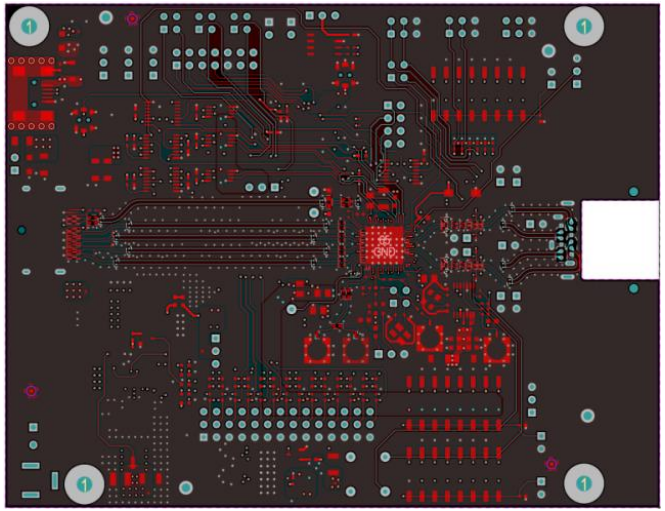
- The Die-attach pad (DAP), if present, provides the most dominant thermal path between the PCB and the die.
- Packages with a DAP, such as QFN package, have a large exposed surface area through which heat can transfer quickly.
- The die and exposed pad glues with non-conductive epoxy where the heat dissipation can quickly extract from the device.
- For fast thermal relief, any unused plane can utilize this by creating equivalent DAP size. It conducts heat from the exposed pad of the package to the PCB ground plane.





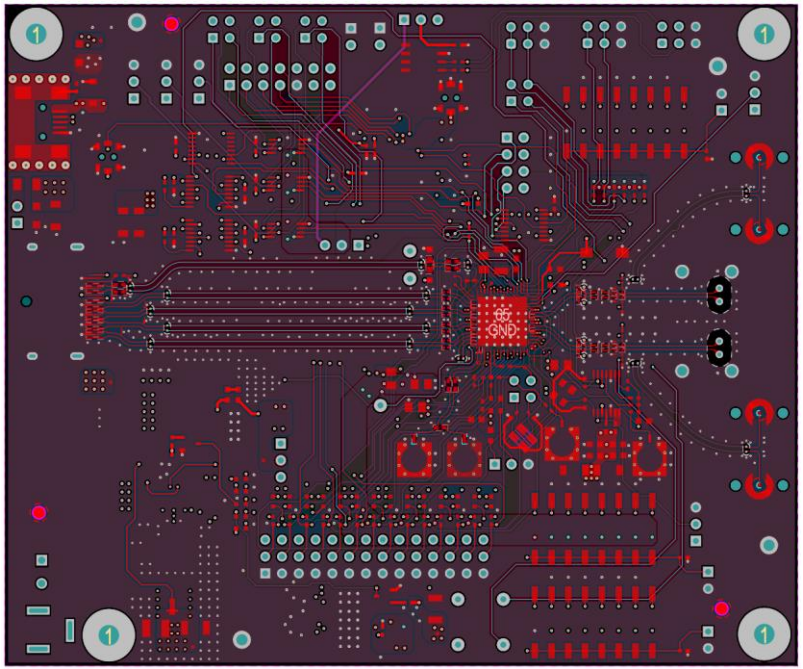
Example layout: DS90Ux9xx-Q1EVM

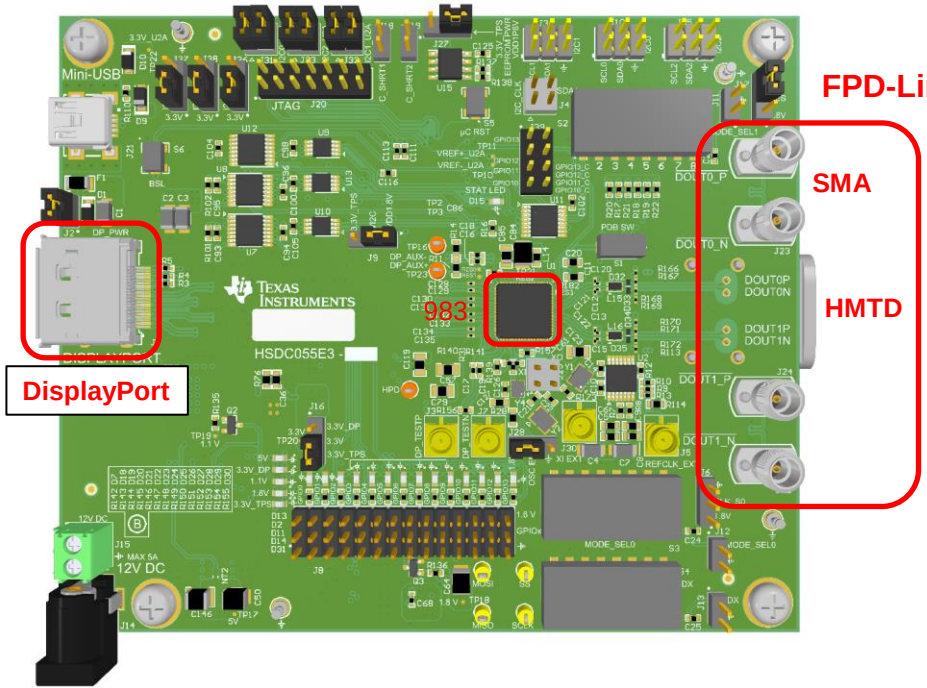




- Runway is kept free from any obstacles that might impede high speed signal path
- Place FPD-Link IV output signals as close as possible to the output connector

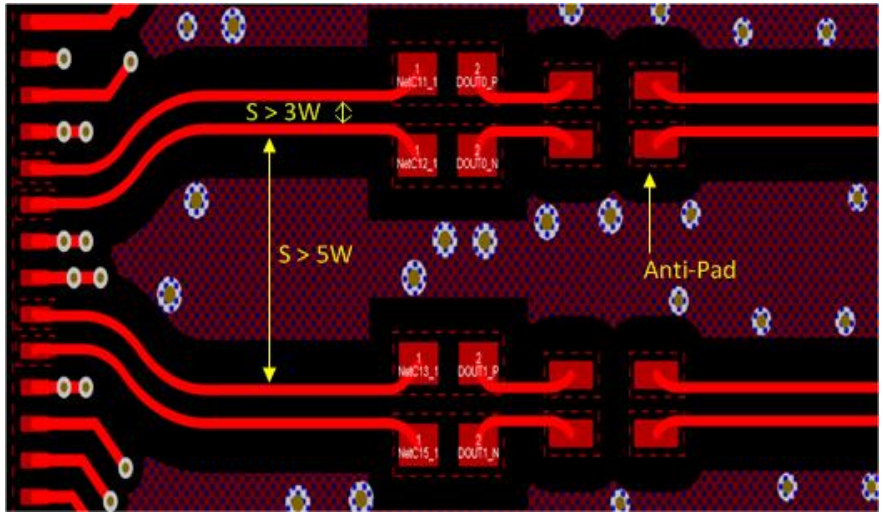
Example layout: DS90Ux9xx-Q1EVM

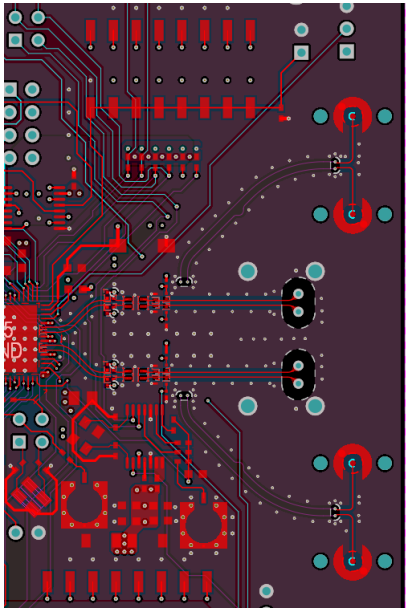




Example layout: DS90Ux9xx-Q1EVM

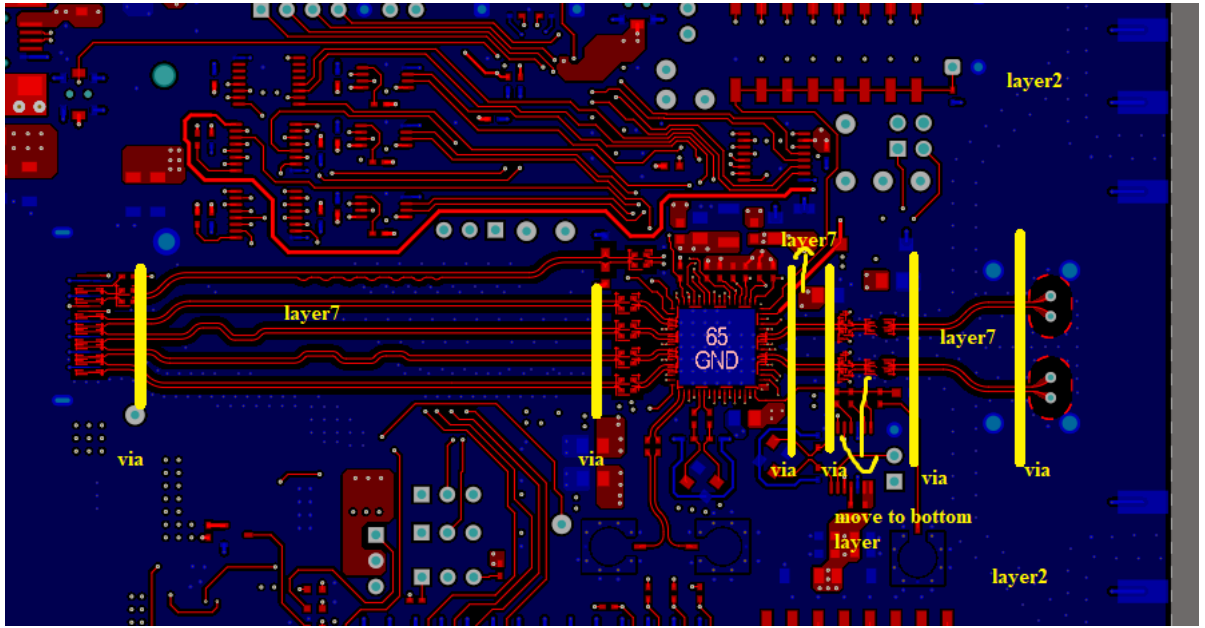
To minimize crosstalk, keep the distance between two traces approximately 2 to 3 times the width of the trace.





Convert microstrip to stripline

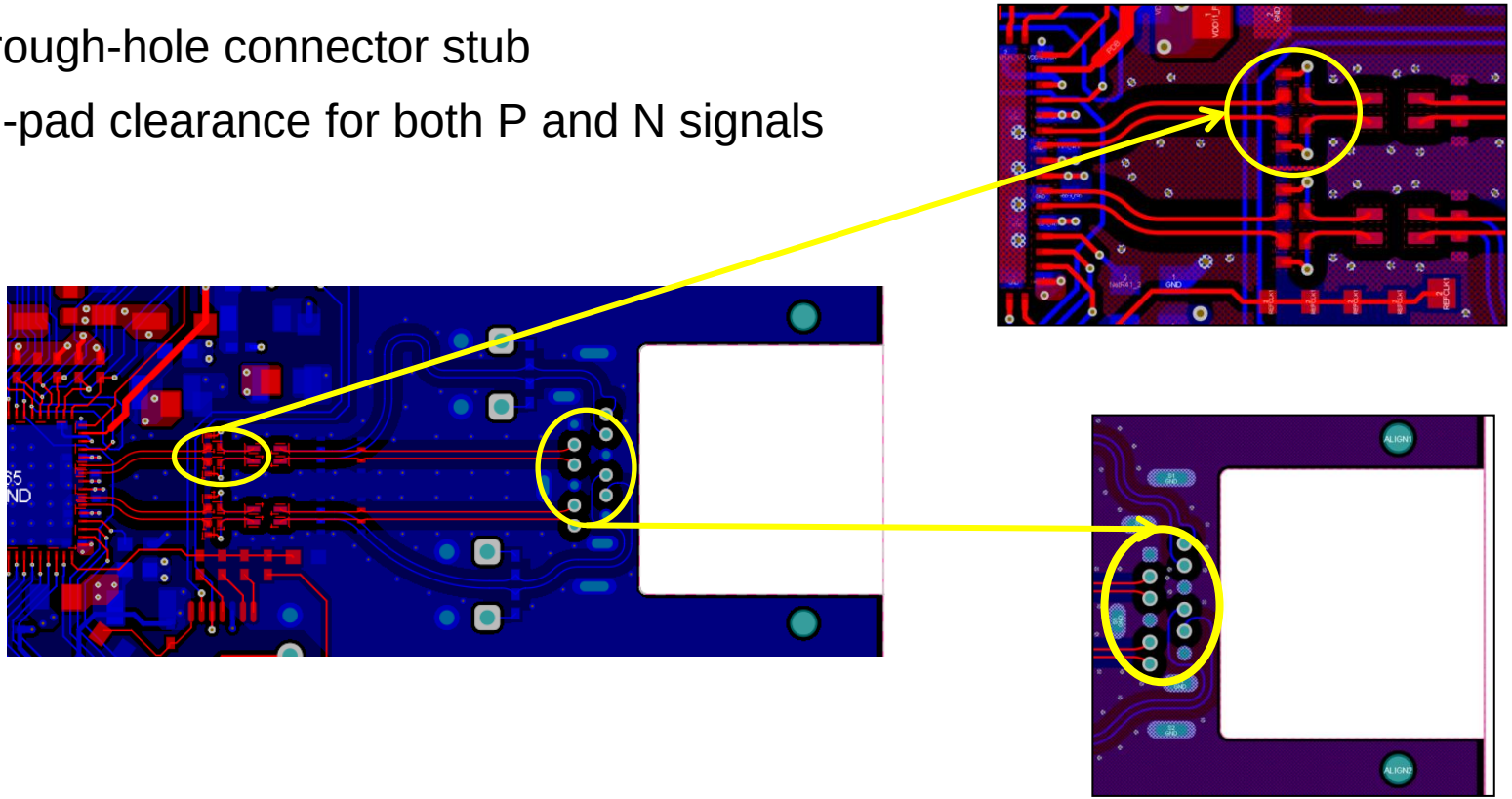
- Requires additional layers
- Introduce more vias



FPD-Link IV output connector layout

recommendation

- Avoid through-hole connector stub
- Oval anti-pad clearance for both P and N signals



Summary

- FPD-Link™ channel requirements
  - Signaling topologies
  - PCB elements and transmission loss characteristics
  - Key channel parameters
- High speed design
  - Cables and connectors
  - PCB dielectrics
  - Layout considerations
- Please visit training.ti.com for more FPD-Link training information

FPD-Link™ channel training

- FPD-Link parameters & transmission channel module
  - High speed serial link basics
    - https://training.ti.com/high-speed-serial-link-basics
  - Basic transmission parameters
    - https://training.ti.com/basic-transmission-parameters
  - Common connectors and cables for automotive applications
    - https://training.ti.com/common-connectors-and-cables-automotive-applications
  - What you need to know about the transmission channel
    - https://training.ti.com/what-you-need-know-about-transmission-channel
  - In-line and common mode chokes - use and effect on the transmission channel
    - https://training.ti.com/line-and-common-mode-chokes-use-and-effect-transmission-channel
  - Channel specification available from FAE

Questions?

Appendix

Appendix A: FPD-Link Channel Specification

Key Channel Parameters

- ***Characteristic impedance***
  - defines the channel's impedance matching to the termination of the SER and DES.
- ***Impedance mis-match***
  - defines the allowable impedance variations caused by connectors or PCB structures.
- ***Return loss***
  - defines the channel's impedance matching and measures of reflections caused by discontinuities along the full-duplex link. The return loss includes the effect of on-board components.
- ***Insertion loss***
  - is the attenuation of signals; including that of SER-board, cable assembly and DES-board. A longer PCB trace introduces higher insertion loss for the board. The channel's insertion loss should be within the range supported by the SER-DES chipset

Key Channel Parameters (II)

- ***Intra-pair skew***
  - Skew between P- and N- signals within the pair; excessive intra-pair skew affects signal integrity of the DES. A common mode choke placed at the input of the DES reduces the amount of intra-pair skew caused by an un-balanced cable assembly, but also add small amount of insertion loss.
- ***Inter-pair skew/ Cross-talk***
  - defines the maximum allowable lane-to-lane skew for adjacent FPD-Link channels used in a multi- link DES.
  - Excessive crosstalk affects the signal integrity for the SER and DES by reducing the signal-to-noise ratio. Cross-talk appears in a cable with more than one signal lane that share one connector, for example, a HSD STQ cable if both pairs are used for FPD-Link, or four coaxial cables that connect to a quad-mini-FAKRA connector.

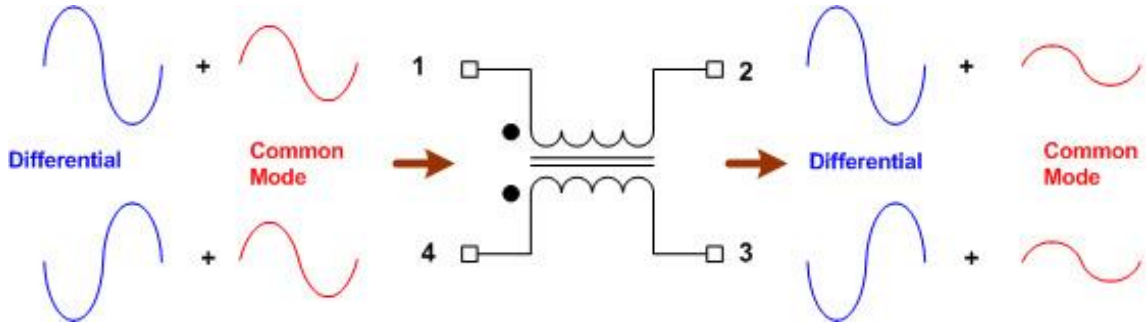
Key Channel Parameters (III)

- ***Aging and Mechanical Stress***
  - Cable assembly dependent. Aging usually introduces increase in insertion loss, while mechanical stress usually manifests as a degradation in the cable's characteristic impedance and return loss.
- ***Shielding Effectiveness***
  - Defines the effectiveness of the shield braid in attenuating EMI radiation or EMC pick-up. Shielding effectiveness is dependent on the braid's density and the connector's contact ground impedance. Contact cable suppliers on shielding effectiveness.

Appendix B: Component Considerations

Common Mode Choke (CMC)

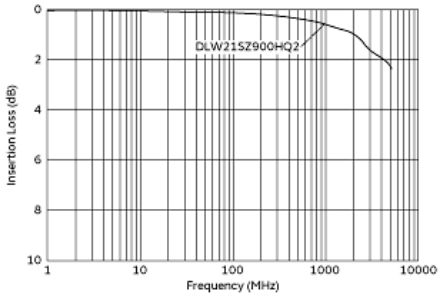
- Common mode choke is a miniature component designed to attenuate common mode signal with small effect on differential signal
- It is used in differential transmitter for EMI mitigation or in a differential receiver for reducing intra-pair skew



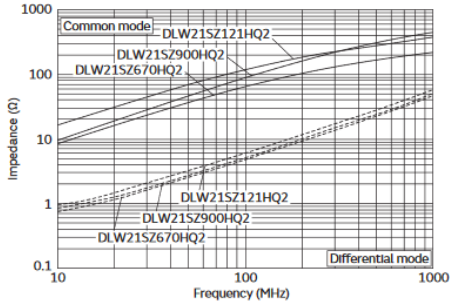
Common Mode Choke Suitability

- Common mode choke adds small amount of insertion loss to the transmission channel
- Choose a common mode choke with
  - Smallest differential insertion loss at the Nyquist frequency of the forward channel transmission
  - Good differential return loss
  - High common mode attenuation
  - 98xEVM used DLW21SZ900HQ2

Footprint	0805 Footprint
DCR	0.25 ohms
Current Rating	400 mA
Temp Rating	-40°C to +105°C
Cutoff Frequency	10 GHz



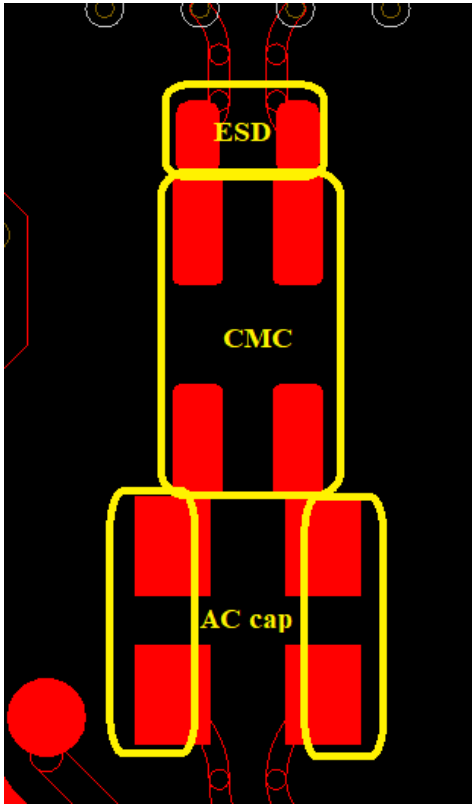
Differential Insertion Loss



Impedance Characteristic

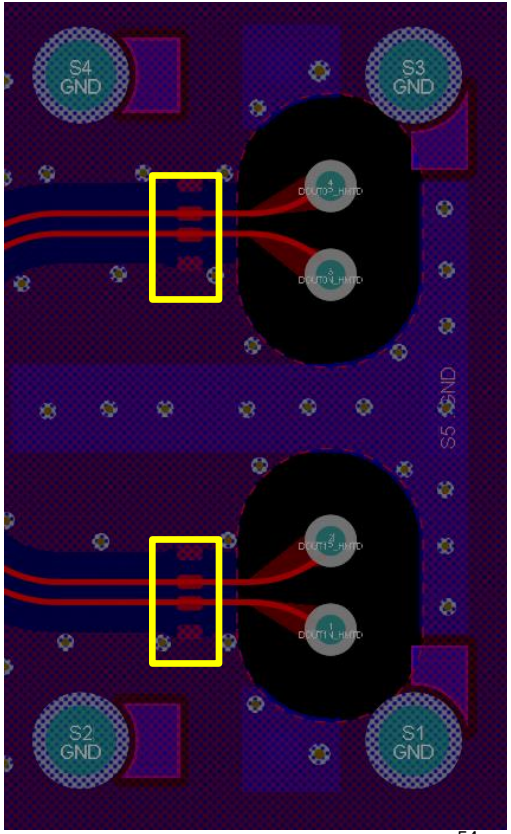
Common Mode Choke (DLW21SZ900HQ2)

- Eliminate any unwanted noise interference
- Prevents the interference from affecting the required high speed signal
- Suppress noise reduction
- Minimize the effect of any mismatch impedance
- Designed to correct line impedance when ESD protection diode is used



ESD Protection Diode Layout

- To support 13.5Gbps the capacitance of the ESD device must be lower than 0.30pF for optimal performance
- Both ESD devices mentioned have lower capacitances
  - TPD1E01B04
  - TPD1E0B04
- ESD protection diode as close as possible to the connector
- Create anti-pad clearance underneath the layer



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