Designing for low distortion with high-speed op amps

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Introduction

The output of any amplifier contains the desired signal and unwanted signals. Noise is one unwanted output that is generated internally by the amplifier's components or is coupled in from external sources like the power supply or nearby circuitry. Distortion is another unwanted output that is generated when the amplifier's transfer function is non-linear.

In the formula of a straight line, y = b + mx, non-linearity refers to any deviation the output (y) may have from a constant multiple (m) of the input (x) plus any constant offset (b).

Many high-speed op amps use bipolar transistors as the basic active element to amplify the signal. In bipolar transistors, junction capacitances are a function of voltage, current gain is a function of collector current, collector current is influenced by collector-to-emitter voltage, transconductances are typically exponential functions, and so on. These all cause non-linear transfer functions.

When a transistor is driven into saturation or cut-off, it exhibits strong non-linearity. In this article, it is assumed that the devices are being operated below their saturation limits in what is typically referred to as linear operation.

Power series expansion

Expanding the non-linear transfer functions of basic transistor circuits into a power series is a typical way to quantify distortion products.[1] For example: assume a circuit has an exponential transfer function $y = e^x$, where x is the input and y is the output. Expanding e^x into a power series around x = 0 results in

$$e^x = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} + \frac{x^5}{120} + \cdots + \frac{x^n}{n!}.$$

Figure 1 shows the function $y = e^x$ along with estimates that use progressively more terms of the power series.

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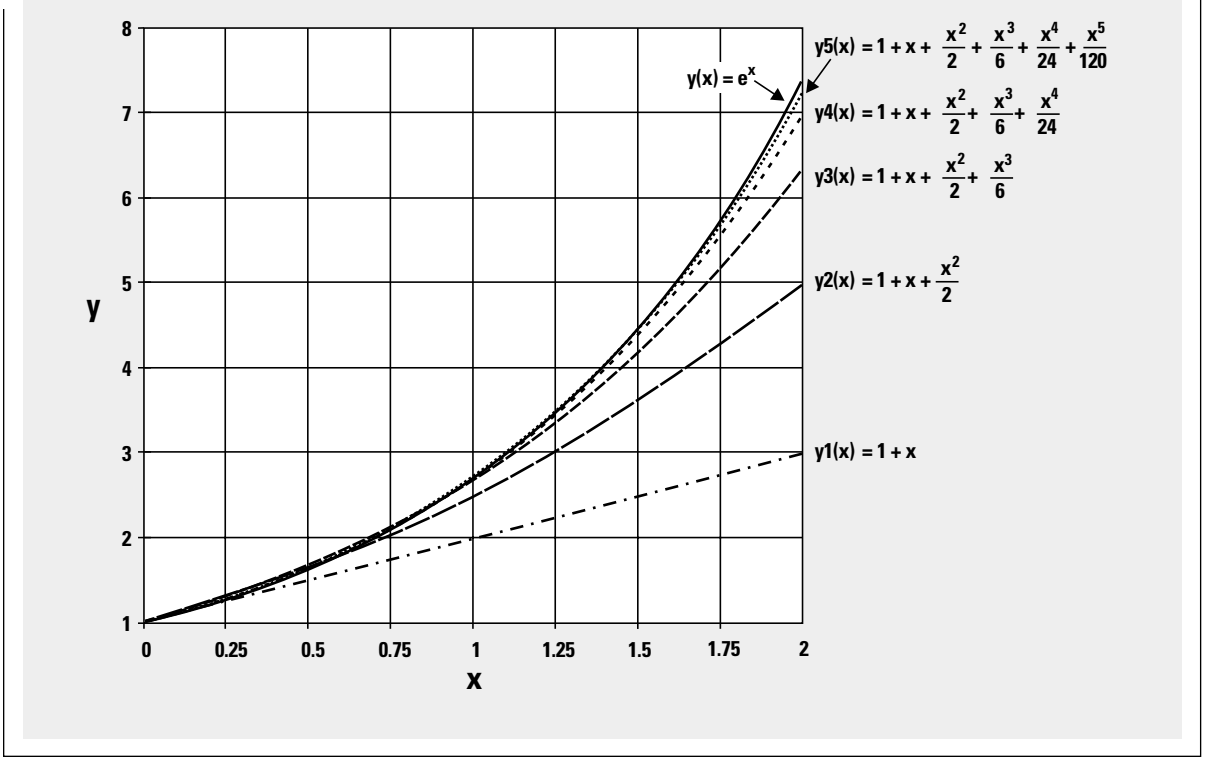
Figure 1. Function $y = e^x$ and its power series estimates



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The farther x is from 0, the more terms are required to properly estimate the value of e^x. If $x < 0.25$, then the linear term, $1 + x$, provides a close estimate of the actual function; and the circuit is linear. As x becomes larger, progressively more terms are required to properly estimate e^x, and the output now contains second-order, third-order, and higher distortion terms.

If the input to this circuit is a sinusoid, $x = \sin(\omega t)$, then trigonometric identities* show that the quadratic, cubic, and higher-order terms give rise to second-, third-, and higher-order harmonic distortion. In a similar manner,[2] if the input is comprised of two tones, then trigonometric identities show that the quadratic and cubic terms give rise to second-, third-, and higher-order intermodulation distortion.

Simplified op amp schematic

A simplified schematic of a high-speed op amp is shown in Figure 2. A simple feedback network and load resistor are included for completeness. A brief overview of its operation is given first for those unfamiliar with op amp circuit design.

$V_{CC}+$ is the positive power supply input, and $V_{CC}–$ is the negative power supply input. $V_{IN}+$ and $V_{IN}–$ are the signal input pins, and V_{OUT} is the signal output. The op amp amplifies the differential voltage across its input pins to generate the output. By convention, the input voltage is the difference voltage, $V_{ID} = (V_{IN}+) – (V_{IN}–)$. It is amplified by the open-loop gain of the amplifier to produce the output voltage, $V_{OUT} = A_f V_{ID}$, where A_f is the frequency-dependent open-loop gain of the amplifier.

The input differential pair, Q1 and Q2, is balanced so the collector currents, I_{C1} and I_{C2}, are equal when the input differential voltage is zero. Applying a voltage across the input pins causes $I_{C1} \neq I_{C2}$.

Q3 and Q4 fold the current from the input differential pair into the Wilson current mirror formed by Q5, Q6, and Q7. The mirror tries to maintain equal collector currents. Any difference current, $I_{C1} – I_{C2}$, develops a voltage at V_{MID}.

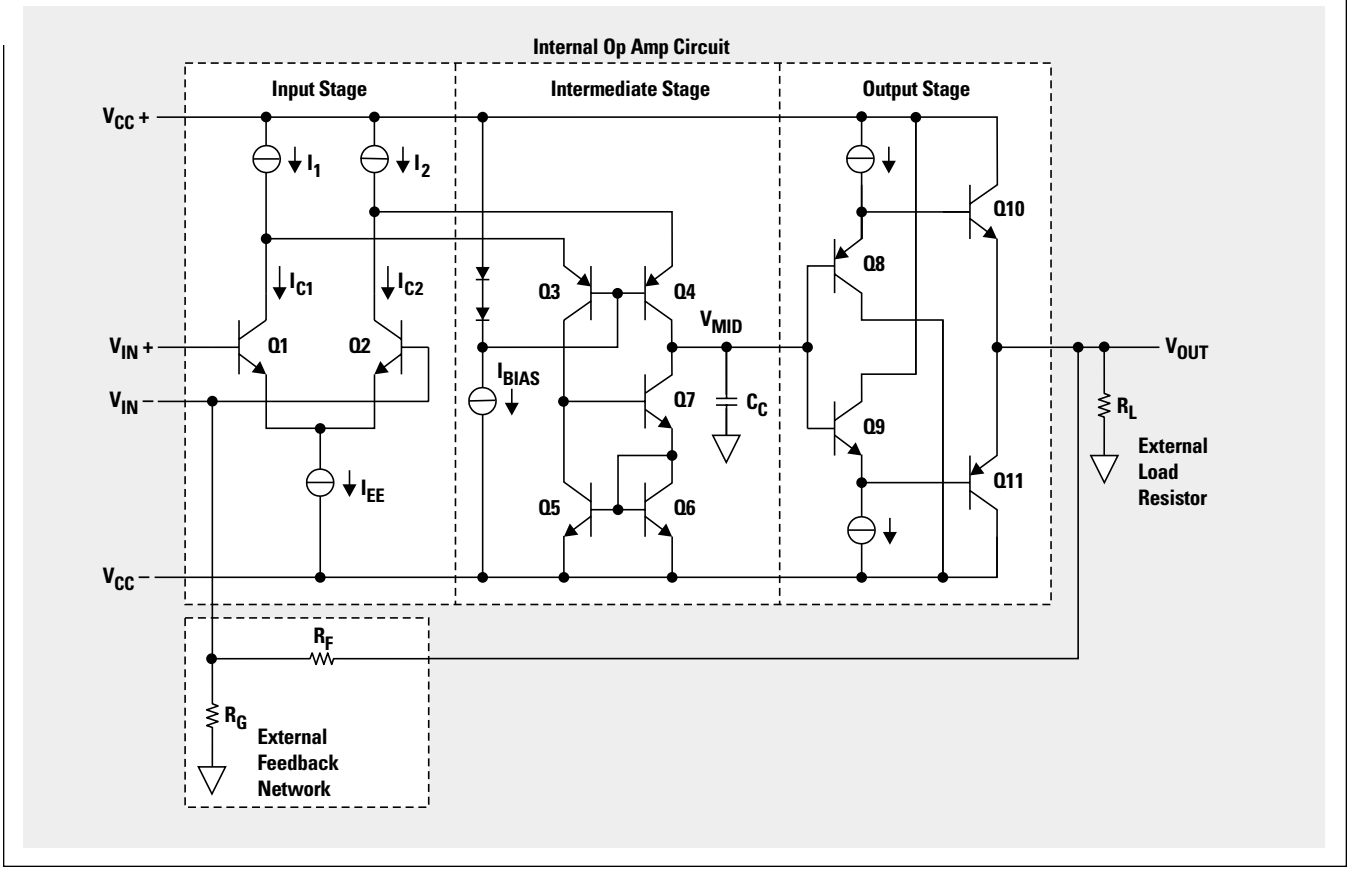
The capacitor, C_C, shown from V_{MID} to ground, is really multiple capacitors to the supply rails. It is used to stabilize the amplifier via dominant pole compensation.

V_{MID} is then buffered to the output via Q8 and Q10, or via Q9 and Q11, depending on polarity.

In the following discussion, we will examine the distortion mechanisms in each of these sub-circuits more closely.

*$\sin^2(\omega t) = \frac{1-\cos(2\omega t)}{2}$ and $\sin^3(\omega t) = \frac{3\sin(\omega t)-\sin(3\omega t)}{4}$

Figure 2. Simplified high-speed op amp schematic



Intrinsic linearity

Intrinsic linearity refers to the linearity of each sub-circuit without the effect of feedback.

The input stage

The transfer function of the input differential pair is given in many texts.[3, 4] The input is the differential voltage, $V_{ID} = (V_{IN}+) - (V_{IN}-)$, and the output is the difference current, $I_{C1} - I_{C2}$, which is proportional to

$$\tanh\left(\frac{-V_{ID}}{2\times V_T}\right),$$

where V_T is the thermal voltage ($V_T \approx 26$ mV @ 25°C). Substituting

$$x = \frac{-V_{ID}}{2\times V_T}$$

and expanding tanh(x) around x = 0 in a power series, we find

$$\tanh(x) = x - \frac{x^3}{3} + \frac{2x^5}{15} - \cdots.$$

Since the power series contains no even-order terms, a perfect differential pair will not generate even-order harmonics. Figure 3 shows three estimates of y(x) = tanh(x), each using progressively more terms in the power series.

If $x < 0.25$, which corresponds to $V_{ID} < 0.5\ V_T$, the function is approximately linear; i.e., y1(x) = x. Under that condition, the input stage is very linear. With larger excursions, third- and fifth-order terms are required for an adequate approximation, and the input stage will distort the signal.

A typical high-speed op amp, without degeneration,** has a very large open-loop gain—on the order of 100 dB. Very small input voltages are required to keep the output from saturating. V_{ID} is normally much less than V_T, and the input stage is normally considered linear. For example: Assume that the output voltage swing is 10 V, with 100 dB of gain V_{ID} = 0.1 mV, which is much less than 0.5 $V_T \approx 13$ mV @ 25°C.

The intermediate stage

The difference current, $I_{C1} - I_{C2}$, from the input stage is the input to the intermediate stage; and the output is the voltage at V_{MID}. The voltage swing at V_{MID} in conjunction with the early voltages, V_A, and collector capacitances, C_J, of Q4 and Q7 causes non-linear behavior in the stage. The other transistors in the intermediate stage see very small voltage and current variations, and do not play a major role in distortion.

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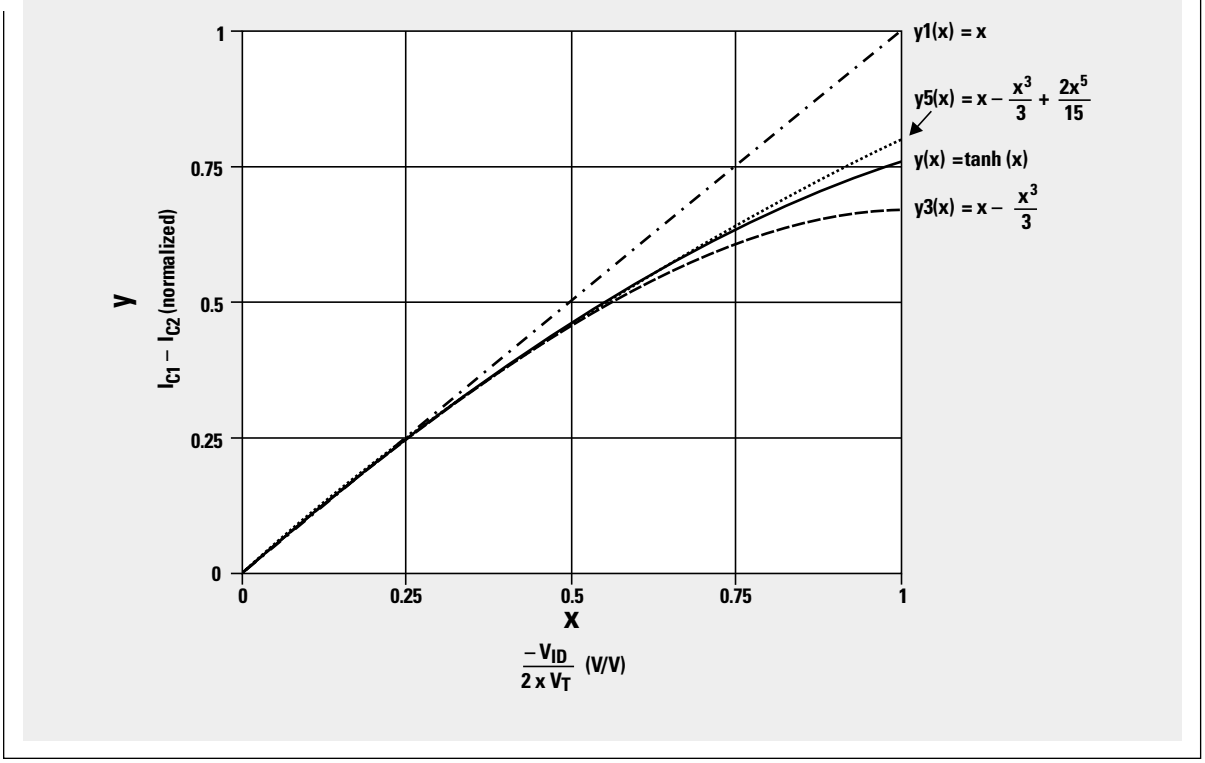
**Often emitter degeneration is used as part of the overall compensation scheme, where resistors are placed in the emitter leads of Q1 and Q2. This increases the linear input voltage range by reducing the gain.

Figure 3. Power series estimates of input pair transfer function



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Early voltage effects

V_A appears in the formula for a transistor's collector current:[3]

$$I_C = I_S \times \exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE}}{V_A}\right),$$

where V_{BE} is the base emitter voltage, V_T is the thermal voltage, V_{CE} is the collector-to-emitter voltage, and I_S is the saturation current.

I_C comprises the input to the intermediate stage, and V_{CE} the output. Assuming that

$$I_S \times \exp\left(\frac{V_{BE}}{V_T}\right)$$

is linear should be valid, considering the previous discussion about the linearity of the input stage. As such, we can write a generalized formula for the intermediate stage: $y = zx(1+\alpha y)$, where y is V_{MID}, z is the impedance of the stage, x is the input current, and α depends on V_A. Rearranging gives us

$$y = \frac{zx}{1-zx\alpha}.$$

Using conservative numbers such as $z = 10^6$ and $\alpha = 100$, the power series expansion around x = 0 is: $10^6x + 10^{10}x^2 + 10^{14}x^3 + 10^{18}x^4 + 10^{22}x^5$ .... Figure 4 shows three estimates, each using progressively more terms in the power series—linear, quadratic, and cubic.

It can be seen that with voltage swings up to 4 V at V_{MID}, the linear term 10^6x is a close approximation, and it is expected that the transfer function is linear within these limits. At higher excursions, between 4 V and 12 V, the quadratic terms are required, resulting in second-order distortion products. Above 12 V, the cubic terms are required, giving rise to third-order distortion products.

Limiting voltage swings at V_{MID} reduces distortion due to the non-linear effects of V_A.

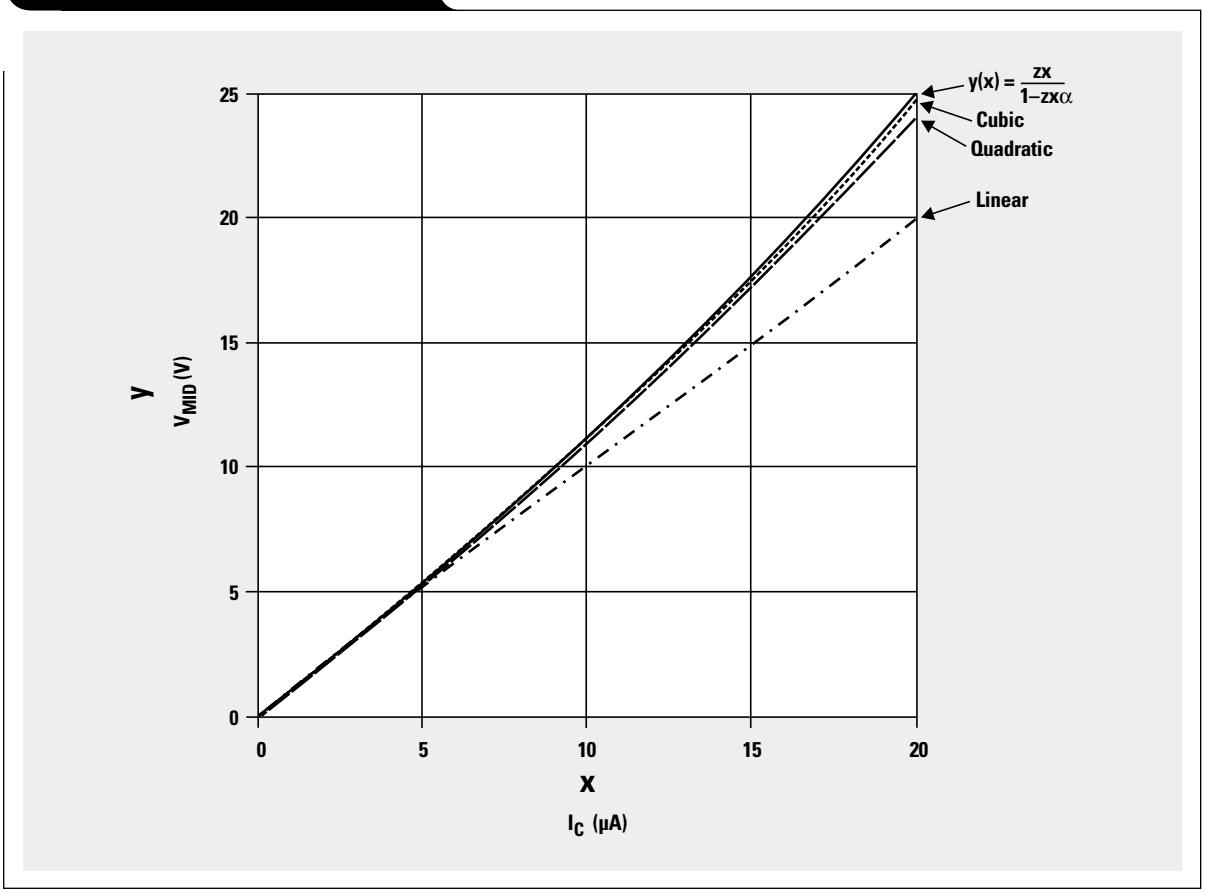
Junction capacitance effects

A simple model of junction capacitance[3] is given by the formula

$$C_J = \frac{C_O}{\sqrt[MJE]{1-\frac{V_J}{\psi_0}}},$$

where C_O is the zero-bias capacitance, V_J is the junction voltage, ψ_0 is the built-in potential, and MJE is the grading coefficient. The transfer function of the intermediate stage is influenced by this non-linear capacitance at V_{MID}.

Figure 4. Non-linear effect of V_A



Using $I_{C1} - I_{C2} = x$ and $V_{MID} = y$, we can write

$$y = x\left[Z \parallel \frac{1}{\omega\left(C_C + \frac{2\times C_O}{\sqrt[MJE]{1-\frac{y}{\psi_0}}}\right)}\right],$$

where Z is the linear, non-frequency-dependent impedance seen looking in the node V_{MID}; C_C is the dominant pole capacitor, and ω is the frequency in radians. At frequencies above the dominant pole, this can be simplified to

$$y = \frac{x}{\omega\left(C_C + \frac{2\times C_O}{\sqrt[MJE]{1-\frac{y}{\psi_0}}}\right)}.$$

With this equation, y cannot be solved for in closed form.

By looking at the impedance and taking y as the independent variable, we can write

$$Z_C(\omega) = \frac{1}{\omega\left(C_C + \frac{2\times C_O}{\sqrt[MJE]{1-\frac{y}{\psi_0}}}\right)}.$$

Typical numbers for TI's high-speed BiCom 1 process include: MJE = 3, $\psi_0 = 0.6$, $C_O = 200$ pF, and $C_C = 5$ pF. Using these values and setting $\omega = 10^6$, we can draw the plot shown in Figure 5. Again, power series estimates are shown that use progressively more terms of the series—linear, quadratic, and cubic.

With voltage swings of about 3 V_{PP}, the linear approximation is valid. At higher voltage swings, the quadratic and cubic terms are required, resulting in second- and third-order distortion products.

The effect of V_A is not frequency-dependent, but the effect of C_J is. Below the dominant pole of the amplifier, V_A dominates the non-linearity of the intermediate stage. Above the dominant pole, the non-linearity is a combination of the two. In either case, limiting the voltage swing at V_{MID} (and thus V_{OUT}) is the key to linear operation.

The output stage—Q8 through Q11

Q8 through Q11 form a double-buffered, class-AB output stage. The voltage at V_{MID} is buffered via these transistors to produce V_{OUT}. Depending on polarity, the signal path is either through Q8 and Q10, or through Q9 and Q11. The analysis is the same in either case. If we assume that the polarity is positive,

$$V_{OUT} = V_{MID} + V_{BE_{Q8}} - V_{BE_{Q10}}$$
$$= V_{MID} + V_T \times \ln\left(\frac{I_{C_8}}{I_{S_8}}\right) - V_T \times \ln\left(\frac{I_{C_{10}}}{I_{S_{10}}}\right).$$

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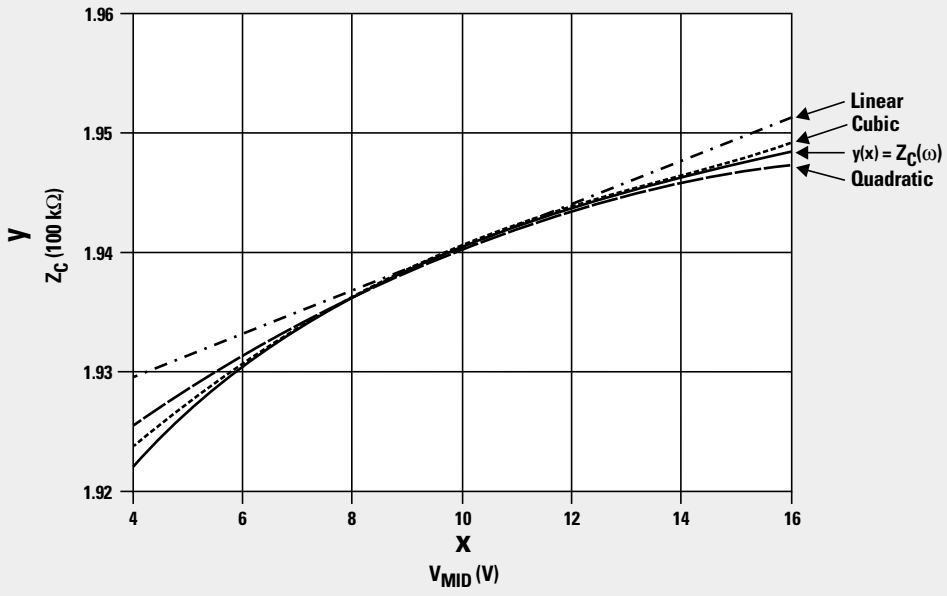
Figure 5. Non-linear C_J



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Q10 will see variations in collector current as it delivers power to the output load. Variations in Q8's collector current are reduced by the beta of Q10, resulting in $V_{BE_{Q10}}$ being the dominant non-linearity in the signal path from V_{MID} to V_{OUT}.

Again, using a power series expansion helps to highlight the nonlinear terms responsible for distortion. If we substitute

$$\frac{I_C}{I_S} = x$$

and expand the natural log function around the point x = a in a power series,

$$\ln(x) = \ln(a) + \frac{x-a}{a} - \frac{(x-a)^2}{2a^2} + \frac{(x-a)^3}{3a^3} + \cdots.$$

Figure 6, which uses typical numbers for V_{BE} = 0.6 V, shows three estimates that each use progressively more terms in the power series—linear, quadratic, and cubic.

Variations of 20% or more in collector current cause the output stage to become non-linear. Increasing the amplifier's load impedance reduces the current variations in the output transistors and helps to reduce distortion in the output stage.

A typical scenario may be an output stage that is designed for a quiescent bias current of 5 mA and can deliver up to 100 mA to the load—a 1:20 ratio. Under these circumstances, distortion in the output stage will dominate the intrinsic distortion of the amplifier.

Power-supply bypass capacitors

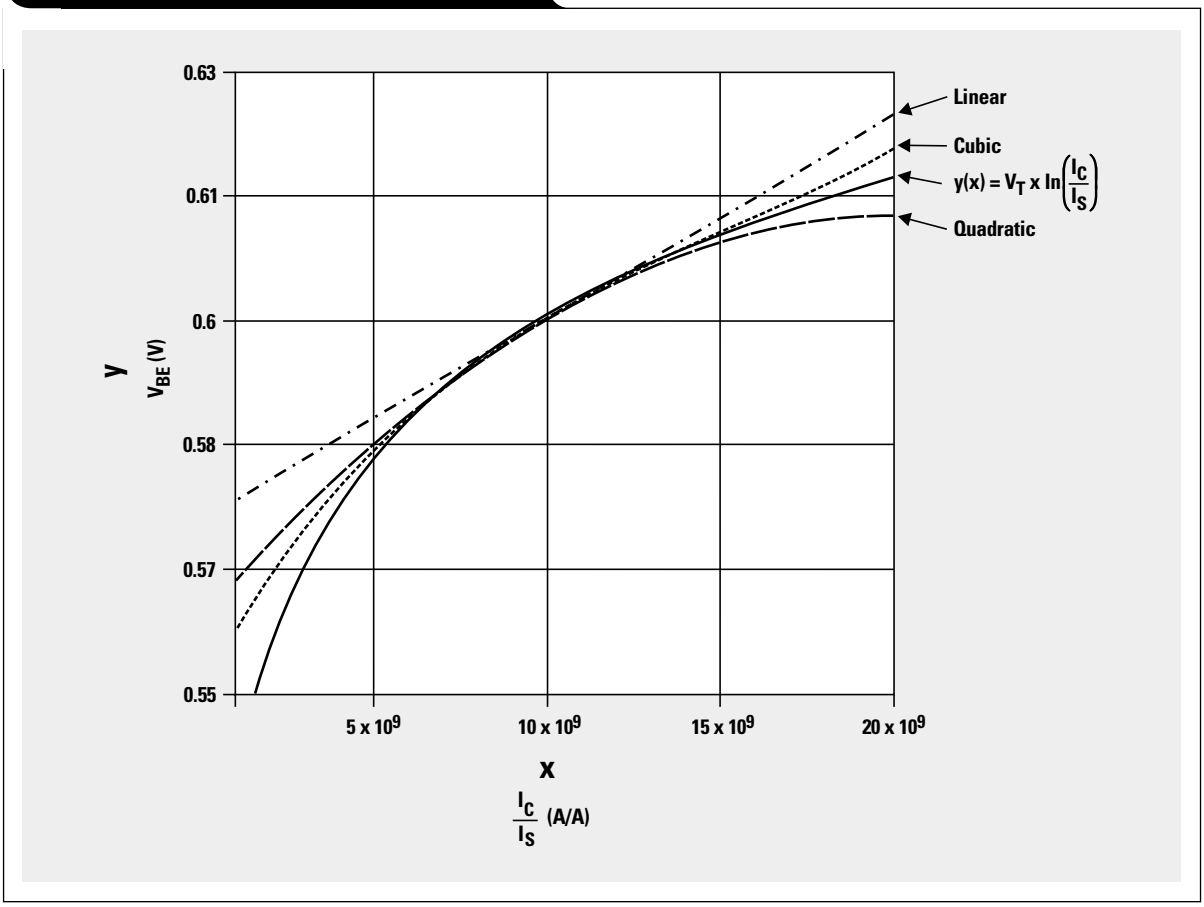
Figure 7 illustrates power-supply bypassing for a high-speed op amp. Current ($I_{CC}\pm$) supplied to the op amp from the power supply must pass through the distributed impedance between the power supply and the op amp. The distributed impedance is due to parasitic resistance and inductance in series with the power supply, and to stray capacitance to the ground plane. Due to the distributed impedance, bypass capacitors are required for high-speed operation.

The voltage drop across the resistance is negligible because the resistance is typically very small; but when the amplifier is required to output a fast rising (or falling) waveform, the series inductance can cause significant voltage drop:

$$V = L\frac{di}{dt}.$$

So what does this have to do with distortion? The voltage drop between V± and $V_{CC}\pm$ reduces the voltage across

Figure 6. Power series expansion of V_{BE}



the op amp, and the transistor operation moves towards saturation, causing significant distortion.

Bypass capacitors provide a local reservoir of energy used to support fast-rising transients, avoid dips in $V_{CC}\pm$, and keep the transistors out of saturation. The strategy shown uses bulk capacitors (typically 6.8 µF to 10 µF tantalum) within 1 inch of the power pins, along with high-frequency capacitors (0.01 µF to 0.1 µF ceramic) within 0.1 inch of the power pins.

The bulk capacitors store more energy but tend to have larger parasitic inductance and equivalent series resistance. For this reason, they can only provide energy at low frequencies. Due to the relaxed requirements for placement on the board, they are typically shared between several devices.

The high-frequency capacitors have lower inductance and equivalent series resistance, and are capable of supplying very fast di/dt. They are located as close as physically possible to the op amp power pins.

Using differential amplification to reduce even-order distortion

Differential signaling has been commonly used in audio, data transmission, and telephone systems for many years because of its inherent resistance to external noise sources. Today, differential signaling is becoming popular in high-speed data acquisition, where the analog-to-digital converter's (ADC's) inputs are differential and a differential amplifier is needed to properly drive them.

Another attractive advantage to differential signaling is that it significantly reduces even-order harmonics. This is easy to see by using a generic power series expansion of the output voltage.

A differential amplifier has two outputs that are ideally 180° out of phase: $(V_{OUT}+) = -(V_{OUT}-)$. The output is the differential voltage: $V_{OUT} = (V_{OUT}+) - (V_{OUT}-)$. If we assume that the amplifier is perfectly balanced, the generic expansion of each output is

$$(V_{OUT}+) = K_1(V_{IN}) + K_2(V_{IN})^2 + K_3(V_{IN})^3 + K_4(V_{IN})^4 + K_5(V_{IN})^5 \ldots$$

and

$$(V_{OUT}-) = K_1(-V_{IN}) + K_2(-V_{IN})^2 + K_3(-V_{IN})^3 + K_4(-V_{IN})^4 + K_5(-V_{IN})^5 \ldots,$$

where K_1 through K_5 are constants that depend on the characteristics of the amplifier. The odd-order terms retain their original polarity, but the even-order terms are always positive. Since V_{OUT} is the difference, the even-order terms cancel, but the odd-order terms increase by a factor of two:

$$V_{OUT} = 2K_1V_{IN} + 2K_3V_{IN}^3 + 2K_5V_{IN}^5 \ldots.$$

Balance is very important. Any imbalance in the two amplification paths will compromise the cancellation of even-order terms. Symmetrical layout and matched amplifiers are required.

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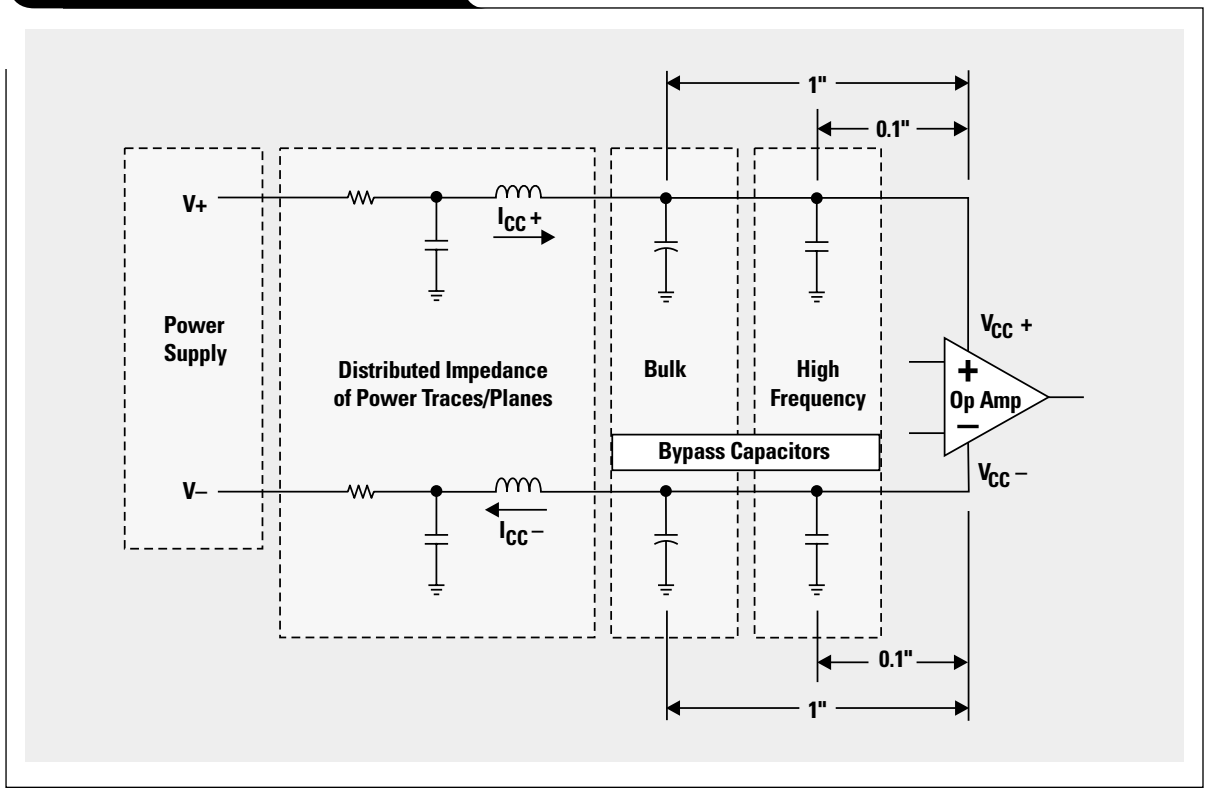
Figure 7. Power-supply bypassing



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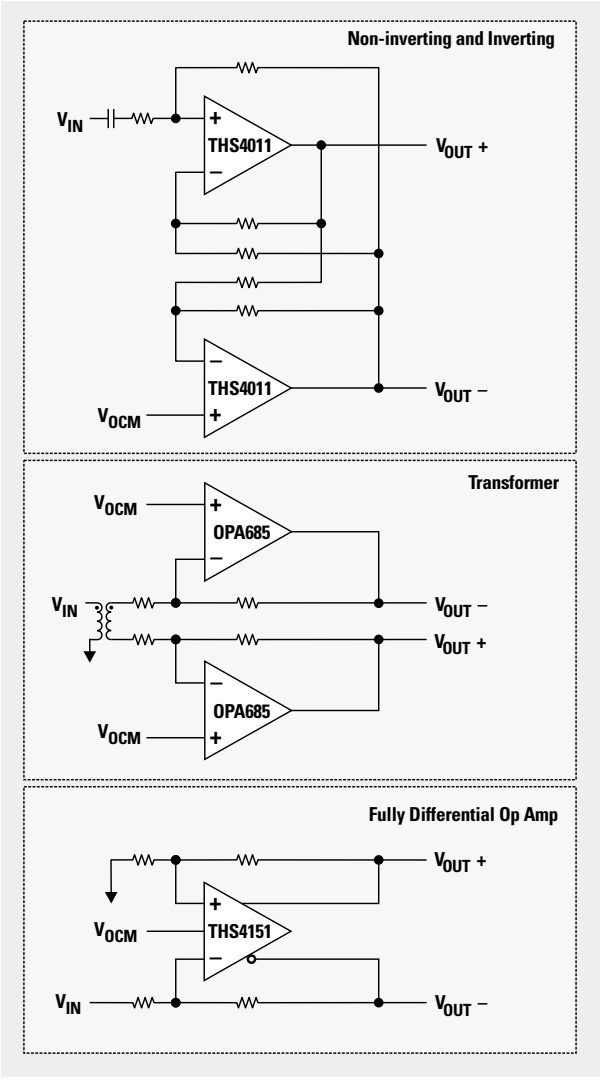
There are many ways to convert single-ended signals to differential signals, as shown in Figure 8. Some employ the use of transformers, multiple single-ended op amps, and various passive components. Integrated fully differential op amps are available that can provide a more elegant solution.

The curative effects of feedback

The curative effects of negative feedback refers to the effectiveness of negative feedback in reducing distortion. This effectiveness depends on the forward gain from the point where distortion is generated and the loop gain of the amplifier.

Figure 9 shows a block diagram of an op amp using negative feedback. The input stage is A1, the intermediate stage is A2, the output stage is the x1 buffer, and β is the feedback factor. The open-loop gain or forward gain of the amplifier is A_F = A1A2; the loop gain is $A_F\beta$ = A1A2β; and e1, e2, and e3 are generalized error sources. The following discussion analyzes the output response that is due to the individual error sources.

Figure 8. Single-ended to differential—alternative methods



An error source at the input stage, e1, is amplified by the full open-loop gain of the amplifier. If there is no feedback, setting all other sources to zero results in V_{OUT} = e1A1A2; but with feedback,

$$V_{OUT} = \frac{e1}{\beta + \frac{1}{A1A2}} \approx \frac{e1}{\beta}$$

if A1A2 >> 1. This means that e1 will be amplified by the closed-loop gain of the amplifier.

An error source at the intermediate stage, e2, is amplified only by A2. If there is no feedback, setting all other sources to zero results in V_{OUT} = e2A2; but with feedback,

$$V_{OUT} = \frac{e2}{A1\beta + \frac{1}{A2}} \approx \frac{e2}{A1\beta}$$

if A2 >> 1. Error source e2 is attenuated by A1β.

An error source at the output stage, e3, is buffered by a gain of +1 to the output. If there is no feedback, setting all other sources to zero results in V_{OUT} = e3; but with feedback,

$$V_{OUT} = \frac{e3}{1 + A1A2\beta} \approx 0$$

if A1A2β >> 1. Error source e3 is attenuated by the loop gain, A1A2β = $A_F\beta$.

Distortion in a high-speed op amp is attributed mainly to the intermediate and output stages. Distortion is reduced by taking advantage of the effect of loop gain in negative feedback. However, be aware that, in a voltage-feedback (VFB) op amp, loop gain decreases linearly with frequency, and so does its effects on reducing distortion.

Design guidelines for low distortion

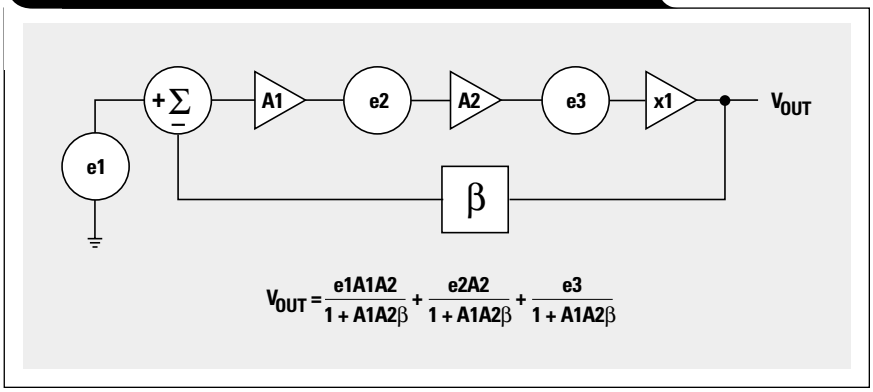
How does one go about designing for low distortion with high-speed op amps? The following are important design considerations.

Op amp selection

1. Look for an amplifier with low intrinsic distortion, high open-loop gain at the frequencies of operation, and high slew rate.
2. For VFB op amps, gain bandwidth (GBW) products in the gigahertz range may be required to provide enough loop gain to reduce distortion significantly in the range of 10 MHz to 100 MHz.
3. Current feedback (CFB) op amps have much higher slew rates than VFB op amps. If the output cannot track the input because of slew rate limitations, the effectiveness of negative feedback is null and void. For this reason, CFB op amps can provide lower distortion in high-frequency applications.
4. For high-gain applications, use decompensated op amps. Decompensated op amps sacrifice stability at lower gain for higher GBW, higher slew rate, and lower noise. They are easily spotted in data books and selection guides by their minimum gain requirements.

5. CFB op amps allow you to optimize loop gain by selecting the feedback resistor value based on the closed-loop gain of the amplifier. At higher gains, lower-feedback resistors can be used without sacrificing stability.[5]

Figure 9. Model of op amp with negative feedback



Circuit design

1. Reduce loading on the amplifier output as much as possible. A common practice when driving an ADC is to make a simple RC filter by placing a small series resistor and load capacitor to ground (or differentially). At the pole frequency, the impedance of the capacitor equals the resistor and the amplifier sees a significant load. Avoid loading the amplifier by using an active filter topology (like MFB, Sallen-Key, or simply a capacitor in parallel with the feedback resistor) to make the amplifier's gain roll off before the pole frequency of the output RC.
2. Use power-supply bypass capacitors. Place bulk capacitors in the range of 6.8 µF to 10 µF within 1 inch of the power pins, and high-frequency capacitors in the range of 0.01 µF to 0.1 µF within 0.1 inch of the power pins. Bulk capacitors typically have been tantalum, but high-value ceramics that may be viable are now available. High-frequency bypass capacitors are normally ceramic.
3. Minimize output voltage swings.
4. Minimize gains. Lower closed-loop gain = higher loop gain.
5. Fully differential architectures help reduce even-order distortion products and are resistant to extraneous common-mode noise sources. Most high-speed ADCs now use differential inputs, and differential amplification is commonly required. Integrated fully differential amplifiers can provide a viable solution.
6. The feedback path is critical. High-speed op amps are very susceptible to the effects of parasitic capacitance. Remove ground plane(s) from under the input pins and any traces leading to them, and use minimum-value feedback resistors. The idea is to avoid creating RC phase lags that decrease the amplifier's phase margin. The resulting peaking and group delay may cause distortion of non-sinusoidal signals.

Conclusion

We have looked at each stage of a simplified high-speed op amp and quantified the main distortion mechanisms. Most of the distortion is produced by the intermediate stage and the output stage due to their dynamic nature.

Reducing the voltage swings at the output and increasing the impedance of external loads will increase the intrinsic linearity of the amplifier. Higher loop gain increases the curative effects of negative feedback.

As frequency increases, the effects of nonlinear parasitic junction capacitance increase, and the curative effects of loop gain diminish. These combine to make distortion more problematic as frequency increases.

Choosing the right amplifier is key. High slew rate and high GBW are two important parameters. CFB op amps can provide for lower distortion, especially at high frequency.

Differential amplification reduces even-order harmonics and is important in driving high-speed ADCs.

Power-supply bypass capacitors are very important at high frequency due to the distributed impedance between the power supply and the op amp.

References

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C011905

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