

Design and analysis of a time-gain-control (TGC) circuit to drive the control voltage for TI's ultrasound AFE

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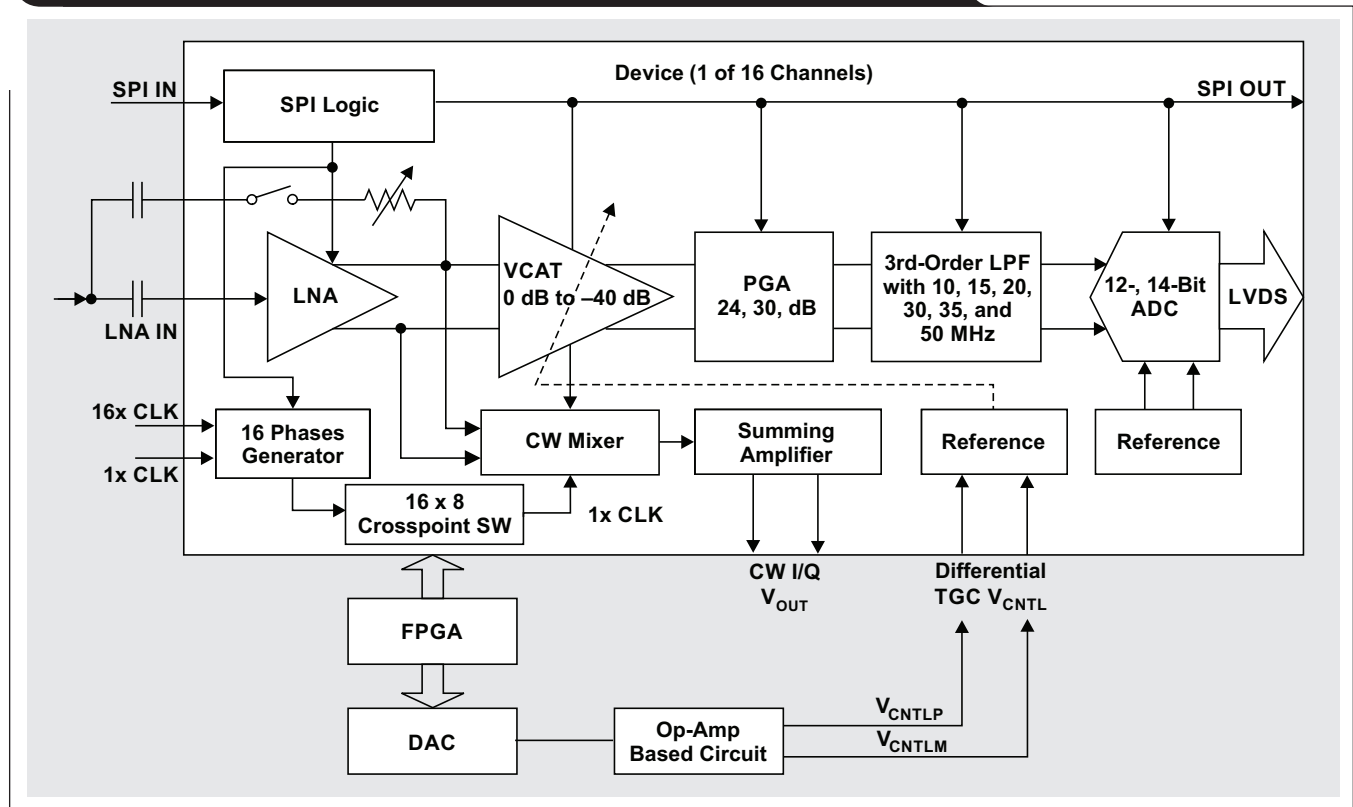
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Introduction

TI's low-noise analog front ends (AFEs) have a time-gain-control (TGC) feature that supports ultrasound applications because they can alter the gain of the receiver as a function of time. The ultrasound signal incident on the receiver decreases in amplitude as the time elapsed since transmission, and the TGC helps achieve the best possible signal-to-noise ratio (SNR), even with the decreasing signal amplitude. This article describes the specifications and design considerations of a circuit used for generating a time-varying V_{CNTL} to drive multiple AFE

receiver chips in a parallel configuration. Figure 1 shows the signal chain of the AFE5818 analog front end. The TGC is implemented using an attenuator that can be controlled with a control voltage, V_{CNTL} . External circuitry comprised of a digital-to-analog converter (DAC) and operational amplifier (op amp) generates the control signal. The input signal for the DAC is a time-varying digital control from a field-programmable gate array (FPGA) that could also handle the beamforming operation required in an ultrasound application.

Figure 1. Signal chain of the AFE5818 and analog control for TGC operation



Here are some V_{CNTL} attributes from the AFE's point of view.

- Signal levels on the control pins of the AFE:** In the case of the AFE5818, V_{CNTL} is a differential input, V_{CNTLP} and V_{CNTLM} . When the V_{CNTL} level (defined as $V_{CNTLP} - V_{CNTLM}$) is above 1.5 V or below 0 V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level, respectively. As shown in Figure 2, V_{CNTL} has a range of 1.5 V to 0 V, and results in a gain-control range of 40 dB.
- Input-referred noise:** As the received ultrasound signal decreases as a function of elapsed time, V_{CNTL} also decreases to reduce the attenuation and increase the channel gain. Figure 3 shows the benefit of the TGC circuit. As V_{CNTL} decreases and the channel gain increases, the input-referred noise of the receiver also continues to decrease. The reduced noise helps arrest the SNR fall related to the declining amplitude of the receiver signal.
- Noise requirement for multiple channels:** One key consideration in the design of the V_{CNTL} drive circuit is the noise specification on V_{CNTL} . Since V_{CNTL} is a common control voltage across multiple channels of the AFE (and possibly shared with the channels of other AFE chips), any noise on V_{CNTL} shows up as a source of noise that is correlated across the multiple AFE channels that share that same V_{CNTL} . Figure 4 shows the allowed noise on V_{CNTL} as a function of the number of channels sharing the same V_{CNTL} drive.

Figure 2. Gain control over the signal range of V_{CNTL}

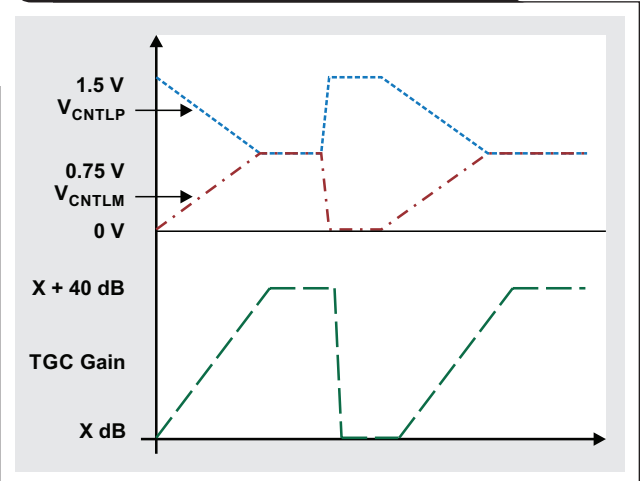


Figure 3. Input-referred noise vs. V_{CNTL}

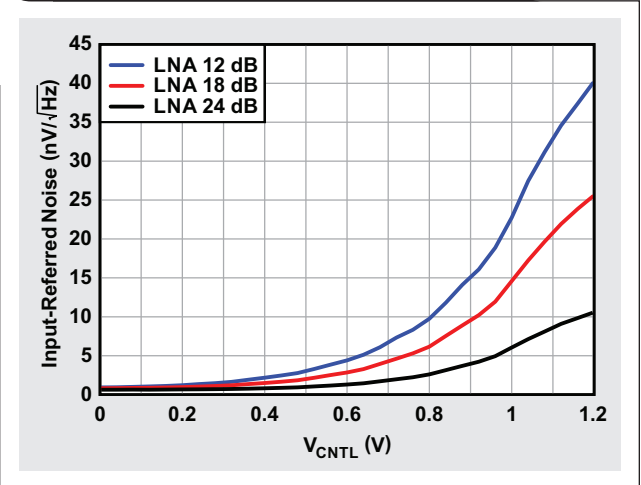
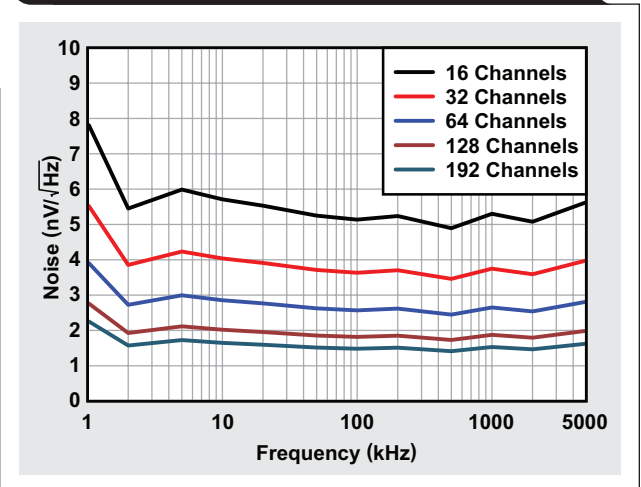


Figure 4. Allowed noise on the V_{CNTL} signal across frequency and different channels



Proposed topology

There are multiple approaches for a TGC control circuit that are based on the type of DAC. Figure 5 shows a high-level block diagram for the topology using a multiplying DAC (MDAC) to generate the drive for V_{CNTL} .

Even though the V_{CNTL} range is from 0 to 1.5 V, a much higher reference voltage, $V_{REF} = 10\text{ V}$, is used for the DAC. Filtering the reference voltage removes high-frequency noise and the DAC generates an output range of 0 to V_{REF} . The output of the DAC is buffered using an op amp to a level of $-V_{REF}$ to 0. Additional signal conditioning may involve low-pass filtering to reduce the noise bandwidth. Finally, an attenuation circuit reduces the range to the desired V_{CNTL} range.

The above approach that starts off with a high reference voltage and high DAC full-scale range, followed by attenuation, helps attenuate noise contributions from the

reference circuit and the DAC, as well as other op amps used for signal conditioning. Using this topology, Figure 6 shows the drive circuit for the control voltage.

The REF102 generates a 10-V reference voltage that is filtered and buffered to generate V_{REF_10V} . This serves as the reference voltage for the DAC8801, which generates a current output on I_{OUT} corresponding to the digital input code. The I_{OUT} pin of the DAC8801 is connected to the virtual ground (negative terminal) of the OPA211; the feedback resistor (R_{FB} is internal to the DAC8801) is connected to the output of the OPA211, resulting in a current-to-voltage conversion. The output of the OPA211 has a range of -10 V to 0 V and it is input to the THS4130, which is configured as a Sallen-Key filter. Finally, the 10-V range is attenuated down to a 1.5-V range, with common mode of 0.75 V using a resistive attenuator.

Figure 5. A current-output MDAC is used in generating a TGC signal

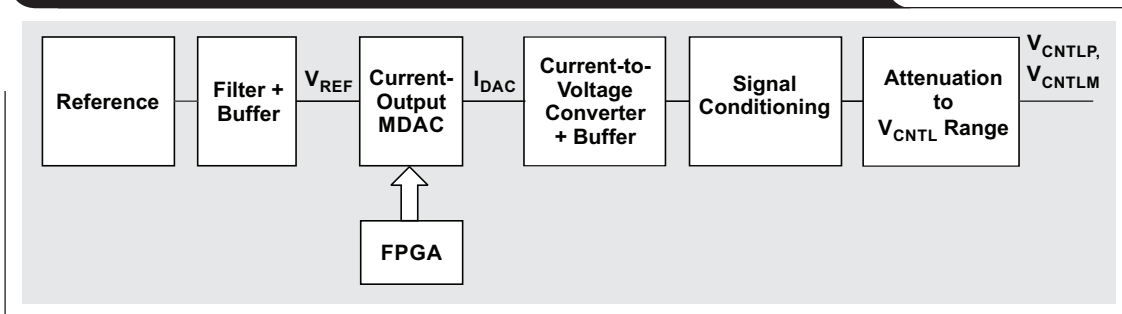
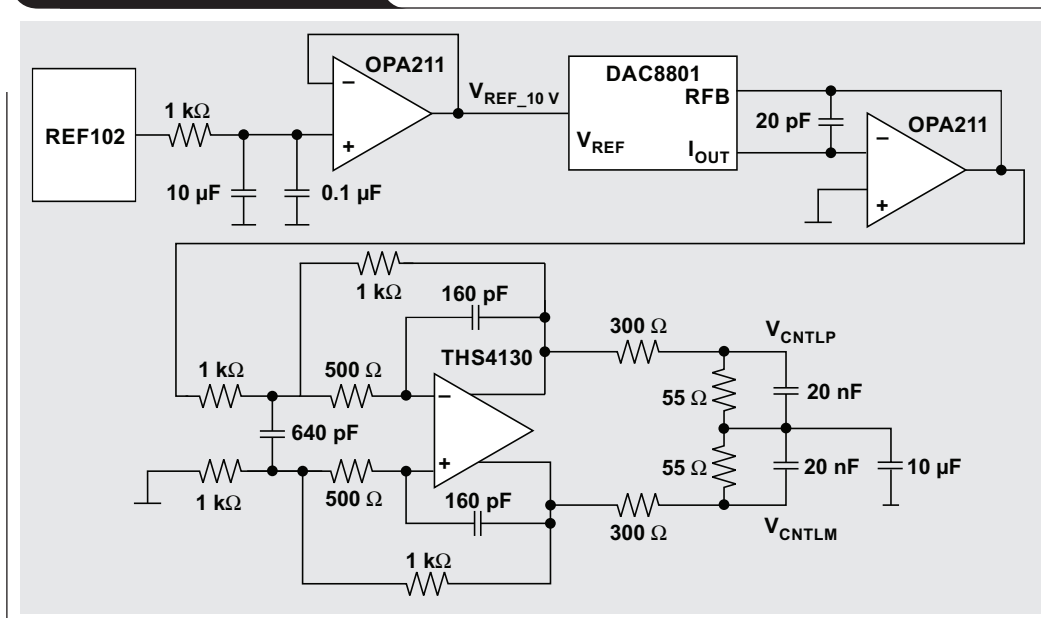


Figure 6. V_{CNTL} drive circuit



TINA-TI™ simulation

The reference section of the circuit shown in Figure 6 can be simulated in TINA-TI™ (shown in Figure 7) and noise analysis can be performed.

The thermal noise contribution from the REF102 is modeled as thermal noise from a 630-kΩ resistor. This noise is bandwidth limited using the resistor-capacitor (R-C) filter at its output. Figure 8 shows the simulated results for the noise contribution from REF102.

Figure 9 shows the modeled noise contribution of the DAC8801 at its maximum output current.

Figure 7. TINA-TI™ simulation for reference circuit in Figure 6

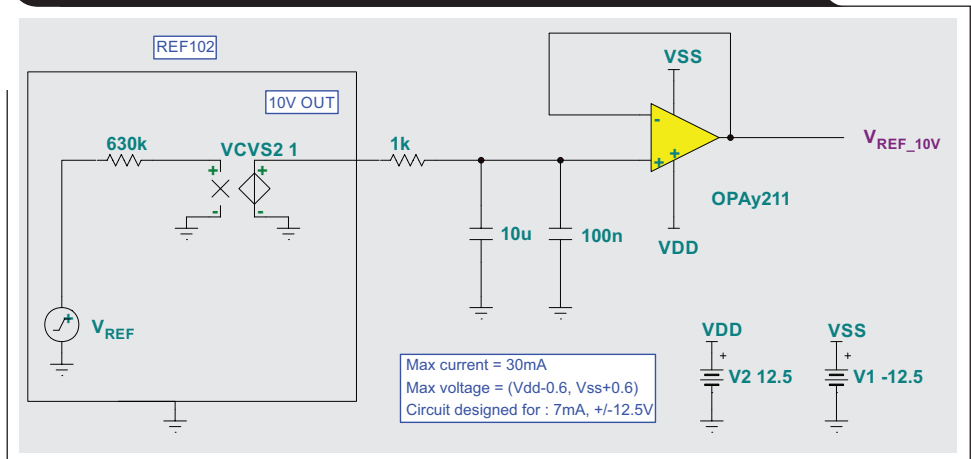


Figure 8. Noise contribution from the reference circuit

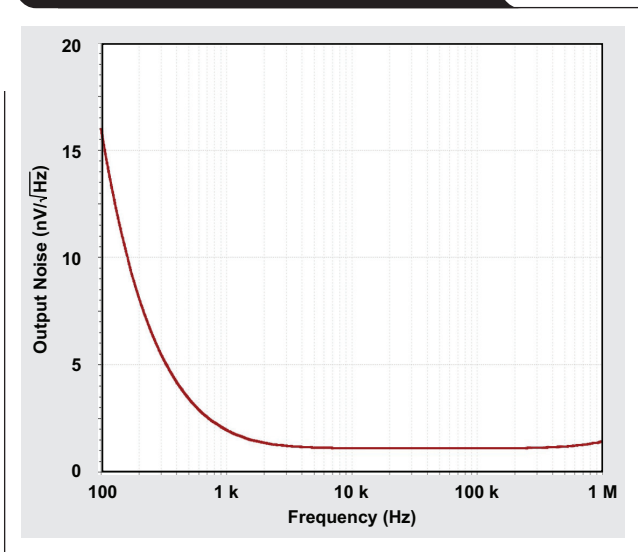
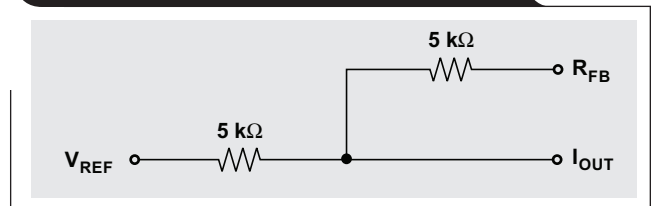
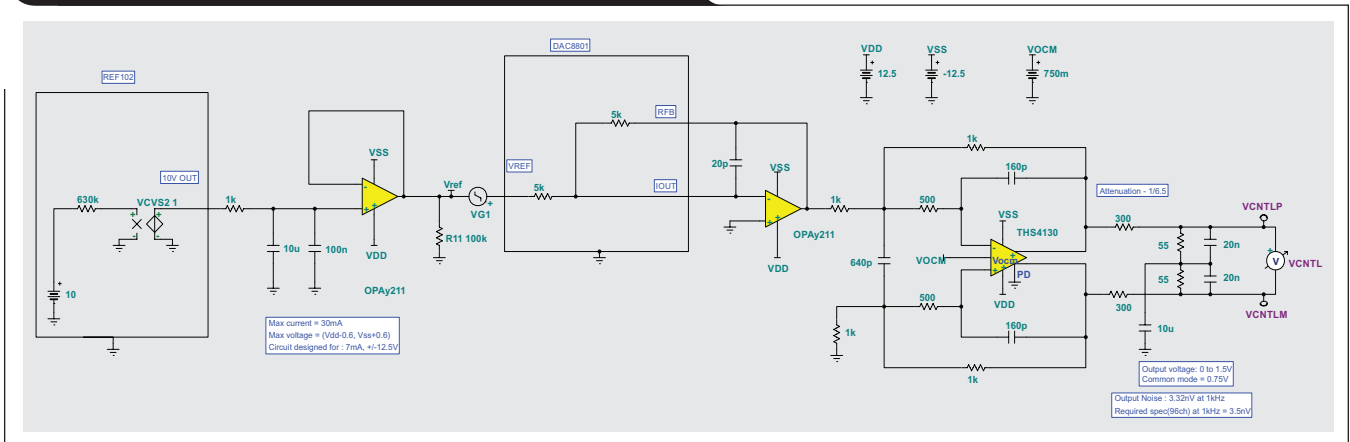


Figure 9. Noise model for the DAC8801



The TINA-TI models for the OPA211 and THS4130 are available from TI. See related Web sites at the end of this article. Figure 10 shows the TINA-TI simulation for the entire circuit.

Figure 10. TINA-TI simulation of the V_{CNTL} drive circuit



Figures 11 and 12 show the differential V_{CNTL} output signal and noise contribution of the circuit, respectively. The output noise of $3.32 \text{ nV}/\sqrt{\text{Hz}}$ at 10 kHz indicates that such a drive circuit can drive between 32 and 64 channels simultaneously.

Conclusion

This article described an approach to designing a low-noise drive circuit for the control voltage in TGC applications. Using a high-voltage DAC and attenuating its output to achieve the required range on the control voltage helps attenuate the noise from the reference circuit, DAC, and op amps used in signal conditioning.

Reference

1. Sanjay Pithadia and Rahul Prakash, "Time Gain Control (Compensation) in Ultrasound Applications," Texas Instruments Application Report (SLAA724), December 2016.

Related Web sites

TINA-TI™ simulation tool

Tools and software with product information:

OPA211

THS4130

Product information:

AFE5818

DAC8801

REF102

Figure 11. Differential V_{CNTL} output signal

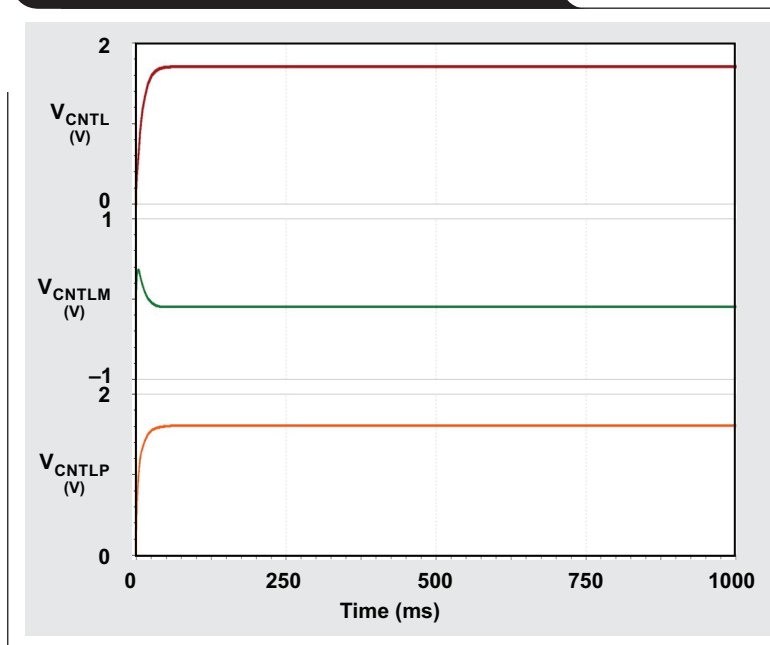
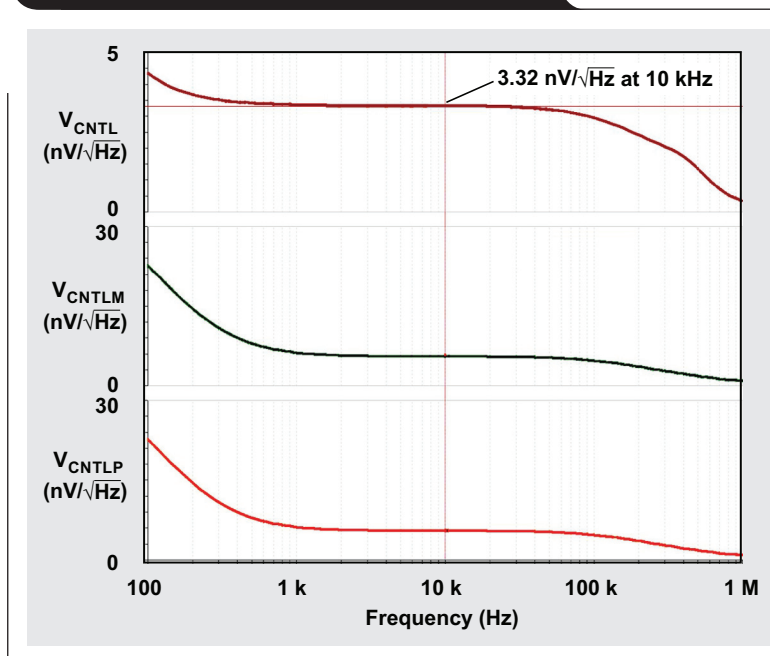


Figure 12. Noise contribution of the circuit



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