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Fixed-frequency DCS-Control: Fast transient response with clock synchronization

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Introduction

A common drawback with constant on-time (COT) control topologies is the switching frequency variation and inability to synchronize to an external clock. TI's fixed-frequency direct control with seamless transition into power save mode (fixed-frequency DCS-Control) topology builds on the popular COT DCS-Control topology with its fast transient response, and adds an oscillator to achieve fixed-frequency operation with optional clock synchronization. This combination enables applications that require both a fast transient response and have specific noise or frequency requirements.

Other features such as differential remote sensing, external control-loop compensation and stackability support the demanding transient requirements of higher-current processors found in noise-sensitive applications, including automotive infotainment and advanced driver assistance systems (ADAS), communications equipment optical modules, industrial test and measurement, medical, and aerospace and defense. This article provides an overview of the fixed-frequency DCS-Control topology, discussing its excellent transient response, constant and synchronize-able switching frequency, lower-ripple power-save mode, and stackability for higher currents.

DCS-Control topology overview

Figure 1 shows the basic block diagram of the DCS-Control topology [1]. Both the output-voltage sense (VOS) and feedback (FB) pins provide the inputs to the control loop for proper regulation. The VOS pin provides the topology's fast transient response by directly feeding the output voltage into a ramp and then into the comparator, where it immediately affects the operating point. The FB pin is a lower-bandwidth path that provides highly accurate DC setpoint regulation. When combined in DCS-Control, the VOS pin's AC path and FB pin's DC path provide an accurate output voltage that also responds quickly to load transients.

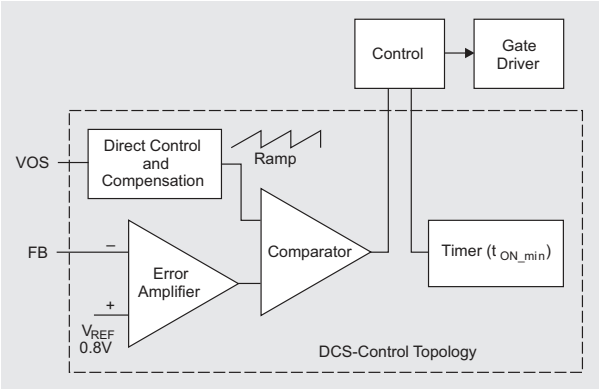

Figure 1. *Block diagram of the DCS-Control topology.*

A COT topology such as DCS-Control sets the on-time with a timer. By adjusting this on-time with the input and output voltage, the timer gives a reasonably constant frequency operation for most duty cycles in pulse-width modulation (PWM) mode. **Equation 1** shows an example, where 416ns is the period for a 2.4MHz switching frequency:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 416ns \quad (1)$$

However, the switching frequency is not precise enough for applications that require operation inside or outside of a specific frequency band. These applications generally require setting the switching frequency with an oscillator, such as in voltage- or current-mode control, and in some cases, the ability to synchronize with a system clock signal. Reference [2] offers further examples of the frequency variation of DCS-Control.

Fixed-frequency DCS-Control topology overview

Figure 2 shows a basic block diagram of the fixed-frequency DCS-Control topology, as implemented in the 15A **TPS62873** buck converter. The addition of an oscillator enables the direct setting of the switching frequency (f_{SW}) in the same way as voltage- or current-mode control. Having an oscillator input into the control loop also provides the ability to synchronize the switching frequency to an applied clock signal.

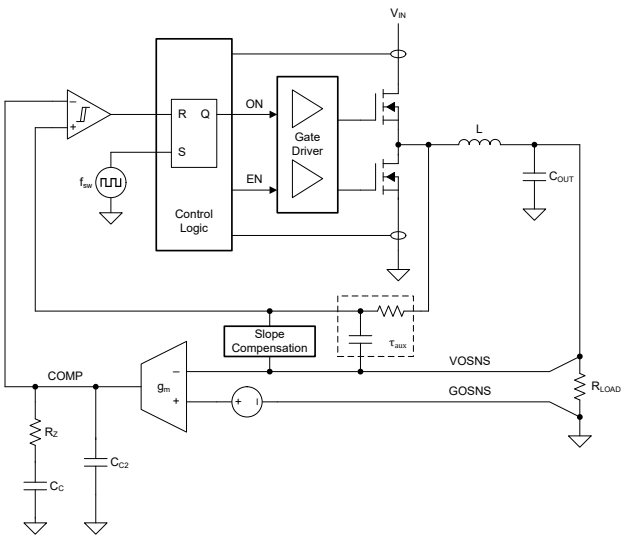

Figure 2. *Block diagram of the TPS62873's fixed-frequency DCS-Control topology with the oscillator, differential remote sensing, transconductance amplifier and hysteretic comparator.*

Fixed-frequency DCS-Control, usually used in higher-current devices, uses differential remote sensing. The device regulates the voltage between the VOSNS and GOSNS pins, which are routed across the printed circuit board (PCB) to sense the output voltage directly at the load. Sensing at the load overcomes and compensates for not only the DC voltage drops across the PCB planes and traces, but also the delays that come from inductance between the device and the load. Both of these characteristics are important for maintaining very tight regulation across the load range and during load transients.

The differential remote-sensing signals are fed into the transconductance amplifier (g_m), which compares their difference against the output voltage setpoint. (For simplicity, **Figure 2** shows this setpoint as a voltage source in series with the GOSNS signal.) The COMP pin gives the output of this amplifier, which is compensated with a Type II (one pole, one zero) network to ground.

This external compensation allows you to optimize the control loop to any system need – from systems with strong load transients with large output capacitance, all the way down to systems with small or no load transients with very little output capacitance and small size. Unlike DCS-Control, the fast feedback path goes through this amplifier – not immediately to the comparator – where compensation component selection can increase (or decrease) the gain. If you need a stronger transient response, you increase the gain and add more output capacitance. If no strong transients are present in the application, you decrease the gain and use a minimal amount of output capacitance in order to achieve the smallest size.

The ability to adjust the transient response to the application needs enables tighter regulation under harsher transients than what is possible with the previous DCS-Control topology, and meets the requirements of demanding processor cores such as TI's Jacinto™ J7 and MobileEye's EyeQ6 [3-4]. **Figure 3** shows a stack of three **TPS62876-Q1** buck converters delivering a 46A load transient, while maintaining the output voltage within ±2% of the 0.875V setpoint.

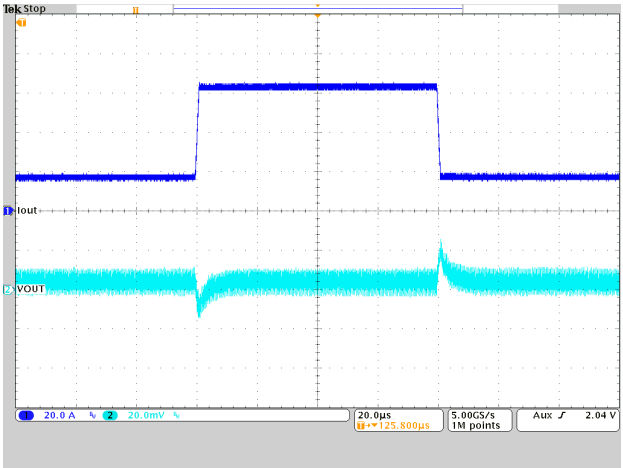

Figure 3. *The transient response of fixed-frequency DCS-Control is tunable to the most severe load transients, where it provides excellent regulation.*

A hysteretic comparator compares the COMP pin output and a replica of the inductor current, created by the τ_{aux} components, with slope compensation added to prevent subharmonic oscillations. The comparator's output drives the Set-Reset (SR) latch circuitry, along with the clock, which controls the gate drivers and device operation. The oscillator controls the switching to occur exactly at the switching frequency.

The Set-Reset latch is a simplified representation of the detailed operation of the control block and is implemented to maintain the fast, hysteretic nature of DCS-Control and thus enable an immediate response to load transients. For example, during a load-dump transient (where the output voltage rises), the output of the hysteretic comparator has priority over the clock signal. The converter extends the off-time of the high-side MOSFET as needed to bring the output voltage back down with minimum overshoot. This is inherently improved behavior compared to textbook peak current-mode control, which switches at every clock cycle, continuing to add energy to the output, even while it is too high. By reducing the output-voltage overshoot, the converter significantly reduces the output capacitance, which is a key influence on the cost and size of the power supply.

Switching frequency variation

In addition to maintaining the fast transient response, which can be further improved and tuned through the external compensation on the COMP pin, fixed-frequency DCS-Control provides a fixed switching frequency with a tight tolerance specification. Because the switching frequency is directly set with an oscillator instead of indirectly controlled with an on-timer, the frequency's tolerance is specified in the device-specific data sheet. **Table 1** and **Table 2** compare the switching frequency specifications of the **TPS62876-Q1**, using the fixed-frequency DCS-Control topology, versus the typical frequency specification of the DCS-Control **TPS62869** step-down converter.

Parameter		Test Conditions	MIN	TYP	MAX	Unit
f_{SW}	Switching Frequency	f_{SW} = 1.5MHz, PWM operation	1.35	1.5	1.65	MHz
		f_{SW} = 2.25MHz, PWM operation	2.025	2.25	2.475	
		f_{SW} = 2.5MHz, PWM operation	2.25	2.5	2.75	
		f_{SW} = 3MHz, PWM operation	2.7	3	3.3	

Table 1. *The TPS62876-Q1, using the fixed-frequency DCS-Control topology, specifies a ±10% tolerance of its four switching frequency options over the full temperature and input voltage ranges.*

Parameter		Test Conditions	MIN	TYP	MAX	Unit
f_{SW}	PWM switching frequency	I_{OUT} = 1A, V_{OUT} = 0.9V		2.4		MHz

Table 2. *The TPS62869, using DCS-Control, only specifies a typical switching frequency.*

Figure 4 and **Figure 5** compare the actual variation of the switching frequency versus load current in an application. Both devices support power-save mode, which reduces the frequency at lower load currents (toward the left of both graphs). Operation in PWM mode (at higher currents) results in a precisely controlled switching frequency for fixed-frequency DCS-Control, while the switching frequency of DCS-Control increases slightly with an increasing load. In forced PWM mode

(not shown), fixed-frequency DCS-Control maintains its constant frequency down to no load.

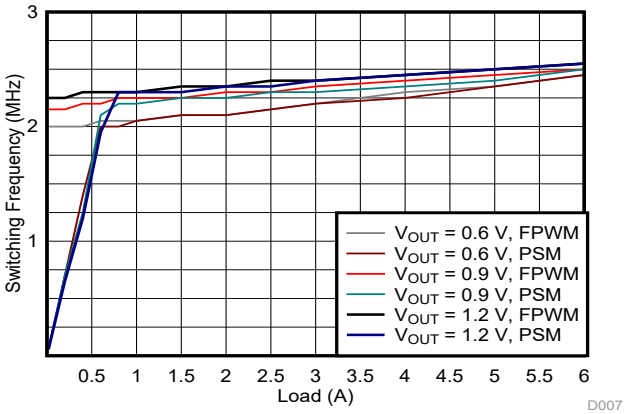

Figure 4. *Switching frequency variation of the TPS62869 with DCS-Control.*

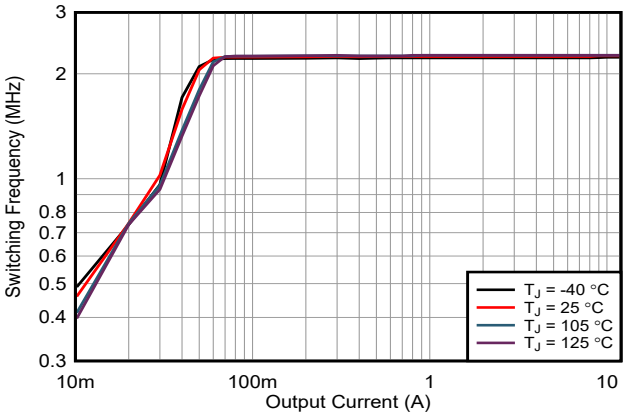

Figure 5. *Switching frequency variation of the TPSM8287A12 power module with fixed-frequency DCS-Control.*

Besides power-save mode, there are two conditions where the switching frequency can deviate from the frequency set by the oscillator: during a strong load transient and if the minimum on-time is reached. When applying a heavy load, the high-side MOSFET may be on for longer than a full switching period, and when removing a heavy load, it may be off for longer than a full switching period. Both scenarios result in one or more pulses that are not present because of the extended on- or off-times.

If the minimum on-time of the high-side MOSFET is reached, both fixed-frequency DCS-Control and DCS-Control reduce the switching frequency in order to meet the minimum on-time and maintain output-voltage regulation. This is improved performance compared to some current-mode devices that maintain the frequency but let the output voltage rise in order to meet the required minimum on-time. While both fixed-frequency DCS-Control and DCS-Control reduce the switching frequency in the same way [2], fixed-frequency DCS-Control has fewer operating conditions during which the minimum on-time is reached, and the frequency reduced, because of its lower minimum on-time. For example, the **TPS62876-Q1** specifies the 44ns maximum value of its minimum on-time at a 5V input voltage and across the operating temperature. Such a low value of minimum on-time enables lower output-voltage applications in automotive and aerospace and defense, for example, to operate in the higher-frequency region sometimes required by the overall system.

Lower-ripple power-save mode

While most applications operate a fixed-frequency DCS-Control device in forced PWM mode in order to obtain lower output-voltage ripple at light loads and a better transient response, the topology does support a power-save mode to increase efficiency at light loads. To maintain the target switching frequency and provide lower ripple down to lower load currents, fixed-frequency DCS-Control reduces the on-time in power-save mode, whereas DCS-Control keeps the on-time constant. Both topologies enter power-save mode when the inductor current becomes discontinuous, which creates slightly higher ripple compared to PWM mode.

Instead of reducing the frequency with the same on-time, fixed-frequency DCS-Control's power-save mode reduces the on-time while maintaining the same frequency. Reducing the on-time delivers less energy to the output, thereby reducing the ripple voltage compared to DCS-Control. Once the on-time reduces to its minimum, skipping pulses reduces the output power further for the lightest loads. Skipping pulses also reduces the frequency.

Figure 4 and **Figure 5** show the difference in frequency reduction in power-save mode. The fixed-frequency DCS-Control device reduces its frequency below loads of around 60mA, while the DCS-Control device begins reducing the frequency around 500mA. Although these current values are different for different devices and operating conditions, fixed-frequency DCS-Control maintains its switching frequency down to lower load currents, leading to lower ripple.

Stacking (paralleling) for higher (or lower) load currents

On one hand, processor cores frequently require higher currents with each successive processor generation. On the other hand, some applications may not use all of the functionality of a given processor or may use a less-capable processor within the same processor family, resulting in lower current requirements. Scaling the power supply's current capability both up and down requires a stackable (parallelable) solution where it is possible to add or remove additional power-supply phases as the current requirements change.

Fixed-frequency DCS-Control devices support stacking. While the specific implementation details vary slightly between each device family, features include current sharing, phase interleaving and interface simplicity.

Current sharing is accomplished through the COMP pin. Since the COMP pin is essentially the small-signal operating point, sharing this pin's signal between all stacked devices enables fixed-frequency DCS-Control to typically achieve tighter than 10% current-sharing accuracy.

Phase interleaving is accomplished by a dedicated SYNC_OUT pin, which connects to the MODE/SYNC input pin of the next device in the stack. SYNC_OUT is automatically phase-shifted in order to provide ripple cancellation. Through this simple daisy chaining, all devices in the stack operate at the same frequency and with lower ripple than a single-phase design. You can stack a large number of converters and achieve very good phase balancing without needing to specify the number of devices in the stack.

When interfacing to the stack through I2C, communication only happens to the primary device – not each device in the stack – in order to adjust the output voltage, change the operating mode, or read back fault registers. Interfacing to a single device greatly simplifies the communication overhead and PCB routing by both reducing the number of reads and writes and the number of PCB signals that need routing.

Conclusion

With its fast transient response and stackability, fixed-frequency DCS-Control powers the latest processors' demanding load transient and output-current requirements, while its fixed-frequency operation and synchronization make it a great fit for noise-sensitive applications. Automotive ADAS and infotainment, optical modules, industrial test and measurement, medical, and aerospace and defense applications all benefit. The tunable external control-loop compensation supports a fast transient response with the minimum amount of output capacitance, reducing the size and cost of a power-supply system.

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A novel charge-mode control algorithm for PFC

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Introduction

In a control system, if you want to control something, you need to sense it; this applies to power factor correction (PFC) applications as well. In offline power supplies with power levels >75W, PFC controls the input current to create a sinusoidal waveform (in other words, following the sinusoidal input AC voltage). In order to control the input current, it needs to be sensed.

The most common current-sensing method places a shunt resistor at the PFC ground return path (designated as R in **Figure 1**) to sense the input current. The sensed input current signal (I_{SENSE}) is then sent to an average current-mode controller [1] (shown in **Figure 2**). Because the current reference (I_{REF}) is modulated by the input voltage (V_{IN}), it is a sinusoidal waveform. The control loop forces the input current to follow I_{REF}, thus achieving a sinusoidal waveform.

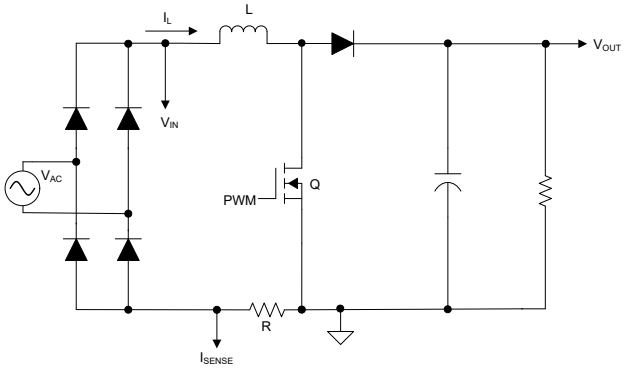

Figure 1. *A common current-sensing method for PFC.*

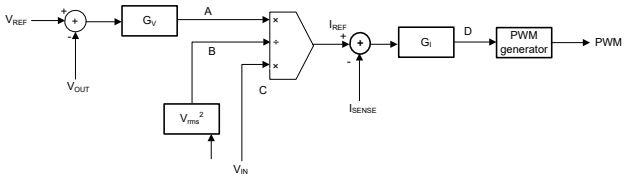

Figure 2. *Traditional average current-mode control for PFC.*

Almost all continuous conduction mode (CCM) PFC controllers use traditional average current-mode control. Although traditional average current-mode control achieves a good power factor and has low total harmonic distortion, it also has some limitations, especially in totem-pole bridgeless PFC. This article presents a brand-new control algorithm: charge-mode control [2].

Charge-mode control

The charge-mode control algorithm is a new control concept: to control an object, you don't really need to sense it – you can sense its consequence and then indirectly control the object. For PFC, instead of controlling the input current directly, this control algorithm controls how much electric charge is delivered to the PFC output in each switching cycle, and employs a special control law such that the input current becomes a sinusoidal waveform by controlling the electric charge.

There are a few ways to obtain the electric charge information. **Figure 3** shows an example of using a current shunt and an operational amplifier (op amp) circuit, with the op amp configured as an integrator. When the PFC boost switch turns off, the inductor current starts to charge the PFC bulk capacitor. The shunt resistor senses this current, which is then integrated through the integrator. The peak value of the integrator output represents the total electric charge

delivered to the PFC output in each switching cycle. This electric charge (V_{CHARGE}) is sampled by the controller as a control-loop feedback signal. The integrator discharges to zero through Q1 before the boost switch turns off.

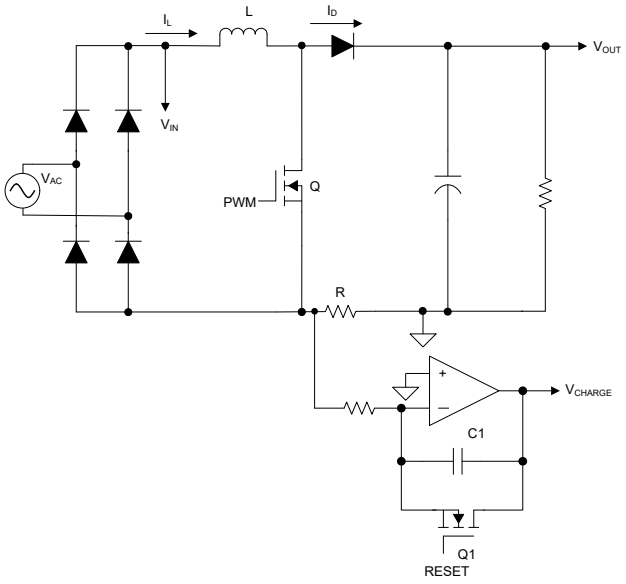

Figure 3. *Using the current shunt and op amp to obtain an electric charge.*

Figure 4 shows another method, which employs a current transformer (CT) on the PFC output side. The CT output connects to capacitor C1. When the PFC boost switch turns off, the inductor current starts to charge the PFC bulk capacitor. The CT senses this current and its output charges C1. The voltage on C1 rises up; its peak voltage represents the total charge delivered to the PFC output. The controller samples the peak voltage V_{CHARGE} as a control-loop feedback signal. C1 discharges to 0V through Q1 before the boost switch turns off.

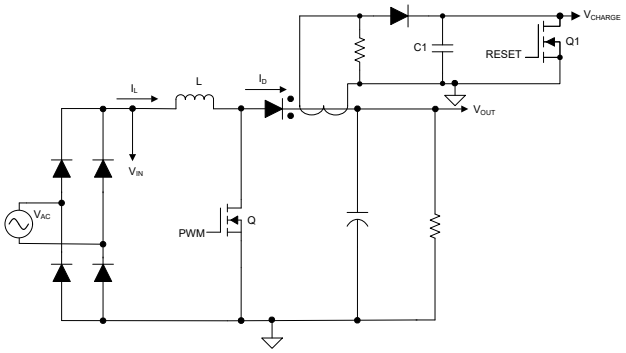

Figure 4. *Using a CT to obtain an electric charge.*

Figure 5 shows the typical signal waveform for charge-mode control.

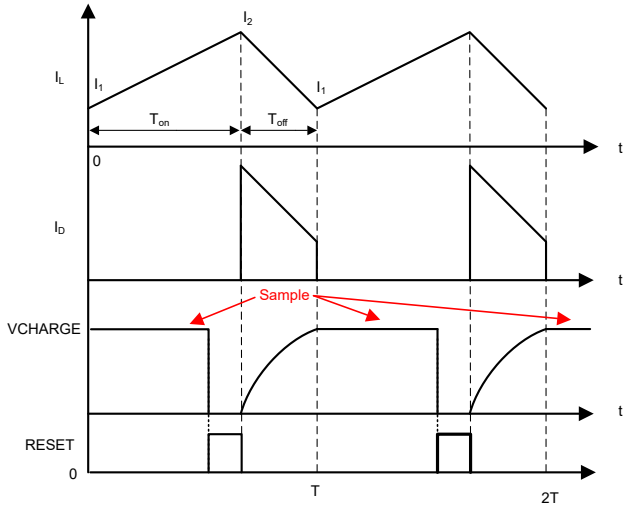

Figure 5. *Typical signal waveforms for charge-mode control.*

Control law

Now that you know how to obtain the electric charge information for each switching cycle, let's take a look at how to get the sinusoidal input current waveform using the new control law, see Figure 6.

Compared to the traditional control law shown in Figure 2, there are two differences:

- The current-loop reference is modulated by V_{IN}^2, not by V_{IN}.
- The feedback signal is the electric charge V_{CHARGE}, not I_{SENSE}.

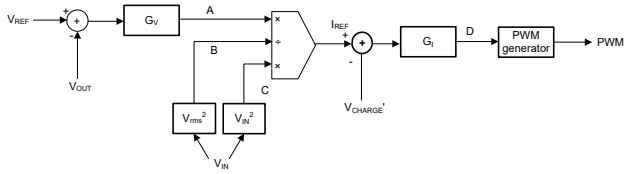

Figure 6. *Charge-mode control law for PFC.*

From Figure 6, the current reference I_{REF} is given by:

$$I_{REF} = \frac{A \cdot C}{B} \quad (1)$$

where, I_{REF} is the current-loop reference, A is the voltage-loop output G_V, B is $Vrms^2$ used for V_{IN} feedforward control, and C is V_{IN}^2.

Looking at **Figure 5**, **Equation 2** expresses the average inductor current in each switching cycle as:

$$I_{AVG} = \frac{(I_1 + I_2)\ (T_{on} + T_{off})}{2\ T} \quad (2)$$

where, I_{AVG} is the average inductor current, I_1 is the inductor current at the beginning of each switching cycle, I_2 is the inductor current peak value in each switching cycle, T_{on} is the boost switch Q turn on time, T_{off} is the boost diode D conduction time, and T is the switching period.

Equation 3 calculates the peak voltage of C1 (V_{CHARGE}) in each switching cycle as:

$$V_{CHARGE} = \frac{(I_1 + I_2)\ T_{off}}{2\ C} \quad (3)$$

where, C is the capacitance of C1.

In steady state, the control loop forces V_{CHARGE} to equal I_{REF} (see **Equation 4**):

$$V_{CHARGE} = I_{REF} \quad (4)$$

For a boost-type converter in steady-state operation, the volt-seconds applied to the boost inductor must be balanced in each switching period (see **Equation 5**):

$$T_{on}\ V_{IN} = T_{off}\ (V_{OUT} - V_{IN}) \quad (5)$$

Equation 6 combines **Equation 1** through **Equation 5**:

$$I_{AVG} = \frac{G_V\ V_{OUT}\ C}{V_{rms}^2\ T}\ V_{IN} \quad (6)$$

In **Equation 6**, since both C and T are constant, and G_V, V_{OUT} and $Vrms^2$ do not change in steady state, I_{AVG} follows V_{IN}. When V_{IN} is a sinusoidal waveform, I_{AVG} is also a sinusoidal waveform, thus achieving PFC. Note that **Equation 2** and **Equation 3** are valid for both CCM and discontinuous conduction mode (DCM); therefore, **Equation 6** is valid for both CCM and DCM operation.

RHPZ effect and solution

The loop compensation for charge-mode control is simple when the PFC operates in DCM. Loop compensation becomes a challenge, however, because a right-half-plane zero (RHPZ) appears in the control loop when the boost converter operates in CCM [3]. The RHPZ induces a phase drop that negatively impacts the potential phase margin of the control loop. **Equation 7** expresses the small-signal model for the control loop as:

$$\frac{\hat{v}_{CHARGE}}{\hat{d}} = \frac{V_{OUT}(1-D)T}{sLC}\left(1 - \frac{sL}{(1-D)^2 R_{LOAD}}\right) = \frac{1 - \frac{s}{\omega_Z}}{\frac{s}{\omega_0}} \quad (7)$$

where R_{LOAD} is the output load of PFC, D is the pulse-width-modulation duty cycle, $\omega_0 = \frac{V_{OUT}T(1-D)}{sLC}$ and $\omega_z = \frac{R_{LOAD}T(1-D)^2}{L}$.

Equation 7 clearly shows the RHPZ ω_Z. Its frequency varies with load, boost inductance and D (D varies with the input and output voltage), which makes loop compensation very difficult.

To eliminate the RHPZ, **Equation 8** modifies the feedback signal:

$$V'_{CHARGE} = \frac{V_{CHARGE}}{T_{off}} \quad (8)$$

Figure 7 modifies the control law, where you can see that I_{REF} is now modulated by V_{IN}, not by V_{IN} [2].

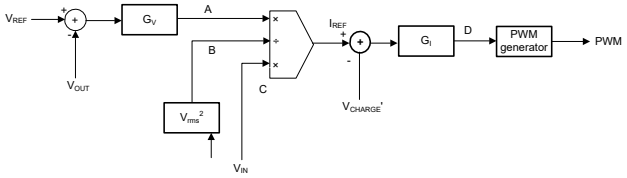

Figure 7. *Charge-mode control law for PFC after eliminating RHPZ.*

With this modification, **Equation 9** expresses the small-signal model of the control loop as:

$$\frac{\hat{v'}_{CHARGE}}{\hat{d}} = \frac{V_{OUT}}{sL} \quad (9)$$

The RHPZ disappears and the system becomes a first-order system, which is very easy to compensate.

Figure 8 illustrates the verification of the new control algorithm through simulation, achieving a sinusoidal input current waveform.

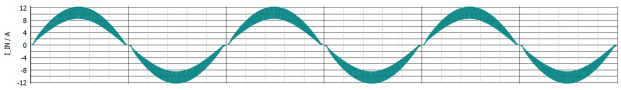

Figure 8. *Simulation result: a sinusoidal input current waveform.*

Conclusion

Instead of controlling the input current directly, charge mode controls how much electric charge to deliver to the PFC output in each switching cycle. This algorithm works for all PFC topologies, but it is especially useful for totem-pole bridgeless PFC, which has traditionally required a sensor such as Hall-effect sensor to sense the bidirectional inductor current. The problem is that Hall-effect sensors are not only expensive, but also have limitations such as limited bandwidth, sensitive to magnetic field and DC offset shifting with temperature, etc. Because charge-mode control eliminates the need to sense inductor current, there is no need for an expensive bidirectional current sensor. Instead, you can use a current-sense resistor along with a low-bandwidth op amp or a CT, which are much less expensive.

Because of its high efficiency, totem-pole bridgeless PFC is attractive for applications that require high efficiency. Its high cost was always a barrier for its broader adoption, but this new control algorithm is now an option in applications that require both high efficiency and low cost. It is possible to implement charge-mode control with existing digital controllers such as Texas Instruments C2000™ microcontrollers and the UCD3138 controller, or you can employ it in the development of a new analog PFC controller.

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Redundant supply topologies for automotive applications using ideal diode controllers

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Introduction

Redundant power supplies use more than one power-supply unit to provide the necessary power for a load. They help increase a system's reliability and availability, and ensure system safety in case one of the power-supply units fails. Redundant power supplies are especially important in automotive systems for safety-critical applications, such as automated driving, where a loss of power could result in serious consequences.

ORing and priority power multiplexing are two popular techniques for implementing redundant power supplies in automotive systems. In ORing, the system selects the highest-voltage power source from multiple inputs, while power multiplexing allows the system to switch between different power sources based on priority levels or other criteria. Designers have traditionally used Schottky diodes, P-channel field-effect transistors or a combination of both for redundant circuits in a power supply.

Ideal diode controllers are integrated circuits (ICs) that can control external metal-oxide semiconductor field-effect transistors (MOSFETs) to emulate the behavior of ideal diodes. They offer several advantages over conventional diodes, such as lower power dissipation, higher current capability, reverse polarity protection, reverse current blocking and load dump protection. Ideal diode controllers can also provide inrush current limiting and overvoltage and overcurrent protection.

In this article, we will discuss the concept and benefits of ORing and power multiplexing using ideal diode controllers, the different types and architectures of ORing and power multiplexing circuits, and the challenges and solutions for implementing ORing and power multiplexing using ideal diode controllers in automotive systems.

ORing and power multiplexing techniques

Both ORing and power multiplexing techniques use ideal diodes to connect multiple input power sources to a single output load, but they differ in how they select and switch between different input sources. **Figure 1** shows a typical use case for power supply ORing and priority multiplexing.

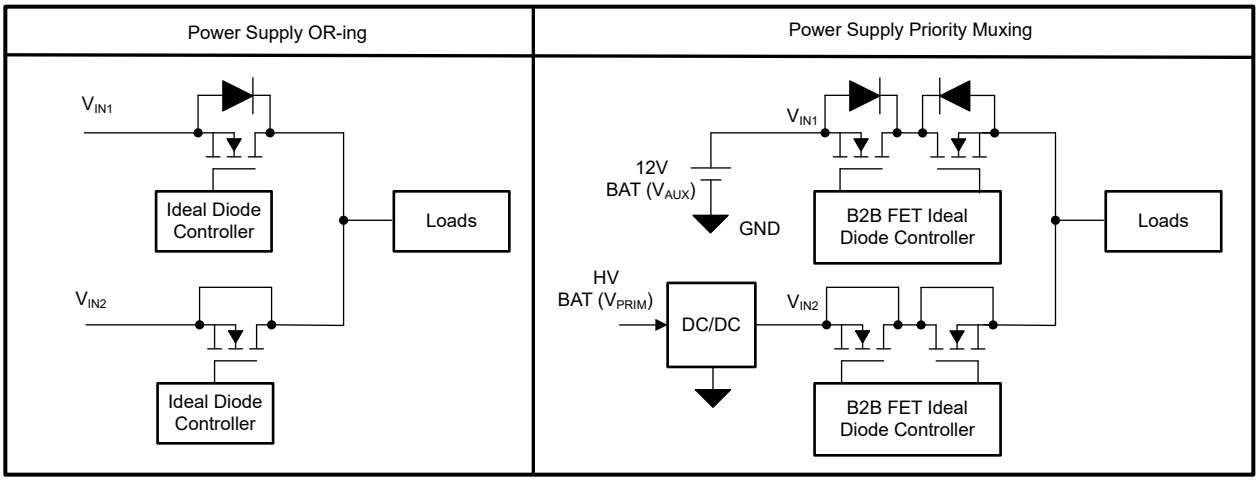

Figure 1. *Typical use case of ORing and priority power multiplexer solution.*

An ORing circuit facilitates system selection of the best available power source from multiple inputs, based on the highest input voltage. The ideal diodes act as switches that turn on when the input voltage is higher than the output voltage, and turn off when the input voltage is lower than the output voltage. This way, the ORing circuit ensures that the input source with the highest voltage is connected to the output, and prevents reverse current flow and cross conduction between the input sources. If the input power supplies are almost equal, it is possible that both power supplies share the load without any circulating current between them. Thus, reverse current blocking is the primary feature required for realizing an ORing circuit.

A power multiplexing circuit allows the system to switch between different power sources irrespective of the voltage magnitude, based on criteria such as source priority or input voltage availability and magnitude. In this configuration, the control circuit needs to switch power paths between each power supply and load on and off, controlled by its own priority logic or an external signal, such as a microcontroller general-purpose input/output pin. The power multiplexing circuit ensures that only one input source is connected to the output at any point in time, and prevents reverse current flow and cross conduction between the input sources. The circuit in this configuration is therefore required to have both reverse current blocking and load path on and off control features to enable the prioritized power supply to serve the load.

Typical application circuits for power-supply ORing

ORing circuits are popular in automotive subsystems such as infotainment, body control modules, advanced driver assistance systems and lighting modules; they provide redundancy and reliability in case of a power-supply failure or disconnection. **Figure 2** shows different ORing topologies using ideal diode controller ICs combined with external N-channel MOSFETs.

An effective ORing solution needs to be extremely fast in order to limit the duration and amount of reverse current in case one of the supplies fails. The ideal diode controllers in an ORing configuration constantly sense the voltage difference between the anode and cathode pins, which are the voltage levels at the power sources (V_{IN1}, V_{IN2}) and the common-load (V_{OUT}) point, respectively. A fast comparator shuts down the gate drive through a fast pulldown – within microseconds as soon as $V_{IN} – V_{OUT}$ falls below a designated reverse threshold, typically a few millivolts. Along with a fast reverse-current detection comparator, TI ideal diode controllers have a linear gate regulation scheme that

ensures zero DC reverse current in the event of an input supply loss.

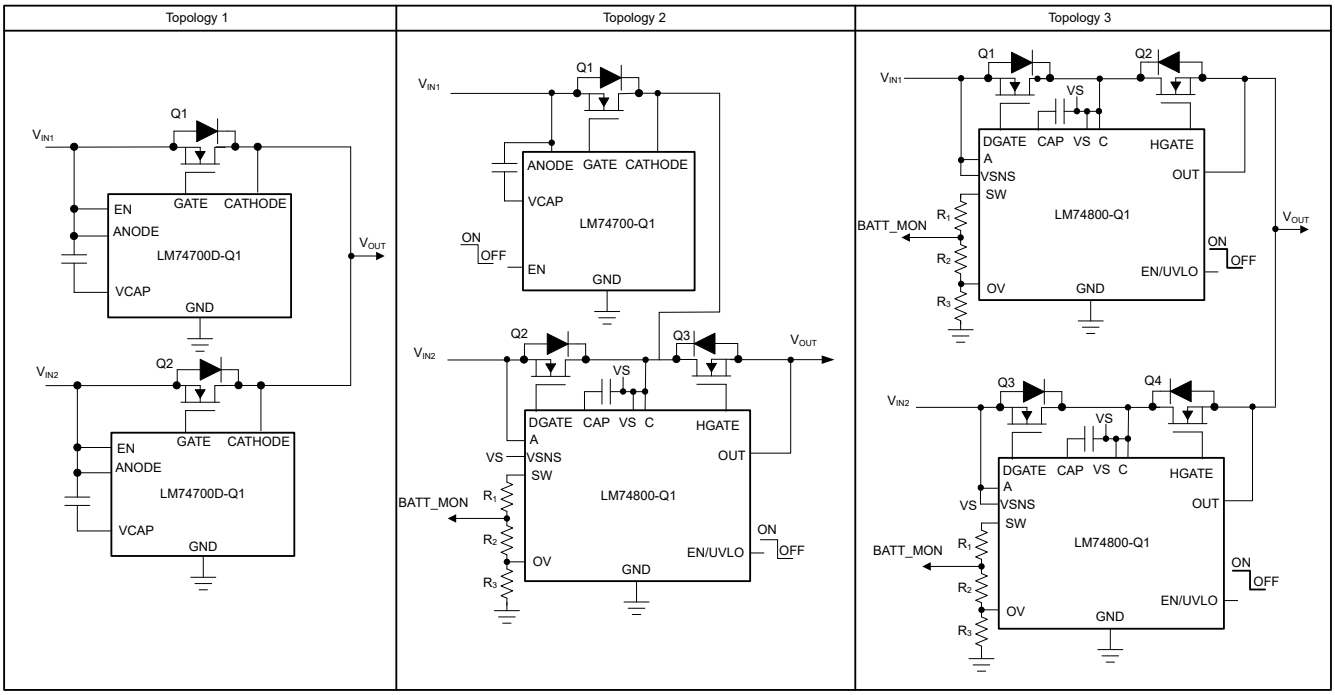

Figure 2. *Typical ORing topologies using ideal diode controllers.*

Few subsystems require disconnecting the load from the power supplies to achieve low quiescent current or to protect the system from fault conditions. Topology No. 2 in **Figure 2** shows a typical application circuit for a dual-supply input ORing with a common load disconnect control using TI's **LM7480-Q1** and **LM7470-Q1** devices. FET Q1 and Q2, driven by the **LM7470-Q1** and **LM7480-Q1**, respectively, provide ORing functionality, whereas the Q3 FET driven by the **LM7480-Q1** can isolate the load from power supplies. When V_{IN1} is greater than V_{IN2}, the independent control of FETs by the **LM7480-Q1** allows Q2 to block reverse current, while Q3 remains on, connecting V_{IN1} to V_{OUT}.

Topology No. 3 in **Figure 2** shows a typical application circuit for ORing with load disconnect functionality for individual rails, thus allowing system designers to assign different load disconnect criteria for each rail.

Figure 3 and **Figure 4** shows power-supply ORing switchover performance between two power-supply rails where V_{IN1} = 12V and V_{IN2} = 15V.

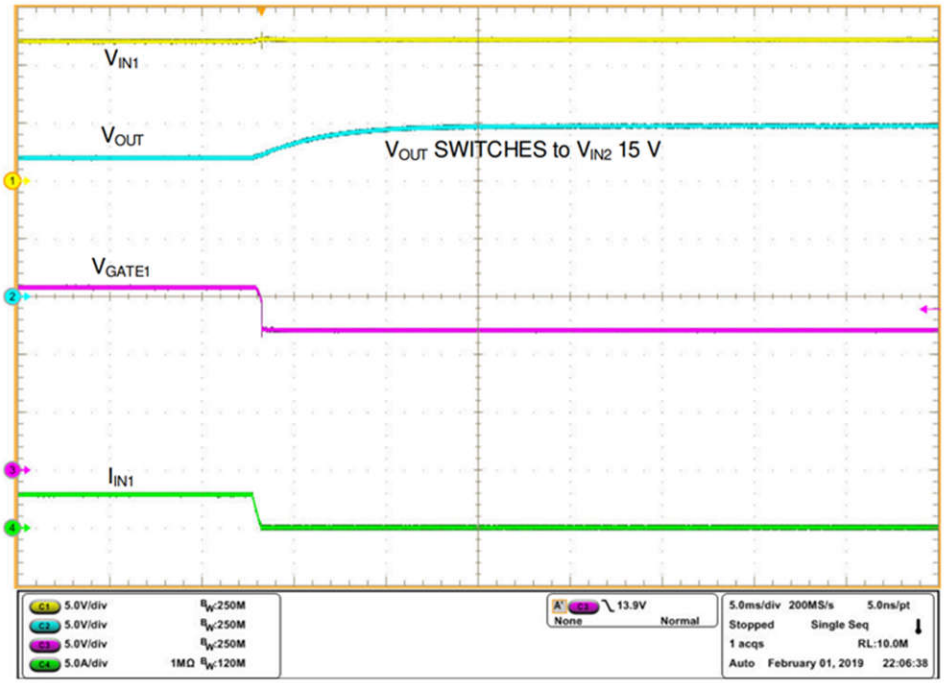

Figure 3. *Supply switchover from VIN1 to VIN2.*

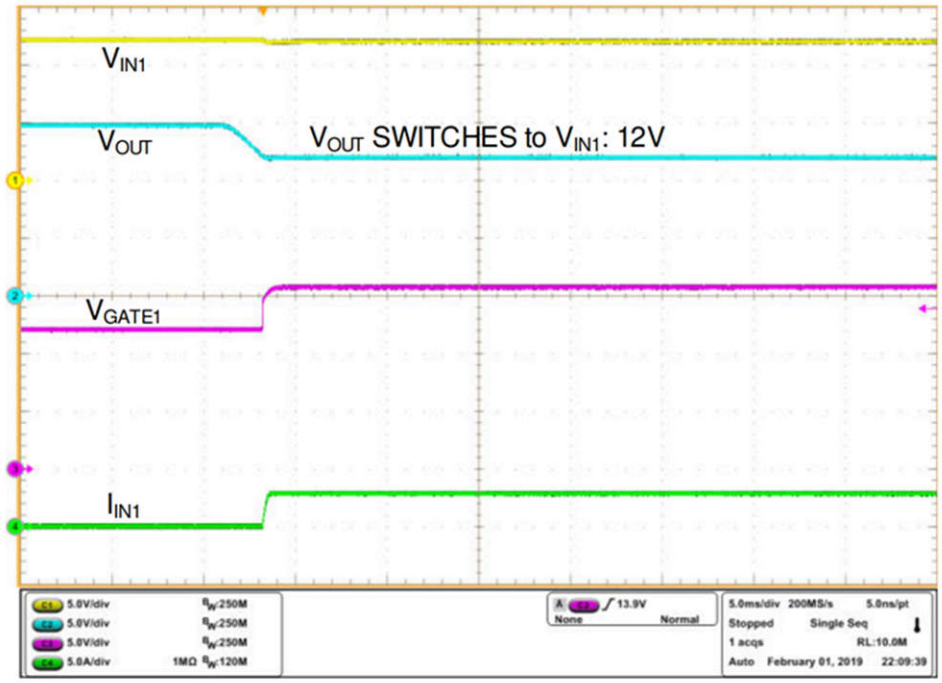

Figure 4. *Supply switchover from VIN2 to VIN1.*

Priority power multiplexer configuration

A priority power multiplexer automatically transitions the primary power supply to an auxiliary (AUX) or secondary power supply when the primary supply voltage drops below a designated threshold. When available and within acceptable limits, the primary power supply is always the first source for powering the load. For example, if an upstream smart fuse in a power distribution unit trips on the primary power supply to a subsystem, the priority power multiplexer circuit automatically connects the AUX supply to the output and disconnects the primary supply from that output to avoid any disruptions in the subsystem operation. If the upstream smart fuse is reset and the primary supply voltage rises to an acceptable threshold, then the priority power multiplexer circuit automatically connects the primary supply back to the output and disconnects the AUX supply.

A power multiplexer circuit requires a controller such as the LM74800-Q1 or **LM74900-Q1** to control two back-to-back MOSFETs on each power-supply rail. When both primary and AUX power supplies are present and within the acceptable range, and the primary is powering the load, the AUX path controller must block reverse current when the primary power-supply voltage is higher than the AUX supply. Likewise, the AUX path controller must block forward current when the primary voltage is lower than the AUX. This ensures that the primary supply, which has the highest priority, powers the load and the AUX supply is isolated from both the primary supply and the load.

The **LM74900-Q1** ideal diode controller drives and controls external back-to-back N-channel MOSFETs to emulate an ideal diode rectifier with power path on or off control and overcurrent and overvoltage protection. **Figure 5** is a schematic for a priority power multiplexer using two **LM74900-Q1** devices in a common drain topology. The overvoltage pin of the **LM74900-Q1** in the V_{AUX} path is configured such that the V_{AUX} power supply connects to the load immediately when V_{PRIM} is disconnected for any reason and ensures continuous supply to the load.

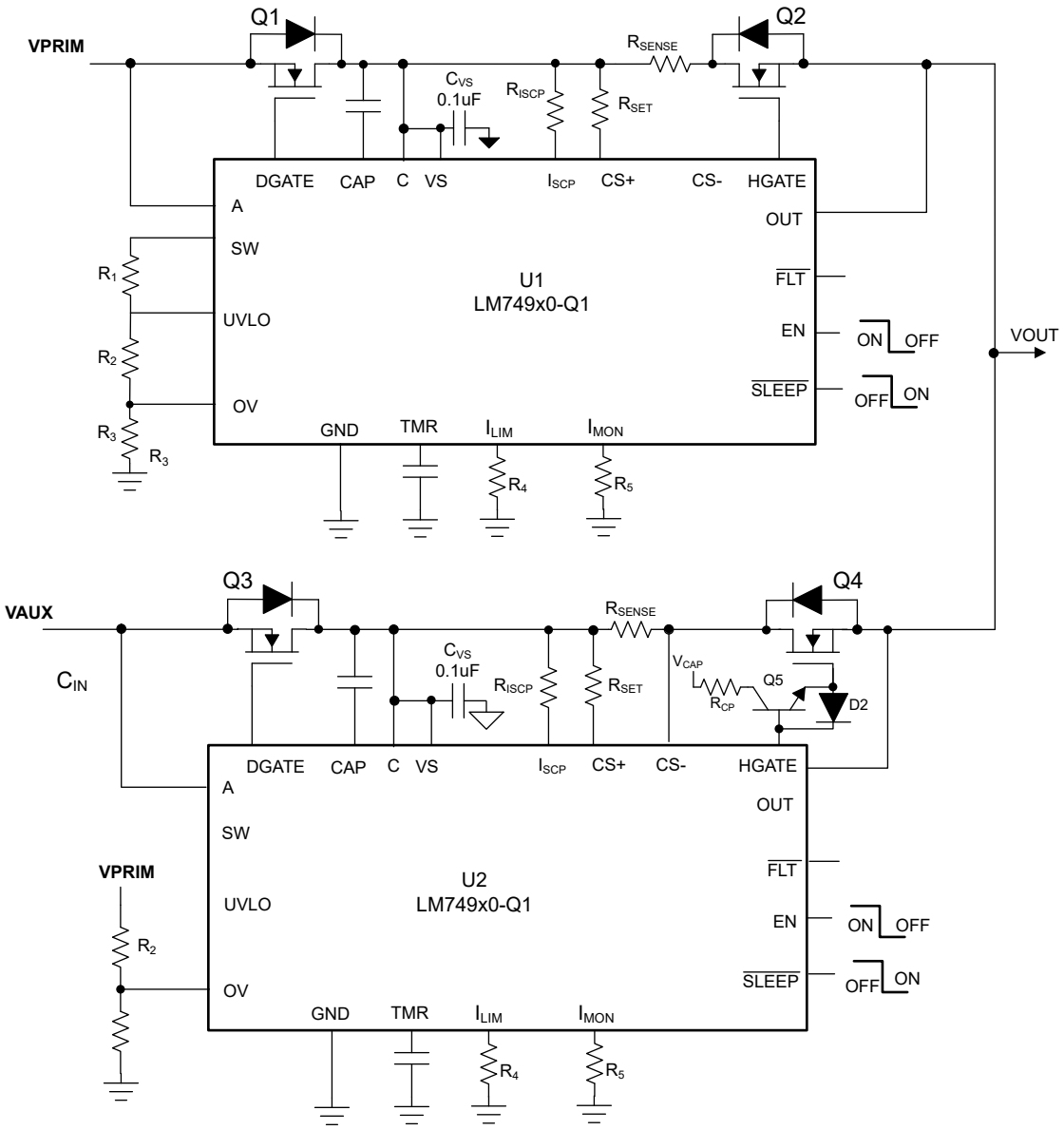

Figure 5. *Typical priority power multiplexer application circuit using the LM74900-Q1.*

A power multiplexer circuit aims to keep the output voltage drop low while the load switches to power from V_{AUX} when V_{PRIM} is cut off or out of the acceptable range. To keep the output voltage drop low during the transition, the load switch FET (Q4), driven by the **LM74900-Q1** in the V_{AUX} path, must be turned on very quickly while the power path of the V_{PRIM} is turned off (by turning off Q2). But the HGATE pin is designed to source only 55µA of gate current to achieve slow startup for inrush current limiting, which is too low to turn the HGATE high quickly. A small circuit with a resistor (R_{CP}), a transistor (Q5) and a diode (D2) can increase the HGATE source current. It is also possible to increase the gate source current by connecting the emitter of Q5 to the gate of Q4, as Q5 allows the charge-pump capacitor to pull the HGATE high directly. Alternately, you could adjust the Q4 gate source current by changing the resistor value of R_{CP}. D2 provides a path around Q5 to turn off Q4.

Figure 6 shows the waveform captured during the instance that V_{PRIM} disconnects and the load transitions to the V_{AUX} rail quickly. The HGATE of the AUX rail turns on within 20µs to reduce the drop-in output voltage.

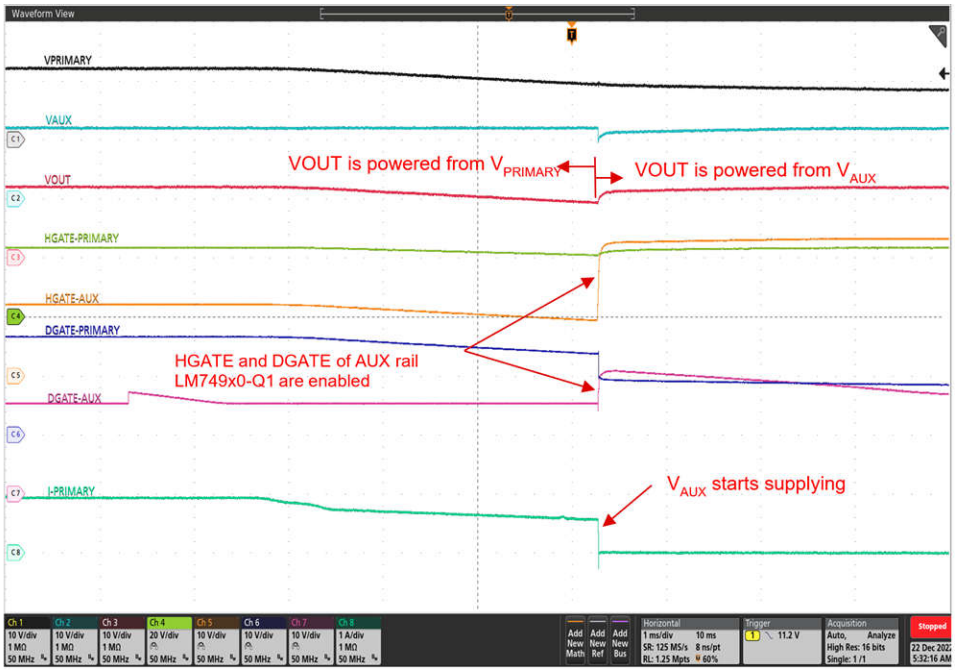

Figure 6. *V_{PRIM} to V_{AUX} switchover in a power multiplexer application*

Figure 7 shows a waveform of the instant when V_{PRIM} recovers back to an acceptable level and the priority power multiplexer circuit smoothly transitions the load with minimal voltage drop to V_{PRIM}, as it has higher priority over V_{AUX}.

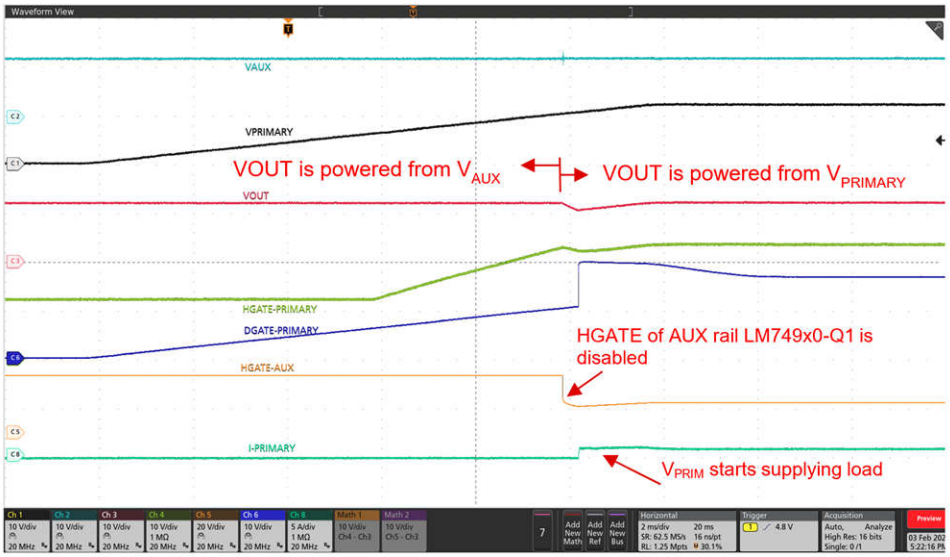

Figure 7. *V_{AUX} to V_{PRIM} switchover in a power multiplexer application.*

Table 1 shows various ideal diode controllers and the redundant supply topologies that they can support based on individual feature sets.

Ideal diode controller	ORing configuration	Power multiplexing configuration (back-to-back FET control)	
		Common drain topology	Common source topology
LM5050-1-Q1	✓	×	×
LM70700-Q1	✓	×	×
LM7480-Q1	✓	✓	✓
LM74720-Q1	✓	✓	×
LM74900-Q1	✓	✓	×
LM74930-Q1	✓	×	✓

Table 1. *List of ideal diode controllers for redundant supply topologies.*

Conclusion

Ideal diode controllers with advanced features enable the different architectures of ORing and power multiplexing circuits. Ideal diode controllers offer features and advantages such as reverse polarity protection, reverse current blocking, load dump protection, active rectification, overvoltage protection and inrush current limiting, thus enabling complete input power-path protection and helping ensure system reliability and safety.

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Low-EMI designs for isolated ADC signal-chain solutions

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Introduction

The sheer volume of electronic devices in use today, coupled with the constant reduction in the size of these devices, makes electromagnetic interference (EMI) a major problem for circuit designers. Circuits used for communications, computations and automation need to operate in close proximity [1]. Products must also comply with government electromagnetic compatibility (EMC) regulations. Virtually every country regulates the EMC of electronic products marketed or sold within its borders. In the United States, the Federal Communications Commission (FCC) regulates all commercial (nonmilitary) sources of electromagnetic radiation [2] and defines the radiated and conducted EMI test procedures in standards such as Standard C63.4 [3] from the American National Standards Institute (ANSI). Countries in the European Union (EU) regulate both electromagnetic emissions and the immunity of electronic devices; the Electromagnetic Compatibility Directive [4] basically states that equipment must comply with harmonized standards on EMC and be tested and labeled accordingly.

There are a large number of EMC standards pertaining to various types of equipment. For example, International Electrotechnical Commission (IEC) 61000 standards cover immunity requirements for most commercial products, while theComité International Spécial des Perturbations Radioélectriques (CISPR) 32 standard specifies limits on conducted and radiated emissions [5]. **Table 1** lists CISPR, European Norm and FCC standards for the relevant product sector. Many other countries outside the U.S. and EU either specify compliance with FCC or EU EMC requirements or have their own requirements. Regulations in countries outside of the U.S. and Europe often resemble the FCC or EU requirements [6].

Product sector	CISPR standard	EN standard	FCC standard
Automotive	CISPR 25	EN 55025	–
Multimedia	CISPR 32	EN 55032	Part 15
Industrial, scientific, medical	CISPR 11	EN 55011	Part 18
Household appliances, electric tools and similar	CISPR 14-1	EN 55014-1	–
Lighting equipment	CISPR 15	EN 55015	Parts 15 and 18

Table 1. *Summary of the main product standards for radiated and conducted emissions [5].*

The need for low EMI becomes even more obvious when considering a specific type of equipment, for example in smart metering. Smart electricity meters are a significant part of the future of energy distribution. They provide real time data on usage to both utilities and end users, helping people monitor energy usage and eliminating meter reading visits. The majority of smart meters connect via wireless communications [7], such as Wireless M-Bus or ZigBee, or they connect to the cellular phone network (GSM, LTE cat NB1- NB2, 2G/3G/5G). As illustrated in **Figure 1**, a smart electricity meter contains a radio-frequency (RF) transmitter circuit, usually in the same housing with the energy-metering (metrology) circuit board. It is important to minimize radiated emissions from the metrology circuit in order to not disturb RF communication, which can operate at frequencies such as 800MHz, 900MHz, 1,800MHz, 2,100MHz or 2,700MHz. The metrology circuit also needs to be resistant in terms of electromagnetic

susceptibility (the ability to withstand electromagnetic energy from wireless communication) in order to avoid billing errors from the injection of RF noise into the sensitive energy-measurement front end.

This article explains the sources of EMI – specifically radiated emissions – and present some techniques to minimize EMI for an analog signal chain, including detailed layout examples and measurement results.

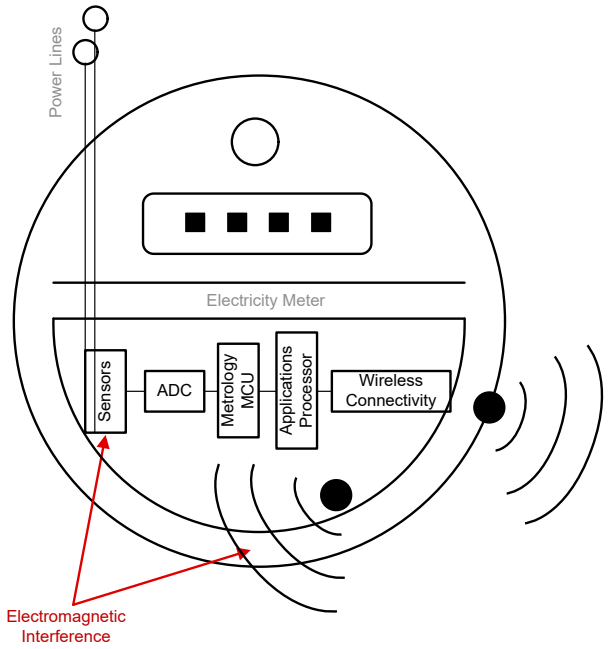

Figure 1. *An RF-enabled smart electricity meter.*

Sources of EMI and radiated emissions

EMC is the ability of an electric system to function properly in its intended environment in the presence of EMI, and to not be a source of interference to that electromagnetic environment beyond the limits as specified in the relevant standard [1].

EMI can be either radiated or conducted. Radiated interference travels in the form of radio waves, and is also called RF interference. Conducted interference comes from the magnetic field generated by current flow in cables carrying signals and power.

The focus of this article is on minimizing radiated emissions. On a printed circuit board (PCB) or inside an integrated circuit (IC) mounted on that PCB, some of the primary sources of radiated emissions include:

- Switching signals such as clocking signals, with rapid changes in voltage levels during digital signal transitions. This occurs because of the high-frequency components in the signals. Switching and clocking signals are essential for synchronizing the operation of various components within and between ICs.
- Switching regulators and other components, which cause rapid changes in current draw through power-supply lines.
- Input/output buffers, especially those associated with high-speed interfaces such as USB, HDMI or Ethernet, because of the high-speed signal transitions they handle.
- Harmonics created by nonlinear behavior in the IC's internal circuits at frequencies higher than the fundamental signals.
- Parasitic capacitance, inductance and resistance in the IC's interconnects and structures.
- Electrostatic discharge (ESD) events that trigger ESD protection circuits.

Figure 2 illustrates TI's **AMC131M03** galvanically isolated analog-to-digital converter (ADC) [8] and the predominant sources of radiated emissions resulting from its internal architecture and connections on the PCB. The ADC is used in a three-phase energy metering application, and **Figure 2** shows the circuitry for one phase (phase A). The signal chain is designed to extract voltage and current measurements for energy monitoring [8]. ADC channel 0 measures the phase current using a shunt resistor, and channel 1 measures the phase voltage through a resistive divider [8]. The most relevant contributor to emissions is the internal switching DC/DC converter (a in **Figure 1**) that generates the isolated power supply on the high-voltage side [8]. The second-highest source of radiated emissions is the digital isolation (b in **Figure 2**), as it is implemented using high-

frequency on/off keying transmission through a stacked capacitor barrier [8], [9]. Furthermore, clock signals emit radiation in a wide frequency range, such as the ADC modulator clock CLKIN (c in **Figure 2**) as well as the digital communication interface between the ADC and the microcontroller (d in **Figure 2**).

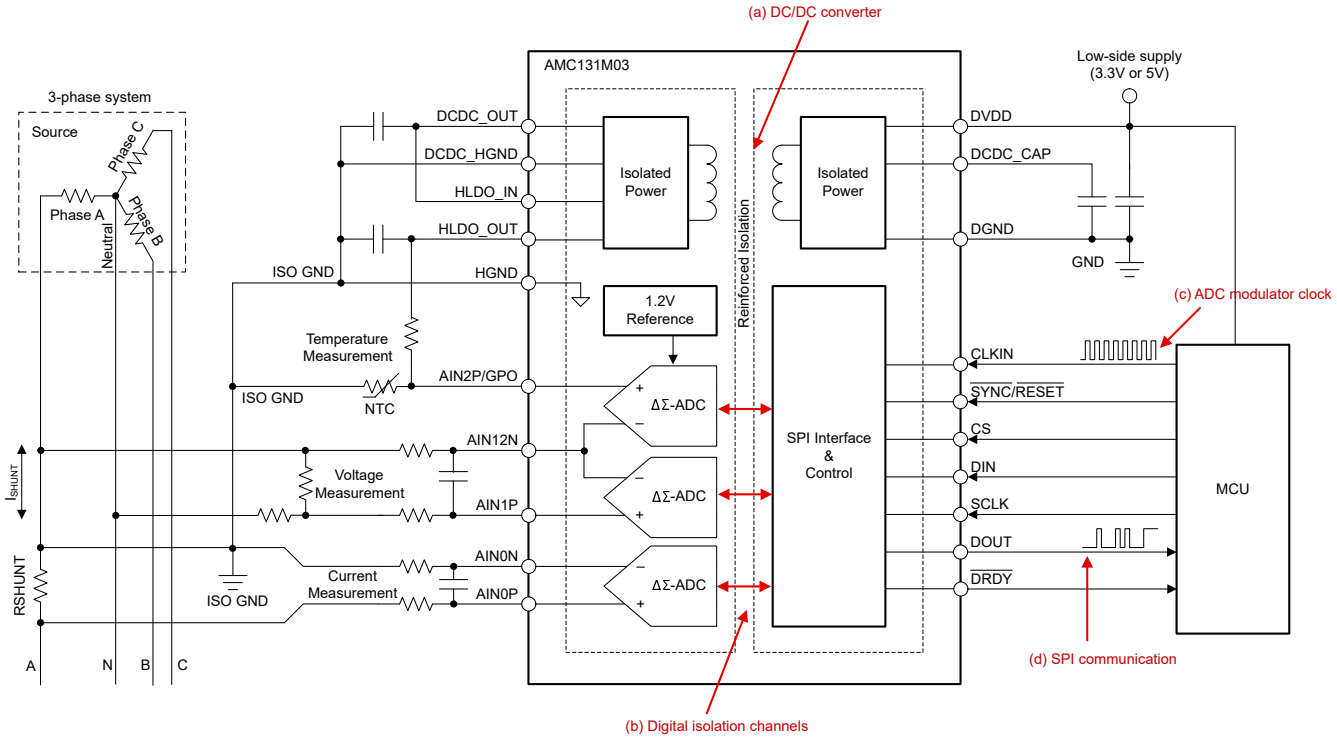

Figure 2. *Analog signal chain with an isolated ADC, and sources of radiated emissions.*

Techniques to minimize EMI

Several common PCB design techniques minimize EMI, also detailed in references [1], [10], [11]:

- Proper grounding. This is one of the most effective ways to reduce radiated emissions. Careful grounding can avoid ground loops that can act as antennas. Using a ground plane can also help reduce loop areas and provide a return path for signals, reducing the potential for EMI. In other cases, however, ground planes can create antennas on sensitive nodes and increase radiated emissions (see specific example shown in Figure 5).
- Component placement. Place components in a way that minimizes the length of signal traces, particularly for high-speed signals. Keep digital and analog components separate to avoid interference.
- Straight, short trace routing. Routing high-speed traces in a straight line and keeping them as short as possible can minimize the potential for EMI. Also, take care to avoid creating right angles in your trace routes, which can cause reflections and signal losses.
- Using decoupling capacitors. Decoupling capacitors can provide a short return path for high-frequency noise to ground. Place decoupling capacitors as close as possible to the power pins of ICs.
- Controlled impedance. Controlling the impedance of signal traces will match the impedance of the source and load and can help prevent signal reflections that can lead to radiated emissions.
- Shielding. Sometimes, using metal shields or shielding material on certain areas of the PCB can prevent radiated emissions.

- Using filters. Filters can block out certain frequencies that are causing radiated emissions, and are particularly useful in power-supply circuits.
- Layer stacking. In multilayer PCBs, take care to arrange the layers in a way that minimizes EMI. It's generally good practice to alternate between power and ground layers, as this can help reduce loop areas and provide a return path for signals. Top and bottom ground layers can help act as a shield field for internal signal layers such as clocks that generate radiated emissions.
- Avoid clock harmonics. Clock signals can generate harmonics that can interfere with other parts of the circuit. Spread-spectrum techniques can help spread these harmonics out and reduce their impact.
- EMI simulations. Radiated emissions simulation tools can help predict and minimize EMI in the PCB design phase itself [12], [13].

Figure 3 is a detailed schematic of the analog signal chain introduced in Figure 2.

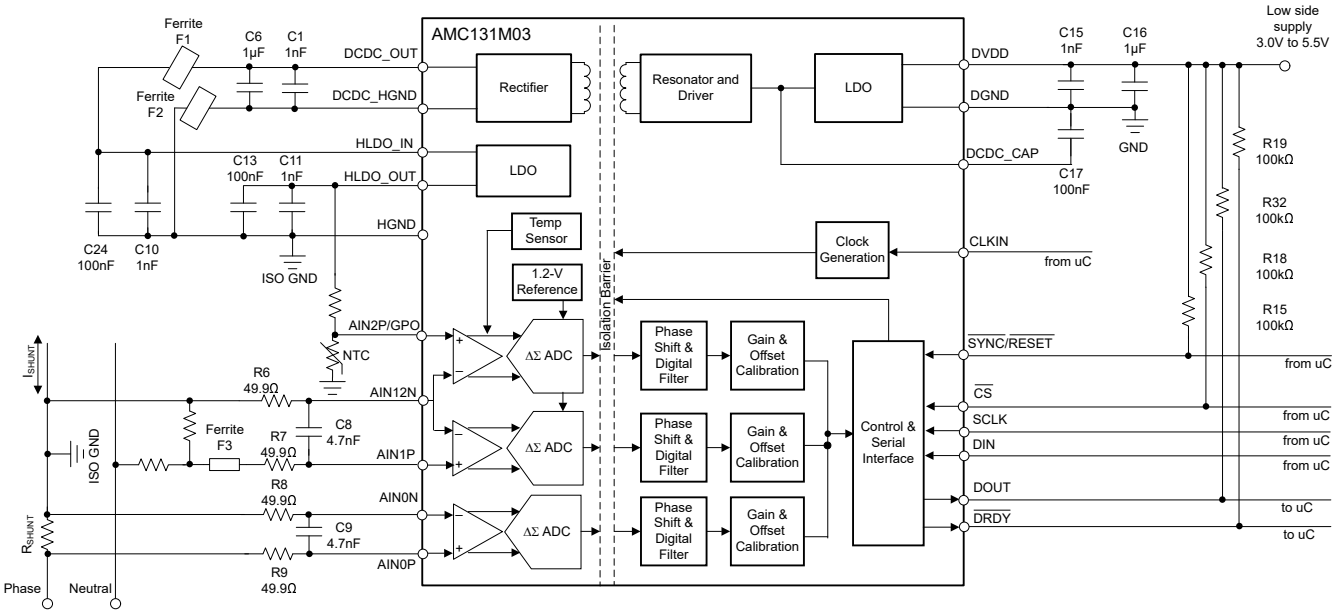

Figure 3. *Detailed schematic of the analog signal chain from Figure 2.*

Figure 4 and **Figure 5** illustrate the application of radiated emissions reduction techniques to the corresponding PCB layout for the AMC131M03. **Figure 4** shows a "good" layout, keeping traces short for ADC inputs and power routes in the high-voltage domain (PCB area to the left of the **AMC131M03** placement) and placing bypass capacitors C1, C6, C8, C9, C11, C13, C14 and C24 close to the IC.

An important aspect when mitigating EMI is the grounding scheme of the isolated ground node ISO_GND. Minimizing trace lengths and not placing a ground plane in the high-voltage domain minimizes the antenna on this node, and thus minimize radiated emissions [14]. Ferrite beads F1 and F2 are inserted into power connections DCDC_OUT and DCDC_HGND to block out high-frequency noise. You can also place an additional ferrite bead (F3) with high impedance at the frequency of excessive radiated emissions (which will depend on the PCB design) in series with the resistive divider for the voltage measurement.

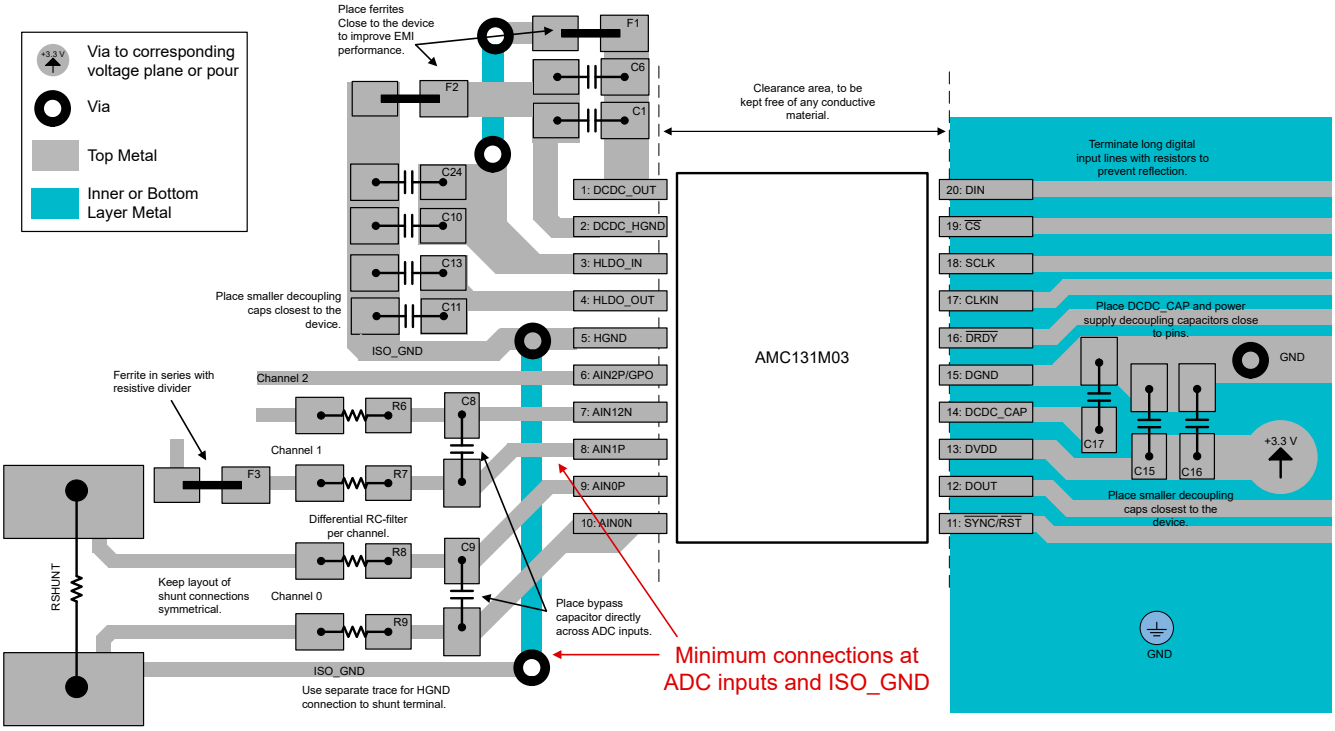

Figure 4. *Good PCB layout (low EMI).*

Figure 5 illustrates a “bad” layout, showing a ground plane connected to the ISO_GND node, which acts as an antenna and can increase radiated emissions significantly [**14**].

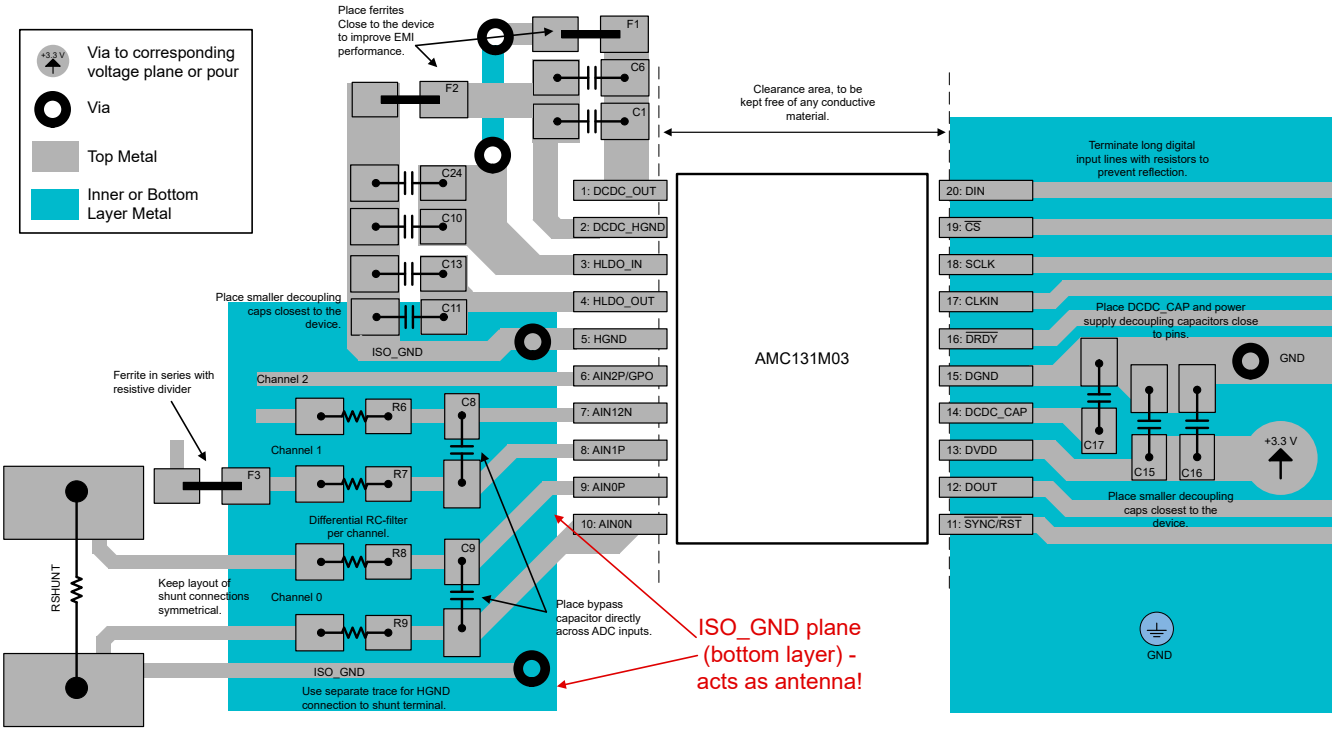

Figure 5. *Bad PCB layout (high EMI).*

Figure 6 and **Figure 7** show the radiated emissions measurement for the **AMC131M03** PCB using the layout implementation depicted in **Figure 4**. The measurements follow CISPR 11 requirements in a semianechoic chamber using a broadband antenna configured for horizontal and vertical polarizations with a 3m distance. The ADC is receiving a continuous clock at the CLKIN pin and is generating conversion results. However, there is no Serial Peripheral Interface communication while the emission profile is characterized. This design meets CISPR 11 Class A and Class B standards with 13dB of margin, offering the lowest radiated emissions performance on the market for an ADC with reinforced isolation for both data and power.

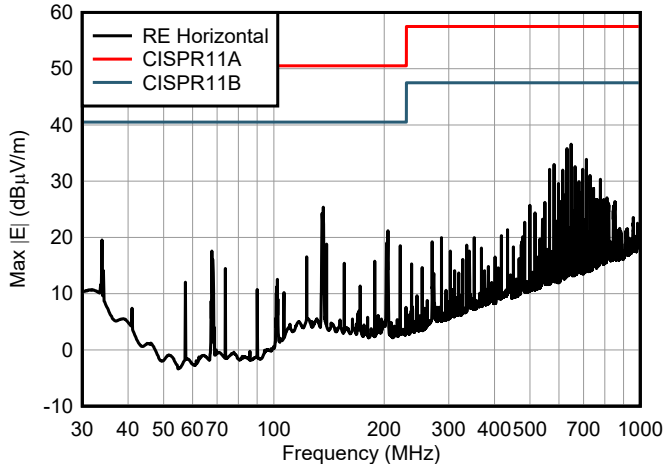

Figure 6. *Horizontal radiated emissions CISPR 11 measurement.*

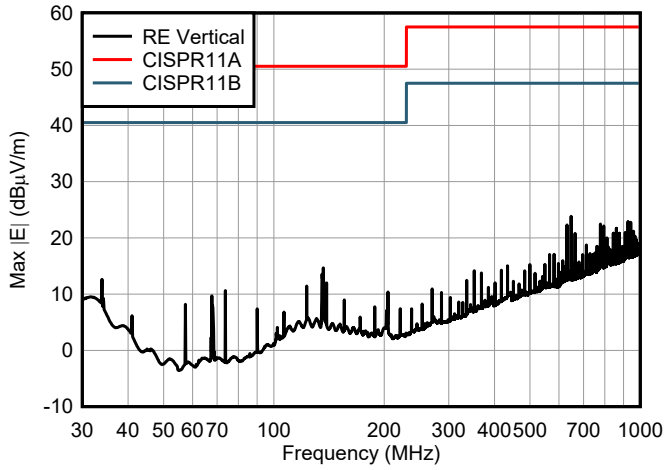

Figure 7. *Vertical radiated emissions CISPR 11 measurement.*

Conclusion

To ensure that the electronic circuits perform as designed, they must be protected from EMI. At the same time, the circuits themselves must not radiate emissions that can threaten or degrade the performance of other equipment. Compliance with EMC standards requires EMI protection at four levels: the component level, board level, system level and overall system level [15].

The techniques presented here minimize EMI at the PCB (board) design level and are easily applicable to a practical example, a best-in-class precision ADC signal chain with reinforced isolation [16] used for electricity metering. With careful design using the proposed EMI reduction techniques, the design achieves sufficient margin [17] for the relevant EMC standards.

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Solving AC dropout recovery in a high-density GaN-optimized PFC converter

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Introduction

A loss of power in data center server power-supply units can interrupt everything from entertainment to financial transactions to home security systems. Specifications such as the V2 Power Shelf Specification from the Open Compute Project (OCP) [1] emphasize the need to reduce server downtime with robust AC dropout control algorithms. In addition, the need for cost-effective solutions in data centers to improve power factor correction (PFC) light load and peak efficiency while shrinking passive components is becoming difficult with conventional continuous conduction mode control [2-8].

To address this problem, TI developed a gallium nitride (GaN)-based high-density design using two-phase integrated triangular current mode (iTCM) PFC (**Figure 1**) [9]. Low-value inductors operating at a high frequency have enabled the high efficiency (>99%) and power density (120 W/in^3) of this design. These small inductors present a unique problem to AC dropout recovery in that only a few microseconds of switch on-time can result in over 70 A of switch current. In addition, any delays in timing can also result in significant reverse current, further exacerbating PFC recovery. Keeping the current levels at a safe magnitude and preventing reverse current required the development of a new solution to the AC dropout and recovery problem. This article discusses this solution with lab verification data based on the Variable-Frequency, ZVS, 5-kW, GaN-Based, Two-Phase Totem-Pole PFC Reference Design [10], for which **Table 1** lists the primary components and system specifications.

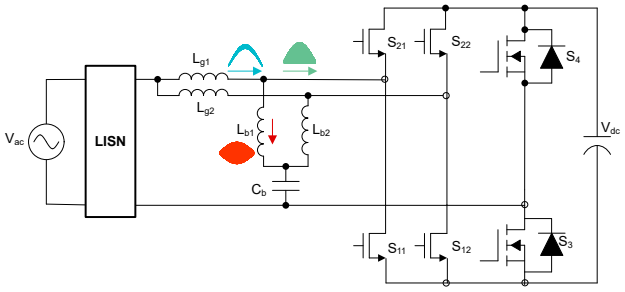

Figure 1. *iTCM topology with inductor and current envelopes.*

Parameters	Value
AC input	90 V-264 V
Line frequency	50-60 Hz
DC output	400 V
Maximum power	5 kW
Holdup time at full load	20 ms
L_g, low-frequency inductor	140 µH
L_b, high-frequency inductor	14 µH
C_b, high-frequency blocking capacitor	1.5 µF
Total harmonic distortion (THD)	OCP v3
Electromagnetic interference (EMI)	European standard (EN) 55022 Class A
Operating frequency	Variable, 75 kHz-1.2 MHz
Microcontroller	TMS320F280049C [11]
High-frequency GaN field-effect transistors (FETs) (S_{11}, S_{12}, S_{22}, S_{21})	LMG3526R030 [12]
Low-frequency silicon FETs (S_3, S_4)	IPT60R022S7XTMA1
Dimensions	38 mm ´ 65 mm ´ 263 mm
Power density	120 W/in^3

Table 1. *iTCM topology with inductor and current envelopes.*

Topology overview

The topology uses two phases operating 180° out of phase with a single DC blocking capacitor, C_b, taking advantage of the ripple current cancellation provided by the two-phase architecture and reducing the root-mean-

square (RMS) current stress in C_b. L_{b1} and L_{b2} are sized to process the high-frequency AC ripple current necessary for TCM operation, removing the DC bias burden required for the inductor used in TCM, as defined in [5]. Using ferrite cores for L_{b1} and L_{b2} ensures low loss in the presence of the high flux swings necessary for zero voltage switching (ZVS). L_{g1} and L_{g2} are larger in value than L_{b1} and L_{b2} (approximately 10 times larger), preventing most of the high-frequency current from flowing into the input source and subsequently improving EMI. In addition, the reduced ripple current in L_{g1} and L_{g2} enables the possible use of lower-cost core materials. **Figure 1** also illustrates the ripple current envelopes for the inductors and switch nodes.

AC dropout technical challenges

The first challenge that I want to highlight is reverse-current generation when the AC input voltage disappears. Since all of the switches in the totem-pole PFC topology are bidirectional, it is essential that the FETs operating as synchronous rectifiers shut off as quickly as possible when removing AC. This shutoff prevents the generation of a negative current that will cause the output voltage to discharge and reduce the available holdup time. **Figure 2** illustrates the path for generating this negative current for the synchronous conduction interval during the positive half cycle. In addition, any substantial delays in turning off the synchronous rectifiers can also result in a large current spike capable of activating overcurrent protection (OCP). For example, if the synchronous rectifier stays on when no input voltage is present, you can solve $V_{dc} = L_{b1} \cdot \frac{dI_1}{dt}$ for the amount of time it takes to generate 70 A of current, namely 2.5 µs. This short time presents a significant problem for the AC dropout detection to identify the problem and stop switching before the system hits OCP or causes damage.

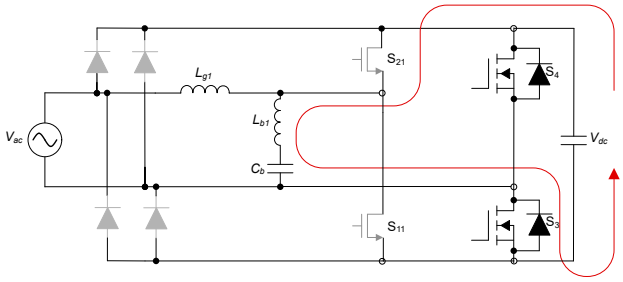

Figure 2. *Synchronous rectifier S_{21} delayed turnoff V_{dc} discharge path.*

The second challenge is resuming operation of the PFC after restoring AC. The central issue of this event comes from the fact that the bypass diodes on the PFC charges the output voltage to the peak of the input sine wave, which occurs most readily at high line when the output voltage has fallen well below this peak value. During these events, the converter has no mechanism to stop the current, making the surge current very large. Improper control of the switches during these events can make things much worse by saturating the inductors, creating OCP events and further discharging the output voltage. The need for a precise control algorithm during this time is again multiplied by the high-frequency operation point of the iTCM topology with the small-value inductors used for L_{b1} and L_{b2}.

AC dropout solution

In order to precisely determine the presence and absence of the AC input, the solution uses a virtual AC input signal that monitors the integrity of the actual AC input. This virtual signal is generated by measuring the input voltage amplitude, frequency and phase, such that during normal operation it tracks the 50- and 60-Hz component of the actual AC input nearly perfectly. The system can easily recognize the presence and absence of the AC input voltage by comparing the actual input to the virtual input. Any sudden changes in the difference between these two signals indicates an input transient event. It is this transient event that is used to detect both the loss and restoration of the AC input voltage. **Figure 3** illustrates the virtual AC input, along with the actual input during a dropout event.

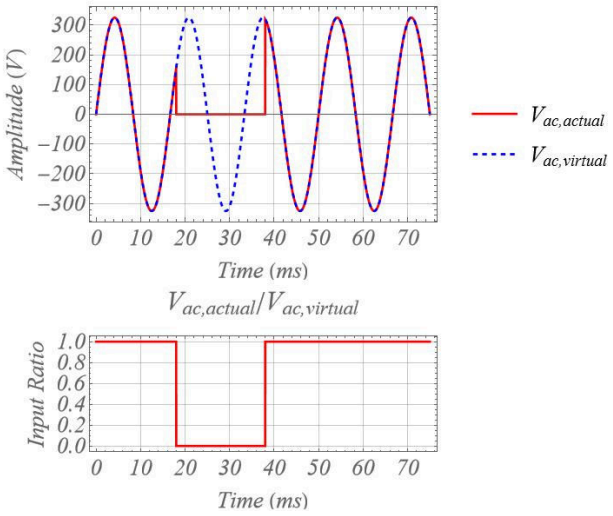

Figure 3. *AC input dropout with the virtual AC signal.*

Figure 4 illustrates the state machine that governs the dropout and restore process. During startup, the system goes through an initialization cycle (Sync Init) where it determines the RMS input voltage magnitude. It uses a software phase-locked loop (SPLL) to ensure that the phase of $V_{ac,virtual}$ matches $V_{ac,actual}$. Once the SPLL is locked (Sync On), the processor monitors the ratio between $V_{ac,actual}/V_{ac,virtual}$ (see **Figure 3**). If this ratio is less than the target threshold, then a dropout event is declared and switching stops immediately (Stop State). From here, the system clears any faults that occurred and goes into a standby state (Ready), where it monitors the $V_{ac,actual}/V_{ac,virtual}$ ratio to determine when it goes above the resume threshold. Once the state machine has determined that AC is restored, it resumes switching immediately and resynchronizes the SPLL (Resume State). By using the $V_{ac,actual}/V_{ac,virtual}$ ratio in concert with the SPLL, the algorithm is able to determine the AC dropout and restore times for any input voltage or frequency. In addition, since the algorithm always monitors the ratio $V_{ac,actual}/V_{ac,virtual}$, it is able to respond more quickly than a traditional level-based-solution that detects when the AC input voltage goes to zero. Level-based monitoring for dropout can create delays that can result in large current spikes and significant reverse current.

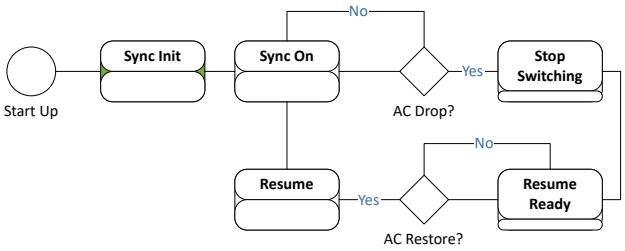

Figure 4. *AC dropout and restore state machine.*

Results

Figure 5 illustrates the performance of the two-phase iTCM totem-pole PFC with the aforementioned algorithm during an AC dropout and restore event. The AC input voltage is 230 V_{RMS} at 60 Hz and the output voltage is 400 V. The load is 5 kW (400 V, 12.5 A) of constant current with a 20-ms AC dropout event. In order to produce the worst-case stress for the system, AC was removed such that it would return at the peak of the AC line cycle. This is the worst case for inrush current, in that the input bypass diodes will cause significant inrush current into the output capacitors when the AC line peak exceeds V_{OUT}.

The waveform in **Figure 5** also provides an image zoomed in on the recovery portion of the event. It is clearly visible that the PFC switch current is well controlled and below the GaN FET OCP limit [12]. Minimized reverse current prevents unnecessary discharge of V_{OUT}. In addition, there is no abnormal behavior from the bypass diode conduction intervals, since the algorithm is able to easily determine whether the input voltage is above or equal to the output voltage.

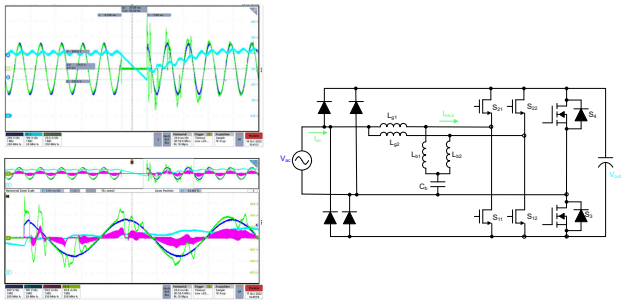

Figure 5. *AC dropout and restore performance at 5 kW.*

In addition to AC dropout, the design also delivers low THD, high efficiency, high power density and fast load transient response.

If you are interested in more details on this algorithm or other aspects of this design, you can find the full schematics, layout, bill of materials, test results and code for the two-phase totem-pole PFC reference design in reference [10].

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