Application Report
SBOA355–May 2019

Trade-offs Between CMOS, JFET, and Bipolar Input Stage Technology

Marek Lis

1 Trademarks

All trademarks are the property of their respective owners.

2 Introduction

What is the difference between CMOS, Bipolar, and JFET input amplifiers, and when should one be used over the other? This application note addresses some of the key differences between the various process technologies to help choose the best amplifier for a specific design application. Since noise is a key specification in many signal chain designs, it is compared for JFET, CMOS, and bipolar op amps, along with other specifications like:

- Input impedance
- Input voltage offset
- Offset drift
- Input common-mode voltage range

3 Flicker Noise Comparison

Flicker noise (1/f) is a critical consideration for low frequency analog applications like buffering data converters, amplifying strain-gauge signals, and pre-amplifying microphone outputs. To select an appropriate amplifier, an engineer must first understand the noise parameters for a particular application, and then determine whether an amplifier is indeed low noise. Therefore, it is imperative that the designer understands how the type of IC (bipolar, JFET-input, or CMOS-input) affects overall noise performance.

In order to illustrate the differences between various processes, this application note takes a closer look at three op amps with comparable bandwidth: the OPA2210 (bipolar), OPA828 (JFET), and OPA2156 (CMOS) – see Figure 1. A flicker voltage noise corner is often considered a figure of merit. The noise corner is at the frequency where 1/f and broadband noise curves intersect. The 1/f noise corner is at much higher frequency for most CMOS (non-zero drift) devices, and for that reason, board designers often use bipolar op amps with a much lower 1/f corner in low frequency designs.

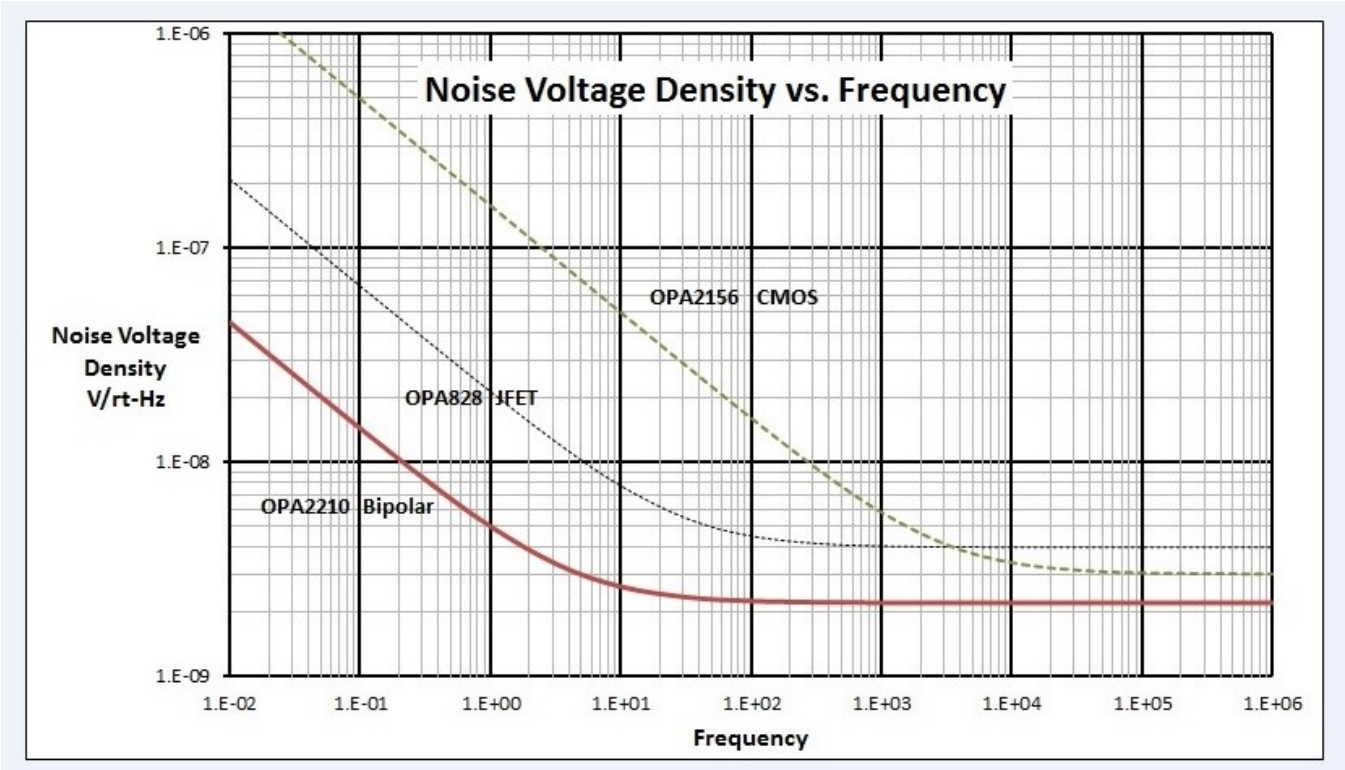

Figure 1. Input Noise Voltage Density Versus Frequency

Having said that, due to inherent nature of zero-drift (CMOS) amplifiers, where any low-frequency signals like input voltage offset and drift are cancelled out, these also eliminate 1/f voltage noise in chopper amplifiers while flicker noise in auto-zero op amps may be lowered down to two times of the broadband noise value. However, one should be aware that the zero-drift amplifiers generate short duration input current spikes caused by the action of the front-end switches that may be converted into voltage spike across high input source impedance, resulting in the effective increase in the input voltage offset. For that reason, it is critically important to balance the impedance at each input terminal by making them equal.

4 Broadband Noise Comparison

Broadband noise (white noise) is inversely proportional to the square-root of the trans-conductance (gm) of the input differential pair. Since gm of bipolar transistor is directly proportional to the collector current, gm = q × Ic / (k × T), while gm in CMOS is proportional to the square-root function of drain current, gm = sq-rt(2 × Id × u × Cox × W/L) for the given bias current, meaning the broadband noise in the bipolar device is the lowest. This can be seen in Figure 1, where the bipolar OPA2210 (with a quiescent current of 2.2 mA) has lower broadband noise (2.2 nV/rt-Hz) than either 3 nV/rt-Hz in the OPA2156 (CMOS) with an IQ of 4.4 mA, or 4 nV/rt-Hz in the OPA828 (JFET) with an IQ of 5.5 mA. This means that for high-bandwidth applications where broadband noise dominates the total noise, bipolar input devices are most efficient in terms of lower noise versus IQ. This is true for as long as the higher input current noise in bipolar devices (caused by higher IB) does not dominate the total integrated noise, as may be the case in high input impedance designs. Therefore, since the op-amp input current noise is proportional to the square root of the input bias current, Inoise = sq-rt(2 × q × IB), JFET input op amps (with IB comparable to CMOS and a low 1/f corner similar to a bipolar device) might be the best choice in obtaining the lowest possible total noise in high-input impedance applications. In other words, due to low IB in JFET input op amps, users get low current noise close to CMOS devices and low 1/f noise corner that is similar in performance to bipolar devices

5 Input Common-Mode Impedance

The input impedance of an amplifier must be as high as possible (ideally infinite) so it does not load the voltage source, as this adversely affects a gain of the previous stage, and may limit the frequency response of the application. The input resistance of an op amp can be directly determined from the graph of the input bias current versus the input common-mode voltage, where Rin = ΔVcm / ΔIB (see the graph of OPA828, IB versus Vcm, as shown in Figure 2) IB versus Vcm. Since the input bias current in CMOS and JFET input op amps is typically many orders of magnitude lower than in bipolar amplifiers, the input resistance in CMOS and JFET op amps is much higher than in bipolar devices; 6×10^{12} (Tera-Ω) in the OPA2156, 1 TΩ in the OPA828, and 1 GΩ in the bipolar OPA2210 — a typical Rin is even lower in most bipolar op amps (<1 MΩ).

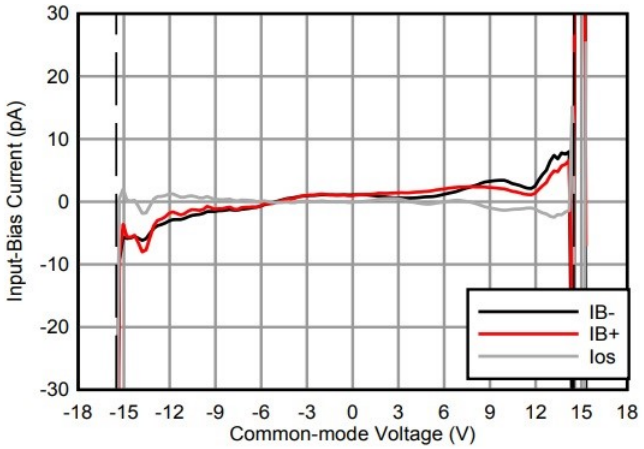

Figure 2. Input Bias Versus Input Common-Mode Voltage

The input bias current in CMOS and JFET amplifiers is caused by the leakage of reverse-biased pn junction, and thus doubles with each 10°C rise in junction temperature. This may result in a three orders of magnitude (2^10) increase in IB over a 100°C rise in temperature. In bipolar devices, however, IB variation with temperature is much more limited, since it is mainly tied to the variation of bipolar transistor Beta (β).

6 Input Voltage Offset and Offset Drift

In general, because of the different, physical inner-workings of bipolar and MOSFET transistors, expect to see tighter, natural (unadjusted) offset, and linear offset drift in bipolar devices – see Figure 3. In fact, in bipolar op amps, offset and drift are closely correlated where for each one millivolt of offset voltage at 25°C, one can expect to get about 3.3 µV/C of offset drift; Vos_drift = Vos(T) / (T + 273°C). This means that trimming the input offset voltage to zero assures that drift is also close to zero. However, when it comes to JFET and CMOS devices, there is no such correlation between input offset voltage and drift, and the drift can be non-linear and non-monotonic – see Figure 4.

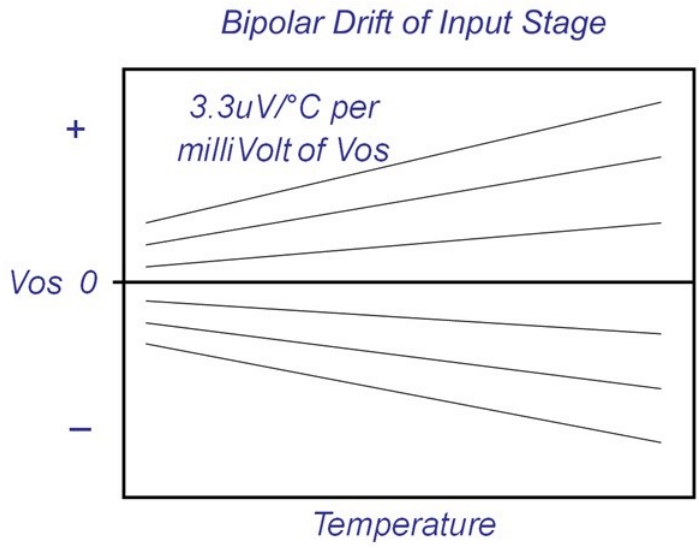

Figure 3. Input Offset Voltage Versus Temperature in Bipolar Input Op Amp

Even though the natural offset and inherent drift are typically much higher in CMOS devices than in bipolar op amps, the offset and drift in precision CMOS products are typically lower than in bipolar. This is because the precision CMOS op amps get package-level trimmed, or use auto-calibration circuitry, to null the offset and drift. Bipolar devices may, at best, be trimmed at the wafer-level, which is prone to packaging shifts.

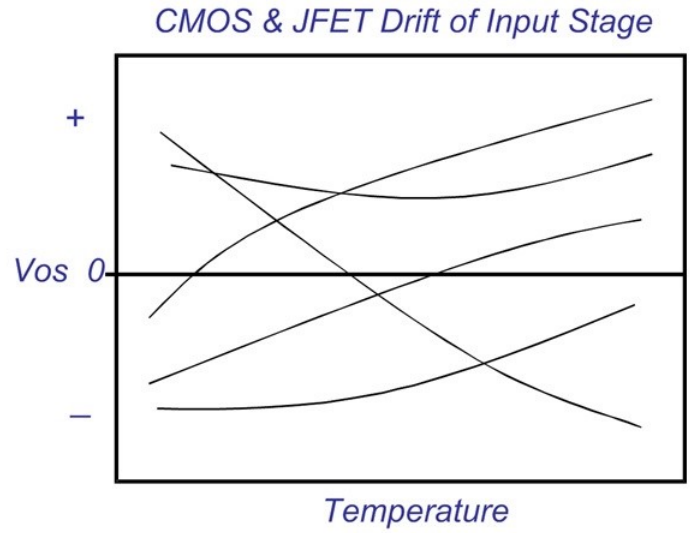

Figure 4. Input Offset Voltage Versus Temperature in CMOS and JFET Input Op Amp

In short, even though it is inherently easier to get tighter initial offset and offset drift using bipolar processes, CMOS technology allows the implementation of auto-calibration circuitry like chopper, auto-zero, or post-package trims (e-trim). This circuitry is capable of adjusting of the input offset voltage to less than 5 µV (see the OPA388), and the offset voltage drift down to 15 nV/C (OPA187).

7 Input Common-mode Voltage Range

The input common-mode voltage range in CMOS amplifiers may extend all the way to the rails of the device. This is possible by using two input differential pairs: a p-channel pair covering the input voltage range from a negative rail up to 1 V to 2 V below the positive supply, and an n-channel pair covering the upper range of the input common-mode voltage range all the way to the positive rail (see the OPA1671). Since the two input transistor pairs have two independent and uncorrelated input offset voltages, when the input common-mode voltage changes, it causes transition between the pairs, and thus the offset voltage value abruptly changes resulting in the input crossover distortion — see Figure 5.

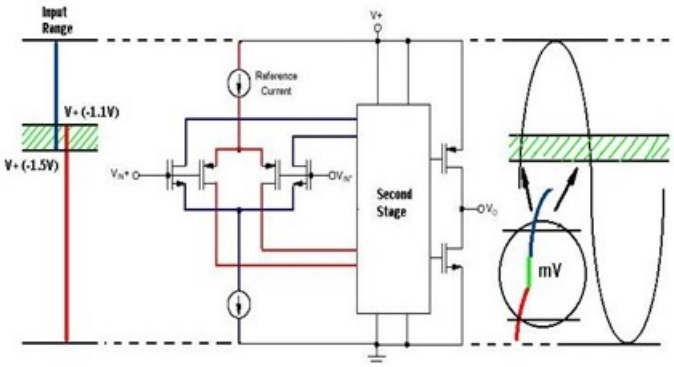

Figure 5. Traditional Rail-to-Rail Input Stage Topology

In order to alleviate the problems related to cross-over distortion, some op amps include internal charge-pump, which raises the internal supply voltage biasing the input differential pair just enough to overcome the Vgs plus Vsat positive rail limitation of p-channel pair – see Figure 6. This approach eliminates the need for use of n-channel pair, and thus greatly improves the linearity of the input stage across the entire input common-mode voltage range – see OPA325.

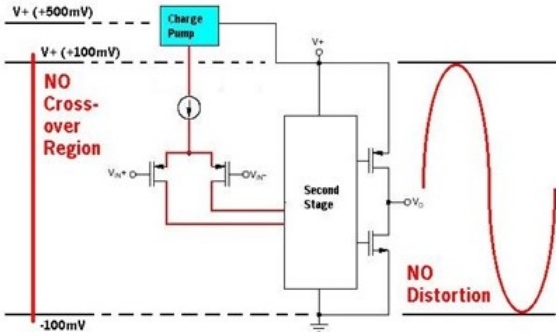

Figure 6. Zero Crossover Rail-to-Rail Input Stage Topology

One concern that often accompanies charge pump circuits is that they use switched capacitors to obtain the necessary increase in the supply voltage. Such switching typically generates noise, but in the case of the OPA325, the amount of noise is minimized by the very low ripple design. However, the charge pump noise may also feed through the external power supply into the signal path. If that happens, it might be combined with other power supply noise sources and create harmonics of the charge pump signal. For this reason, it may be necessary to look closely and include proper decoupling on the op amp power supply pins. In some cases, use of ferrite beads between the amplifier supply pin and other sensitive circuits may also benefit overall board design.

8 Summary

In board-level design, an engineer must clearly understand the technology trade-offs between different op amp parameters like voltage versus current noise, source impedance, effective bandwidth and so forth, since they all may influence the specifics of the application. A lower broadband voltage noise of the bipolar op amp for a given quiescent current, frequently results in a higher total integrated noise because of the higher bandwidth, unless the bandwidth is limited by other means. Likewise, the lower voltage noise of the bipolar input stage may often be overwhelmed by its much higher current noise interacting with high source impedance. All in all, in order to achieve optimal system performance, a board-level designer must thoroughly understand the application to consciously decide when to choose one op amp technology over the other.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265