Analog Engineer's Circuit

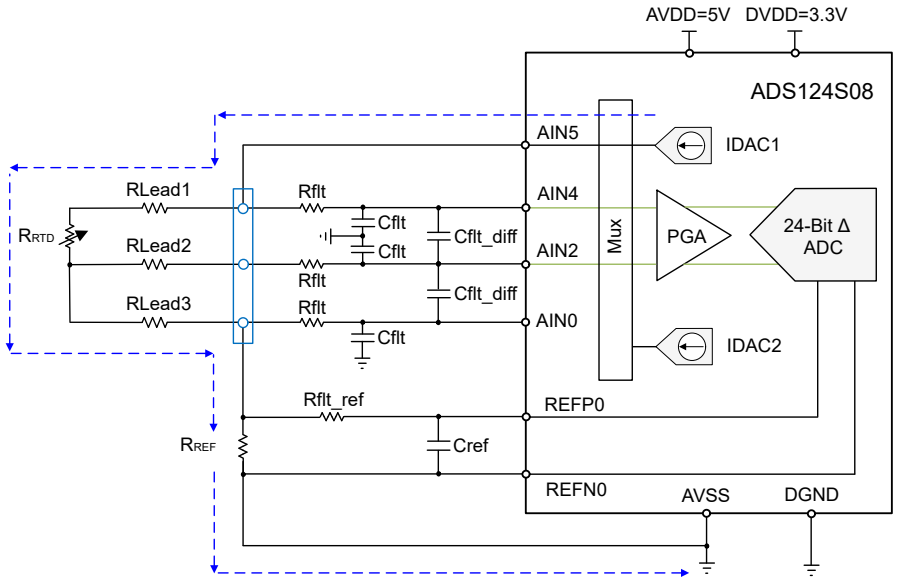
Circuit for Protecting ADS124S08 ADC from EOS for RTD Measurement

Data Converters *Dale Li*

Specification		Minimum	Maximum
Overstress Signal	Voltage (V_{EOS})	–30 V	+30 V
Absolute Maximum Input Voltage Rating – ADC (AVDD = 5 V, AVSS = 0 V)	Voltage – Analog Input (V_{in_Abs})	AVSS – 0.3 V	AVDD + 0.3 V
	Current – Analog Input (I_{in_Abs})	–10 mA	+10 mA

Design Description

This circuit shows a solution to protect ADS124S08 delta-sigma ADC from electrical overstress (EOS) for a resistance temperature detector (RTD) application. The protection circuit is designed to provide protection against a ±30-V DC continuous fault as well as a much higher transient fault. Protection against the ±30-V DC fault is needed in case the input terminals are inadvertently connected to the DC supply. The ±24 V is a standard DC supply in industrial systems, so ±30-V protection provides a design margin. The solution is developed for 3-wire RTD input with PT100 RTD sensor and the protection method can also be used for 2-wire, 4-wire RTD input and PT1000 RTD sensor. The protection circuitry includes an external transient voltage suppressor (TVS) diode and a current-limiting resistor to implement an external protection clamp for overstress signal and maintain a minimum impact on measurement accuracy. This circuit is useful in the temperature controller and analog input module of the *Programmable Logic Controller* in factory automation and control system. For protecting high-voltage SAR ADC from electrical overstress, see the *Input protection for high-voltage ADC circuit with TVS Diode* and *Circuit for protecting ADC with TVS diode and PTC fuse* circuit designs. For protecting low-voltage SAR ADC from electrical overstress, see *Circuit for protecting low-voltage SAR ADC from electrical overstress with minimal impact on performance*.



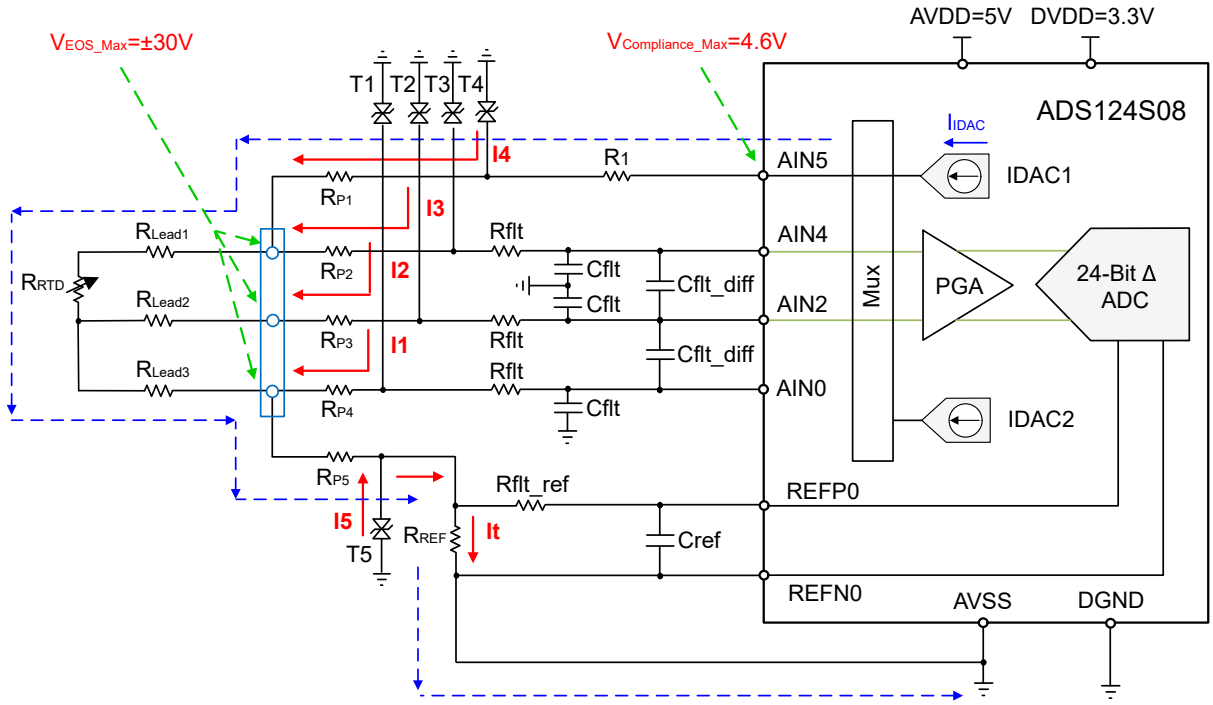
Typical Circuit for 3-Wire RTD Measurement Without Protection

Design Goals

System Specification	Goal	Measured
Overstress Voltage	±30 V	No damage on ADS124S08
Accuracy (uncalibrated, –40°C to 85°C)	±0.5%	< ±0.05%

Design Notes

1. The SMBJ14CA bidirectional TVS diodes from Bourns® are selected to protect each input of the ADS124S08 from electrical overstress signals by considering:
   - Select SMBJ series TVS diode for proper package size and the ability of 600-W power dissipation
   - Select bidirectional 14-V standoff voltage for minimum power dissipation on current-limiting resistors
2. The current-limiting resistors R_{P1}, R_{P2}, R_{P3}, R_{P4} and R_{P5} are used to limit fault current for protecting the TVS diodes and ADC, also helping to clamp the input overstress signal on the diodes by selecting the proper resistor value. The high-resistance value of R_{P2}, R_{P3}, R_{P4}, and R_{P5} is exactly the same as the resistance value of R_{P1} to avoid any additional errors caused by the resistance mismatch when the leakage current of TVS diodes flows through these resistors. Note that the R_{Lead1}, R_{Lead2}, and R_{Lead3} in *Input Protection Circuity for ADC From Electrical Overstress* are equivalent lead wire resistance.
3. Keep the capacitance value of differential capacitor ≥ 10 × common-mode capacitor. Keep the bandwidth of differential filter ≥ 10 × data rate.
4. See the Electrical Overstress on Data Converters in the TI Precision Labs - ADCs video series. This series discusses the details on protection solutions for different types of data converters including theoretical explanation, diode selection, current-limiting resistor selection, and test result.



Input Protection Circuity for ADC From Electrical Overstress

Component Selection

1. The ADC input voltage range is set as the maximum voltage (V_{in_Abs}) before turning on the internal ESD diode. The input current range is the maximum current that the internal ESD diode can support continuously.
2. The maximum voltage on ADS124S08 is 5.3 V when the AVDD is 5 V, so any positive electrical overstress signal higher than which 5.3 V should be clamped for protecting the input of the ADS124S08. In this solution, the SMBJ14CA bidirectional TVS diode is selected to protect the ADC from an electrical overstress signal. This diode will break down between 15.6 V and 17.9 V and limit the input voltage. This voltage level exceeds the absolute maximum of the ADC, but current-limiting resistors in conjunction with the ADS124S08S internal ESD diodes will protect the device.

Part Number	MFG	Reverse Standoff Voltage (V_R)	Breakdown Voltage (V_{BR})		Clamping Voltage Max (V_C at I_{PP})	Reverse Leakage Max (I_R at V_R)	Peak pulse Current (I_{PP})	Peak Power Dissipation (P_{PP})	Steady State Power Dissipation (P_{PP})
			Min	Max					
SMBJ14CA	Bourns	14 V	15.6	17.9	23.2 V	1 µA	25.9 A	600 W	5 W

3. This design shows a protection solution for a single IDAC current, low-side external reference and 3-wire RTD measurement. The current-limiting resistor R_{P1} in the IDAC channel AIN5 is more critical because the node voltage on the AIN5 pin is limited by the maximum compliance voltage which is 4.6 V for 5-V AVDD supply. A high-resistance value of R_{P1} and R_1 is helpful to limit fault current and protect the ADC in a fault condition; however, the high-resistance value of these resistors increases the voltage on the AIN5 pin in a normal operation to violate the compliance voltage. The protection solution is designed to protect the ADC from miswiring ±24-V power supply to the input of RTD measurement circuit. The ±30-V fault signals are considered for a design margin. The absolute maximum input current rating of ADS124S08 is ±10 mA, so ±5-mA current is used for a margin and limit flowing into ADC input and ±25-mA total fault current is limited to flow through R_{P1}.

EOS Fault Voltage		ADC Input Voltage (Abs)		ADC Input Current		Fault Current	
V_{EOS_max}	+30 V	V_{in_max}	+5.3 V	I_{ADC_max}	+5 mA	I_{fault_max}	+25 mA
V_{EOS_min}	–30 V	V_{in_min}	–0.3 V	I_{ADC_min}	–5 mA	I_{fault_min}	–25 mA

The R_{P1} and R_1 are determined by the largest resistor values from the following equations:

For positive overstress voltage +30 V,

$$R_{P1} \geq \frac{V_{EOS\_max} - V_{BR\_min}}{I_{fault\_max}} = \frac{30\ V - 15.6\ V}{25\ mA} = 576\ \Omega \left(\text{round up to standard } 590\ \Omega\right)$$

$$R_1 \geq \frac{V_{BR\_min} - V_{in\_max}}{I_{ADC\_max}} = \frac{15.6\ V - 5.3\ V}{5\ mA} = 2.06\ k\Omega \left(\text{round up to standard } 2.2\ k\Omega\right)$$

For negative overstress voltage –30 V,

$$R_{P1} \geq \frac{V_{EOS\_min} - \left(-V_{BR\_min}\right)}{I_{fault\_min}} = \frac{-30\ V - (-15.6\ V)}{-25\ mA} = 576\ \Omega \left(\text{round up to standard } 590\ \Omega\right)$$

$$R_1 \geq \frac{-V_{BR\_min} - V_{in\_max}}{I_{ADC\_min}} = \frac{-15.6\ V - (-0.3\ V)}{-5\ mA} = 3.06\ k\Omega \left(\text{round up to standard } 3.4\ k\Omega\right)$$

The larger value 3.4-kΩ resistor is selected for R_1 and a 590-Ω resistor is selected for R_{P1}.

In the following equations, the dissipated power is calculated in R_1 and R_{P1} during a negative electrical overstress fault event which is the worst case for these resistors. The objective is to make sure that the correct power rating is used on the resistors, R_1 and R_{P1}.

$$P_{RP1} = \frac{\left(V_{EOS\_min} - \left(-V_{BR\_min}\right)\right)^2}{R_{P1}} = \frac{(-30\ V - (-15.6\ V))^2}{590\ \Omega} = 351\ mW$$

Hence, the P_{RP1} is selected as 0.5 W for R_{P1} with extra design margin.

$$P_{R1} = \frac{\left(-V_{BR\_min} - V_{in\_min}\right)^2}{R_1} = \frac{\left(-15.6\ V - (-0.3\ V)\right)^2}{3.4\ k\Omega} = 68.85\ mW$$

Hence, the P_{R1} is selected as 0.1 W for R_1 with extra design margin.

4. The resistance of the PT100 sensor is approximately 20 Ω at –200°C and 400 Ω at +850°C. The resistance of R_{REF} is determined by the maximum voltage across the PT100 (R_{RTD}) when the I_{IDAC} current flows through the PT100. The 0.5-mA single I_{IDAC} current from AIN5 is selected and configured to keep the error low which is caused by self-heating on the PT100. The PGA gain on the ADS124S08 is set to 4. The minimum voltage (V_{REF_min} **)** on the R_{REF} is calculated by the following equations:

$$V_{RTD\_max} = I_{IDAC} \times R_{RTD\_max} = 0.5\ mA \times 400\ \Omega = 0.2\ V$$

$$V_{REF\_min} = V_{RTD\_max} \times Gain = 0.2\ V \times 4 = 0.8\ V$$

The voltage (V_{REF}) on the R_{REF} is set to 1 V for a margin. The resistance of R_{REF} is determined by the following equation:

$$R_{REF} = \frac{V_{REF}}{I_{DAC}} = \frac{1\ V}{0.5\ mA} = 2\ k\Omega$$

5. The input resistor in parallel with differential and common-mode capacitors in other channels is used to filter the noise from the front-end circuit. The exact resistor value is not critical because there is no compliance voltage limit on these channels and there is no IDAC current flowing through it.

$$R_{flt} > R_1 = 3.4\ k\Omega$$

$$R_{flt} < 10\ k\Omega$$

$$\Rightarrow R_{flt} = 4.99\ k\Omega$$

$$f_{in\_Diff} > 10 \times Data\_Rate$$

$$Data\_Rate = 200\ Hz$$

$$\Rightarrow f_{in\_Diff} = 3\ kHz$$

$$C_{flt\_diff} = \frac{1}{2\pi \times f_{in\_diff} \times \left(R_{RTD} + 2 \times R_{flt} + 2 \times R_P\right)}$$

$$= \frac{1}{2\pi \times 3\ kHz \times (400\ \Omega + 2 \times 4.99\ k\Omega + 2 \times 590\ \Omega)} = 4.6\ nF$$

Hence, a standard value 4.7 nF is selected for C_{flt_diff}.

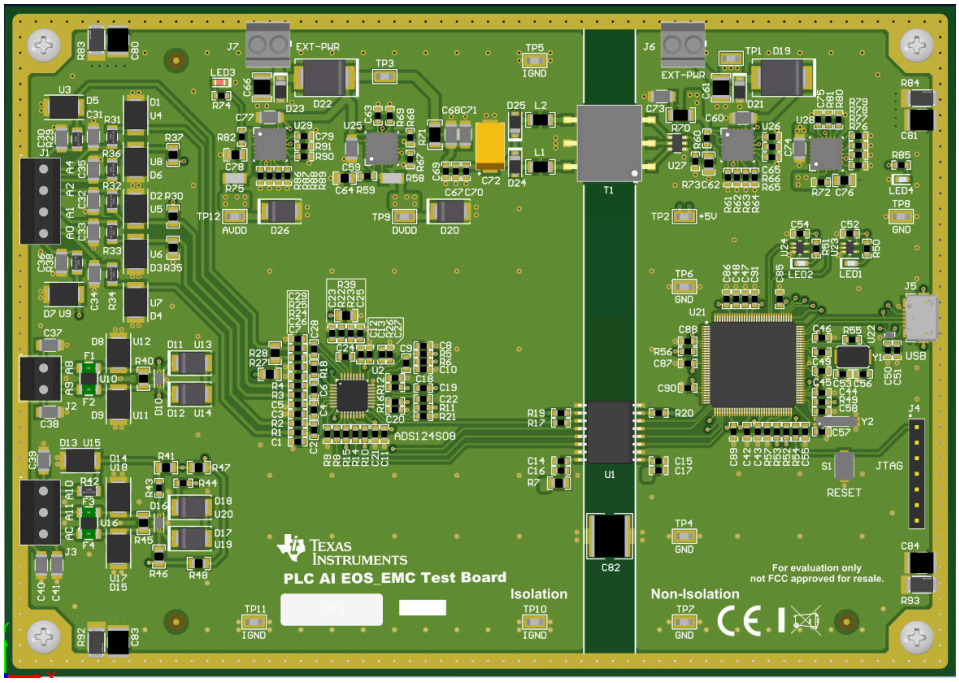
$$C_{flt} = \frac{C_{flt\_diff}}{10} = \frac{4.7\ nF}{10} = 470\ pF$$

$$C_{ref} = C_{flt} = 470\ pF$$

$$R_{flt\_ref} = R_{flt} = 4.99\ k\Omega$$

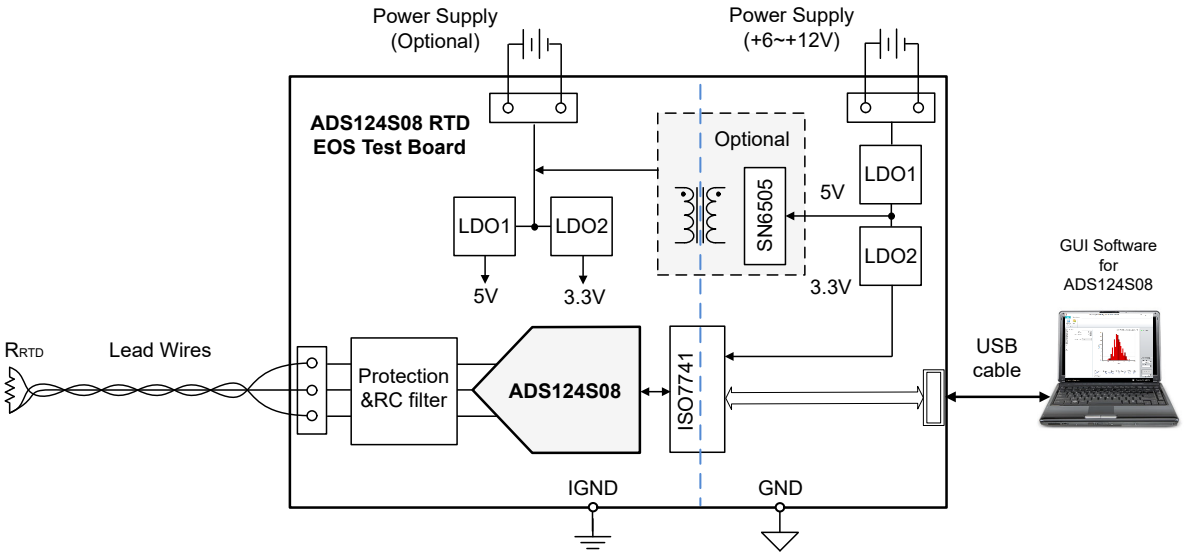
Accuracy Measured on Hardware

ADS124S08 Test Board With Input Protection Circuity shows the ADS124S08 EOS test hardware board which is designed for RTD measurement and is protected using the SMBJ14CA TVS diode from Bourns and TVS1401 bidirectional TVS diode from Texas Instruments. The isolated power supply and digital communication circuit on the test board are designed for EMC (electromagnetic compatibility) testing which are not covered in this document. The test board utilizes the onboard TM4C1294NCPDT Tiva™ Arm® Processors to communicate with the ADC via serial peripheral interface (SPI) and provide communication with a PC over a universal serial bus (USB) interface. The software including the Delta-Sigma ADC EvaluaTIon Software installer and ADS124S08 Device Package installer from the EVM tool page are used to collect conversion data from the ADC and check the performance.



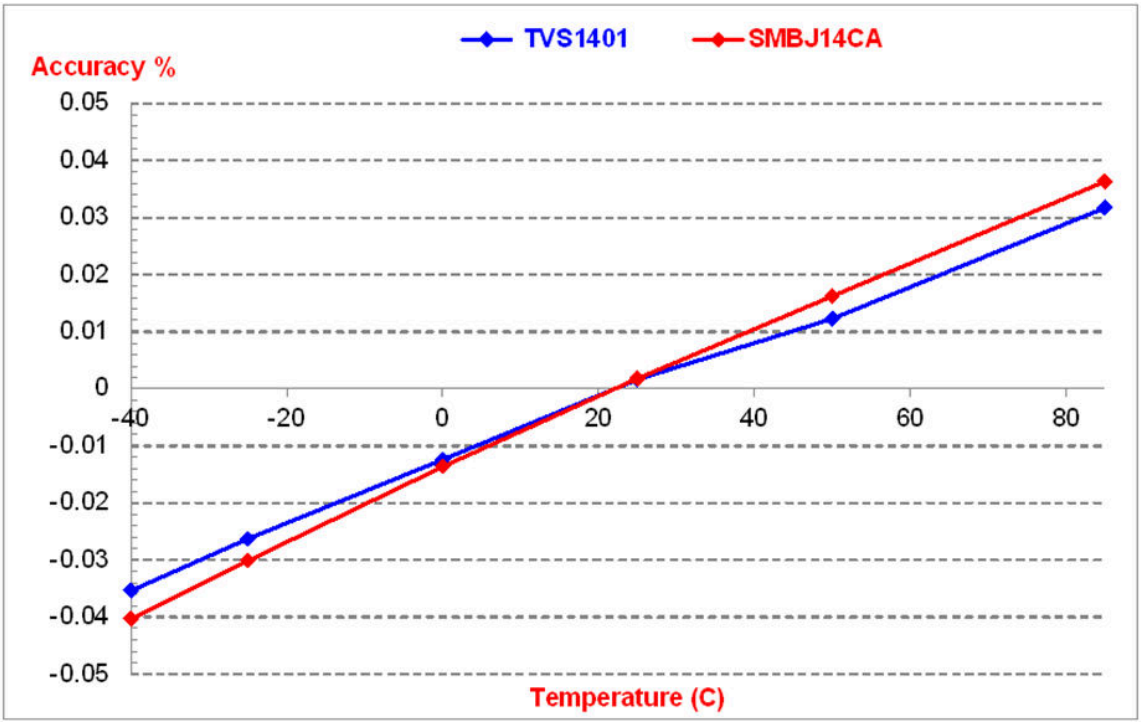
ADS124S08 Test Board With Input Protection Circuity

The following image shows the test setup for measuring accuracy and performance.

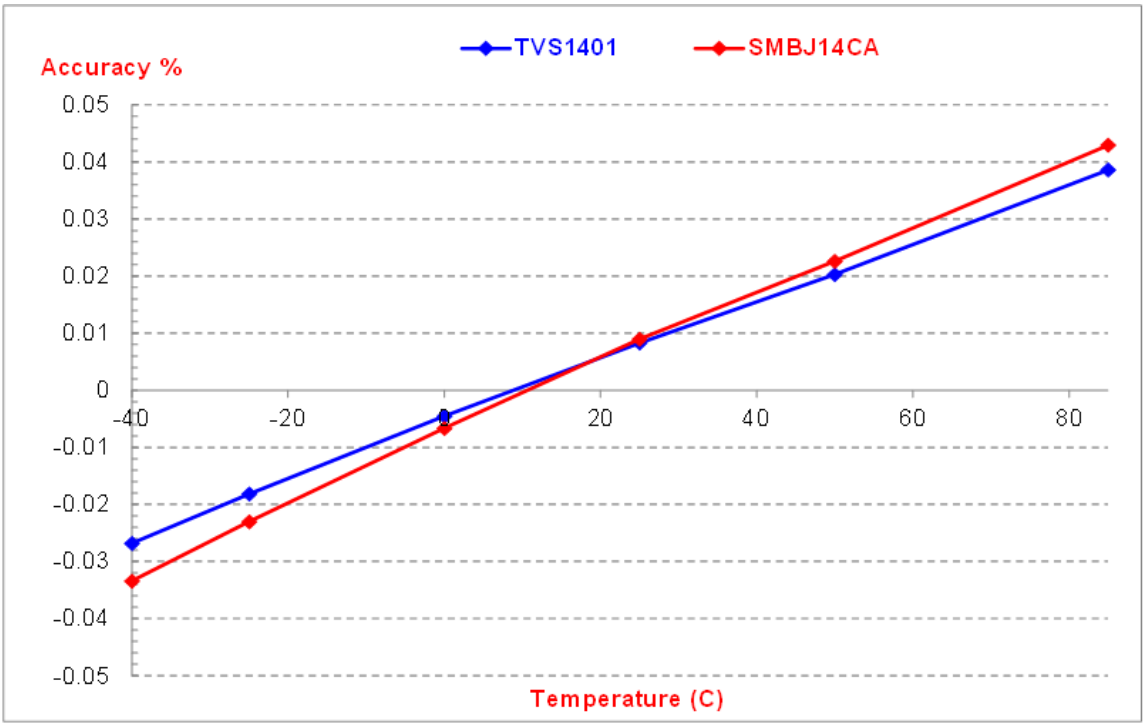


Test Setup

The next images show the measured accuracy performance for full and zero scale RTD values over ambient temperature from –40°C to +85°C. The purpose of this test is to confirm that the TVS diode leakage did not introduce a significant error across the system ambient temperature range. The test result shows the measured accuracy (< ±0.05%) with all the protection circuitry including TVS diodes and current-limiting resistors across the entire temperature range meets the expected accuracy (±0.5%).



RTD Measurement Accuracy at RTD = 100 Ω (0°C)



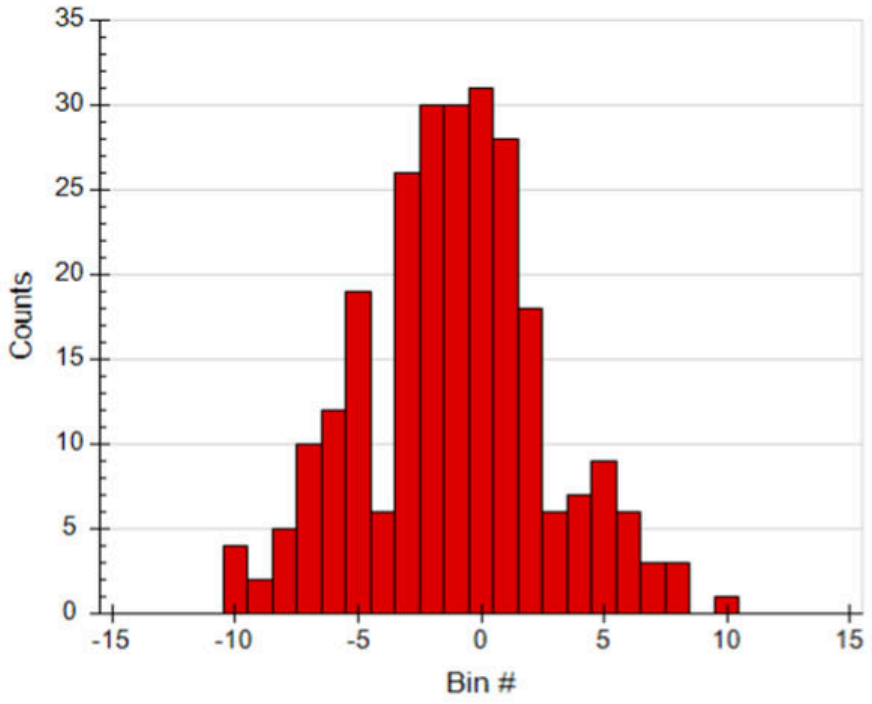
RTD Measurement Accuracy at RTD = 400 Ω (850°C)

Resolution Measured on Hardware

The next image shows the measured effective number of bits (ENOB) and noise-free resolution with bidirectional TVS diode TVS1401 from Texas Instruments. This test shows that the protection circuit has no significant impact on the ADC noise performance.

Table Title

Measured Result	ENOB (Bits)	Noise-Free Resolution (Bits)
High Temp (+85°C)	21.2	18.8
Room Temp (+25°C)	21.3	19.0
Cold Temp (–40°C)	21.5	19.1
Test Condition: low side reference, 3-wire RTD with TVS1401 protection solution.		

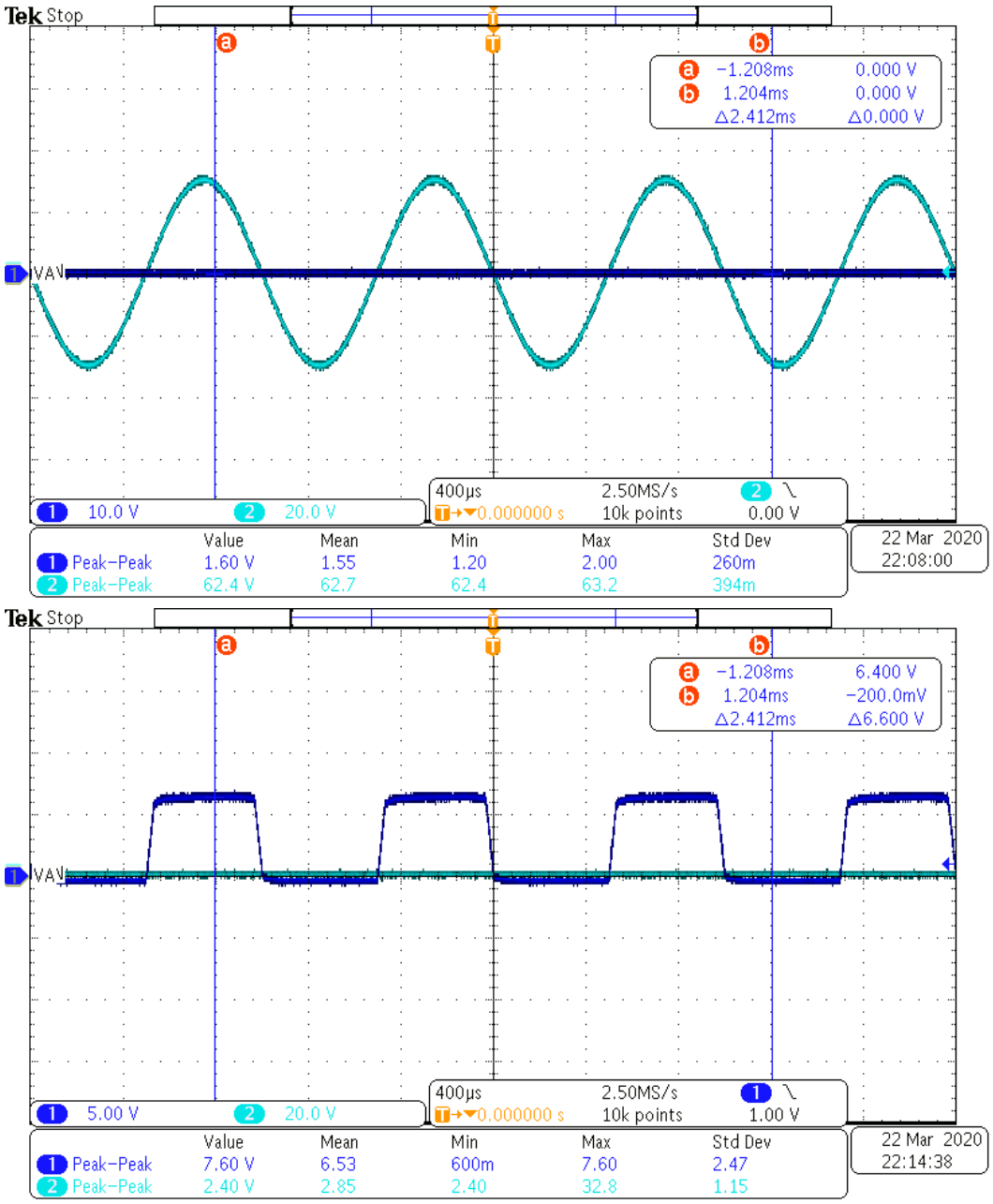


Channel	Samples	Mean	Std Dev	Pk-to-Pk	ENOB	NFB
ADC0	256	1679321.4	6.9	38	21.2	18.8

Measured Resolution for RTD = 100 Ω With TVS1401 at +85°C

ADC Input Overvoltage Condition

The circuit was tested and verified with overstress DC signals. To see how the protection circuit works, an overstress sine wave signal (±60 $V_{peak-peak}$) is applied to the input of the EOS test board. Simulated EOS Signal and Clamped Waveform on IDAC Channel Input shows the clamped waveform which was captured on the AIN5 input of the ADS124S08. The external TVS diode has been turned on and the overdriven signal has been clamped to the voltage between –200 mV and +6.4 V. Note that the clamped waveform is captured on the IDAC channel input (AIN5), so the resistance value of R_1 is limited because of the compliance voltage limit on the ADS124S08. The R_{flt} resistors on other channels of the ADS124S08 are not limited by the compliance voltage, so a large resistance value of R_{flt} is used to limit the fault current to the ADC input and the overvoltage sine wave signal is clamped to be less than +5.3 V absolute maximum input voltage on the ADS124S08. The ADC device is successfully protected from external electrical overstress signal.



Simulated EOS Signal and Clamped Waveform on IDAC Channel Input

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	Low power, low noise, 24-bit, 4-kSPS, 12-channel delta-sigma ADC with PGA and voltage reference	ADS124S08	ADCS
ADS124S06	Low power, low noise, 24-bit, 4-kSPS, 6-channel delta-sigma ADC with PGA and voltage reference	ADS124S06	ADCS
TVS1401	14-V bidirectional flat-clamp surge protection device	TVS1401	Circuit-Protection

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