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CAREFUL LAYOUT TAMES SAMPLE-HOLD PEDESTAL ERRORS

by Anthony D. Wang

In most sampling systems, the inherent characteristics of the sample-hold dictate its overall performance. However, one error source that sample-hold users do have under their direct control is the external charge injection from the digital control signal. This is known as charge transfer when measured in coulombs or as charge offset when measured in volts. It is often also known as pedestal because of its manifestation as a step change to the output. The culprit is generally the parasitic capacitance between the digital control pin and some sensitive node(s) of the circuit.

Figure 1 shows the pinout of the SHC5320 with the addition of a parasitic capacitor between pins 1 (inverting input) and 14 (the mode control pin). The inverting input is the closest pin to the digital control signal that is sensitive enough to amplify the parasitic feedthrough.

This is a typical coupling path because a convenient layout approach would be to close the feedback loop between the output and the inverting input by routing the trace underneath the device, where it could run too close to the mode control pin.

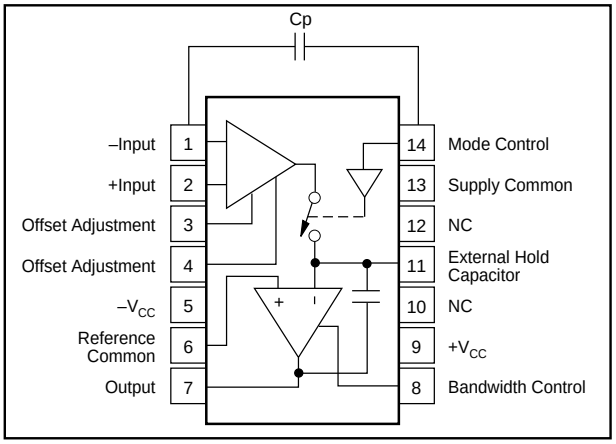

FIGURE 1. SCH5320 Pinout With Cp, Parasitic Capacitance.

Although the output of the sample-hold is considered a low impedance node, this is not true at all frequencies. The output impedance is kept low by the open-loop gain of the amplifier. As the open-loop gain falls, the output impedance rises and the amplifier is unable to swallow the high frequency component of the parasitically coupled signal.

The correct layout technique would minimize the surface area exposure between the inverting input node and the digital sample-hold control pin. Routing the feedback trace underneath the unit, as mentioned previously, would be acceptable if the line were kept to minimum width and spaced well away from the mode control line. Ideally, only one of those two traces would route beneath the package. Precautions should also be taken for two other pins that are sensitive to coupling from the digital control pin. These are pins 11 (external hold capacitor) and 8 (bandwidth control).

In case the sample-hold is configured for gain with a feedback network, position the resistors such that their junction with the inverting input occurs as close to that pin as possible. If pedestal error still results, lower the feedback network resistor values to reduce the sensitivity of this node to parasitic coupling.

A more insidious parasitic path occurs when sockets are used. Figure 2 shows the signal coupled across an empty socket. The attenuation is roughly 50dB, but can still provide enough of a signal to cause a significant pedestal error. This is suitably documented by the scope photo in Figure 3.

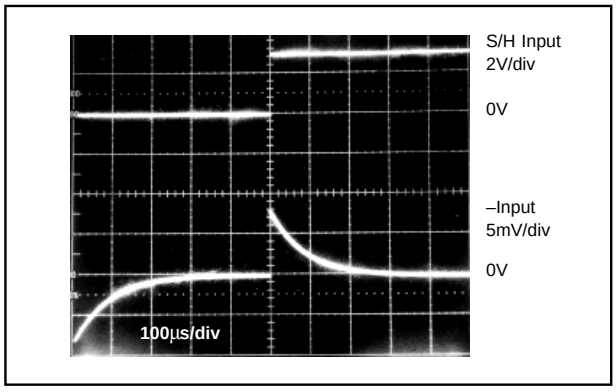

FIGURE 2. Signal Coupling from Pin 14 to Pin 1 for Empty Textool Socket.

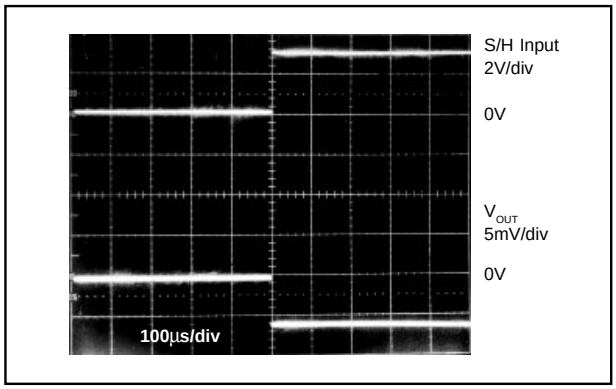

FIGURE 3. Pedestal Error Resulting from the Use of a Textool Socket.

The sample-hold was configured as a unity gain follower with its input grounded. The output trace displays a pedestal error of –6mV. Note that this is a negative excursion due to the rising edge of the digital mode control signal coupling to the inverting input of the sample-hold circuit.

The best way to avoid this is to solder the sample-hold directly into the board. If hard soldering is not a viable option, avoid the use of high profile sockets, especially the zero insertion force type. The optimum approach uses zero profile solderless sockets (such as Augut P/N 8134-HC-5P2).

The waveforms in Figure 4 confirm that a test board built with the zero profile pin connectors shows no evidence of signal coupling from the digital control pin to the inverting input. The board layout uses the technique mentioned earlier of routing a minimum width feedback trace underneath the circuit. In this example, the socket is empty and the signals are measured just as they were in Figure 2.

Figure 5 demonstrates the reward for the attention to detail covered by this discussion. The pedestal is a barely perceptible –0.5mV for the same unity gain configuration and for the same unit as illustrated in Figure 3.

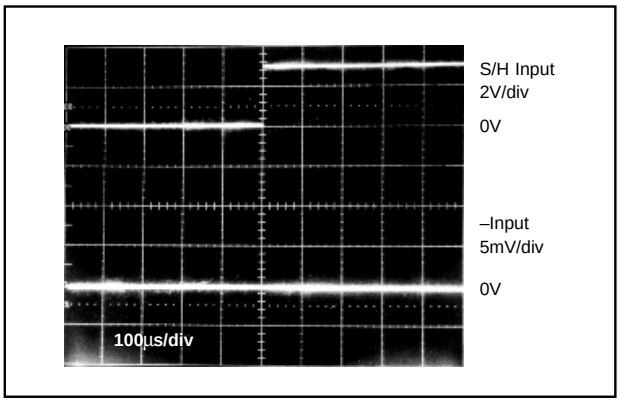

FIGURE 4. Signal Coupling from Pin 14 to Pin 1 for Empty Zero Profile Socket.

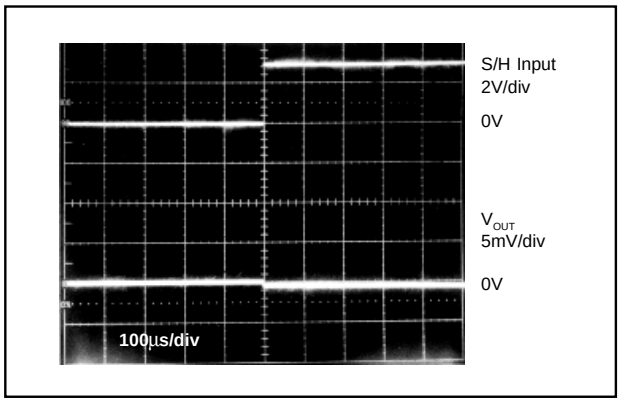

FIGURE 5. Pedestal Error Resulting from the Use of a Zero Profile Socket.

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