

# THE KEY TO UNDERSTANDING SOURCES OF ERROR IN THE ISO100 ISOLATION AMPLIFIER

A Practical Guide to Optimizing Accuracy

While most applications of the IS0100 do not require error correction, being aware of the adjustment options can be beneficial. Provisions for several types of error correction are included to allow the circuit designer to obtain maximum accuracy in a specific application. Adjustments can be made to null errors that are internal to the isolation amplifier, or in other parts of the system.

This application bulletin describes how to quantify the effects of these potential errors, and to help identify the most appropriate means of correction. Each figure has a caption that gives a summary of the important ideas. Subjects to be covered include:

- · Theory of operation
- Definition of terms
- Offset current (I<sub>OS</sub>)
- Gain error  $(A_E)$
- Offset voltage (V<sub>os</sub>)

#### **THE IS0100**

The ISO100 has several modes of operation: unipolar or bipolar, voltage or current input, and inverting or noninverting. The product data sheet for the ISO100 includes sections detailing both the error model and the theory of operation. Study of the data sheet is suggested. A simplified block diagram of the ISO100 is shown in Figure 1.

Signal transmission (across the isolation barrier) is accomplished through an optical coupler, which acts as a 1:1 current translator. Current at the input of the device is replicated on the output side of the coupler. The isolated output current ( $I_{OUT}$ ) is forced to flow through  $R_F$  by the summing node action of the output op amp.

At first glance it might seem unusual that the noninverting input of the ISO100 is connected to the inverting input of the input op amp. However, this is due to two inversions in the



FIGURE 1. Simplified ISO100 Block Diagram. The ISO100 can be thought of as a 1:1 current transistor with its output flowing into a current-to-voltage converter. This isolation amplifier is inherently a current input device. However, since the input is a virtual ground, an input voltage can be converted to a current by simply including  $R_{IN}$ . The optional  $I_{REF}$  connections are used to produce bipolar operation.

signal path from isolation input to output. Care should be taken not to be confused on this point.

The resulting simplified transfer function for the IS0100 is given by:

$$V_{OUT}/I_{IN} = (R_F) (1 + A_E)$$

Gain error  $(A_E)$  is defined as the deviation of the ratio,  $I_{IN}/I_{OUT}$  from unity. It can be thought of as the "coupling error."

The optical coupler uses a matched pair of photodiodes and a light emitting diode (LED) to produce signal transmission. Since an LED only works when current flows in one direction, the basic mode of operation is unipolar. In the unipolar mode, only negative input currents are allowed (i.e., only currents out of the input produce a positive voltage to turn the LED on). Bipolar operation can be easily produced by internally offsetting the input from zero. Two matched current sources ( $I_{REF1}$  and  $I_{REF2}$ ) are included in the IS0100 for this purpose. By connecting current source,  $I_{REF1}$ , on the input side of the coupler, the amplifier is made to operate at half-scale (when the input current is zero). Connecting an equal source, (I<sub>REF2</sub>) on the output side, shifts the output voltage back to zero. This arrangement maintains a desirable "zero-in/zero-out" relationship, while allowing input currents of either polarity to be accepted.

#### THE ERROR MODEL

The model used to represent IS0100 errors is shown in Figure 2. Offset current ( $I_{OS}$ ) is defined as the input current required to make the output voltage zero. In the unipolar mode, it is mainly composed of mismatches in the optical paths.  $I_{REF1}$  and  $I_{REF2}$  are the current sources that are optionally connected to produce bipolar operation. The major source of bipolar  $I_{OS}$  is the mismatch in  $I_{REF1}$  and  $I_{REF2}$ . The various contributions to the offset current are grouped together and are modeled as a single current source at the

input. Keep in mind that  $I_{OS}$  has a sensitivity to temperature, supply voltage, common mode voltage and iso mode voltage. However, it would be very rare that all of these factors would be significant. Analysis examples for these terms are found in the data sheet. It will be shown that gain error also introduces an offset current term. Voltage offsets ( $V_{OS}$ ) are modeled as voltage sources at the inputs of each op amp.  $I_{D1}$  and  $I_{D2}$  represent the currents being generated by the photodiodes. The currents are related by the equation:

$$I_{D2} = I_{D1} (1 + A_E).$$

These are internal currents which mathematically cancel in presenting the total transfer equation. The gain error  $(A_{\rm E})$ and the unipolar offset current (Ios) cannot be directly altered. However, these terms can be considered constant for each amplifier, allowing their effects to be compensated by simple external means. For instance, the gain error is compensated by adjusting either  $R_F$  or  $R_IN$ . Voltage offset can be trimmed as in most other op amps, using the trim pins provided. Offset current is trimmed by adjusting the magnitude of one of the reference currents (I<sub>REF1</sub>, I<sub>REF2</sub>). Because of the on-chip design, sampling or adjusting of the internal references does not have a detrimental effect on the isolation amplifier's performance. Ios trim with an external input current is possible, but careful consideration should be given to the effects of temperature and supply voltage variations. Noise can also be an important error source. While not treated in this application note, information can be found in the product data sheet.

#### WHAT IS THE OUTPUT?

It is important to be able to calculate total worst case errors for a particular circuit configuration. Clearly, this is important for establishing incoming inspection criteria as well as circuit and system design.



FIGURE 2. DC Error Model.  $V_{OSI}$  and  $V_{OSO}$  model the respective input offset voltages. There are several possible contributors to offset current. The composite effect is modeled with one current source,  $I_{OS}$ , at the input. The gain error  $(A_E)$ defines the relationship between  $I_{D1}$  and  $I_{D2}$  ( $I_{D2} = I_{D1} [1 + A_E]$ ). While shown as separate sources, any mismatch in  $I_{REF1}$  and  $I_{REF2}$  are included in the  $I_{OS}$  term.

Equation 2 in the IS0100 data sheet allows the user to solve for the output voltage under any conditions. This transfer equation (for the voltage mode) is repeated here:

$$\begin{split} \mathbf{V}_{\mathrm{O}} &= \mathbf{R}_{\mathrm{F}}\left[(\mathbf{V}_{\mathrm{IN}}/\mathbf{R}_{\mathrm{IN}} + \mathbf{V}_{\mathrm{OSI}}/\mathbf{R}_{\mathrm{IN}} - \mathbf{I}_{\mathrm{REF1}} + \mathbf{I}_{\mathrm{OS}})(1 + \mathbf{A}_{\mathrm{E}}) + \mathbf{I}_{\mathrm{REF2}}\right] + \mathbf{V}_{\mathrm{OSO}} \end{split}$$

The transfer equation for an input current is:

$$V_{O} = R_{F} \left[ \left( I_{IN} - I_{REF1} + I_{OS} \right) \left( 1 + A_{E} \right) + I_{REF2} \right] + V_{OSC}$$

By substituting worst case numbers for all the error terms, the maximum error in the value of  $V_0$  can be determined as shown in Example 1.

**Example 1:** An ISO100CP is to be tested at incoming inspection. The part is to be tested in a bipolar unity gain configuration. For the conditions of  $R_F = R_{IN} = 1M$  and  $V_{IN} = 0$ , what output voltage would be within the specification limits?

The maximum values for the error terms are found in the data sheet. Inserting them into the output equation presented above:

$$V_{ERR} = 1M [\pm 200\mu V / 1M - 12.5\mu A \pm 35nA)$$
$$(1\pm 0.02) + 12.5\mu A] \pm 200\mu V$$
$$V_{ERR} = \pm 286mV (maximum)$$

 $\pm 286$  mV would then be the range of permissible output voltage in this configuration.

A significant portion of the output error in the bipolar mode is due to the gain error. With no input,

$$V_{O} \cong R_{F} [I_{OS} - I_{REF1}(A_{E})]$$

The term that dominates is the reference current times the gain error. This error appears as an offset, and must be accounted for if the output is being measured to obtain the actual  $I_{os}$ . Otherwise, the user may wonder why an additional error is present in the output voltage measurement. The next example shows that this is not true for the unipolar mode of operation.

**Example 2:** Consider a unipolar, non-inverting, gain of one amplifier, as shown in Figure 3A. The output equation can be rewritten for the unipolar case as shown:

$$V_{O} = R_{F} [(V_{IN} / R_{IN} + V_{OSI} / R_{IN} - I_{OS})(1 + A_{E})] + V_{OSO}$$

Error analysis proceeds as follows: unipolar operation is not defined at zero input current because the LED could be turned off, disabling the amplifier's internal feedback loop.  $V_{IN}$  will be set to the minimum allowed value. The remaining errors are as specified in the data sheet. Note that the  $V_{IN}$  (MIN) specification of 20mV follows from the 20nA minimum input current specification for linear operation.

$$V_{O} = 1M \left[ (-20 \text{mV} / 1\text{M} \pm 200 \mu\text{V} / 1\text{M} \pm 10 \text{nA}) \right]$$
$$(1 \pm 0.02) \pm 200 \mu\text{V}$$

 $V_{\Omega} = -31 \text{mV}$  (worst case, all errors negative)

Therefore,  $V_{ERROR} = V_O - V_{IN} = \pm 11 \text{mV}$ .



FIGURE 3. Standard Configurations. Most applications of the ISO100 will make use of these configurations, with slight variations. (A) shows the configuration for unipolar operation, which functions for negative inputs only. (B) shows how to use the internal references to provide bipolar operation. The circuits show all necessary connections and indicate the package pin numbers. Note that power supply connections ( $V_p$  and  $V_N$ ) to the input and output and output stages must be "isolated."

#### **CORRECTING THE ERRORS**

The next logical step after calculating the errors is to reduce them. In the following discussion, each error is considered by itself. The suggested methods of trimming or adjusting errors are considered, and some general hints are presented.

#### **OFFSET CURRENT ERRORS**

Because the ISO100 is a current input device, the dominant error in most configurations will be the input offset current ( $I_{os}$ ). As stated above,  $I_{os}$  is defined as the current, injected at the input, necessary to force the output to zero. In the unipolar mode, this definition has a limitation which must be understood. Zero output requires that  $I_{D2}$  be zero, implying that the optical feedback path is open. This condition is unsatisfactory for predictable performance. Therefore, a



FIGURE 4.  $I_{os}$  Adjustment from the Input Side. If  $I_{os}$  were negative, the ideal transfer curve would be shifted to the left, as shown above. This would cause a positive output voltage when there was no input current. Connecting a negative correction current,  $I_{c}$ , to the summing node of the first op amp causes the transfer curve to shift to the right. Thus, the effect of  $I_{os}$  can be trimmed out.

minimum input current must be maintained to assure that the amplifier is operating in its linear region. The transfer function is only defined when the net current at the input node flows out of that node. The unipolar  $I_{OS}$  term is extrapolated from this minimum practical current.

In the bipolar mode, no such limitation exists. In this mode the internal references keep the LED and photodiodes running at half-scale when the input is zero.  $I_{os}$  can therefore be measured directly.

### **I**os ADJUSTMENTS

As suggested above, the internal references can be used to generate a compensation current to cancel  $I_{os}$ . In Figure 4 a current divider is used to divert a small portion of the input stage reference current to the input node. Note that the



FIGURE 5.  $I_{OS}$  Adjustment from the Output Side. Connecting a negative correction current ( $I_C$ ) to the summing node of the output amplifier causes the transfer curve to shift upward by the amount of  $I_C$ . This causes the output to shift back toward zero. Again, a current divider is used to derive the correction current from the internal references. By combining the methods of Figures 4 and 5, a correction current can be generated that will cancel either polarity of  $I_{OS}$ .

direction of the current is negative. This additional current flowing out of the summing node behaves like any input signal, and thus causes more current to flow in  $R_F$ . The change in  $V_O$  is  $-I_C$  ( $R_F$ ), where  $I_C$  is the new (offset correcting) current. The graph of the transfer function shows how the curve is shifted by this adjustment.

Since the reference current is of fixed polarity, the curve can only be shifted in one direction with the above connection. However, the curve can be shifted the other way by making use of the output reference ( $_{REF2}$ ). Figure 5 shows the effect of tapping a small current from this source and applying it to the input of the second stage. The nominal value of  $I_{REF}$  is l2.5 to 13µA.



FIGURE 6. Using the Unipolar Amplifier at Zero Input. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with  $R_5$  and  $R_6$ the minimum current required to keep the input stage in the linear region of operation can be established.  $R_7$  and  $R_8$  are adjusted to cancel the offset created in the input stage. This brings the output to zero when the input is zero. While the amplifier can now operate down to zero input votlage, it only has a small portion of the current drain and noise that the true bipolar configuration would have.

By using a combination of these two methods it is possible to always move the transfer curve to the ideal position. In Figure 6, the network in the input stage offsets the system in a known direction. The variable divider network in the output stage has enough range to move the output voltage through zero. It is worth repeating that the correction currents could be generated with resistive dividers connected to the power supplies, but using the internal references takes advantage of their inherent stability, accuracy, and power supply rejection.

**Example 3:** A common use of the circuit in Figure 6 might be to provide a "keep alive" current for the ISO100. This might be required in a unipolar application where it is possible for the input to go to zero. While it would be a little simpler to use the bipolar configuration, this would result in higher noise and increased quiescent current.

The circuit uses a fixed current divider in the input stage to ensure the direction of  $I_{os}$ . A variable divider in the output stage allows the user to adjust the amplifier to be just "slightly bipolar." Enough current (20 to 30nA minimum) must be drawn from the input to fulfill the minimum unipolar requirement. Since only a small portion of the reference current is being used, a minimal increase in the noise will result.

A suggested value of  $I_{C1}$  is about 100nA (1%  $I_{REF}$ ). Solving the resistive current divider network yields:

$$R_5 / R_6 \cong I_{REF} / I_{C1} = 120.$$

Practical resistor values would be:  $R_5 = 10M$ ,  $R_6 = 84k\Omega$ . The adjustment range of  $I_{C2}$  should include  $I_{C1}$  and the built-in error sources (100nA + 20nA = 120nA). This yields:  $R_7 = 10M$ ,  $R_8 = 200k\Omega$ .

### GAIN ERROR ADJUSTMENTS

Gain error in the ISO100 is due mainly to mismatches in the optical cavity. These mismatches show up as an error in the ratio of the two photodiode currents ( $I_{D1}$  and  $I_{D2}$ ).

As shown in Figure 7, a gain error will cause the transfer function curve to rotate about the quiescent operating point of the photodiodes. The output stage functions as a current-to-voltage converter with a transconductance (gm) =  $1/R_{\rm F}$ . Thus, changing  $R_{\rm F}$  will also cause the line to rotate about the Q point. Therefore, in the unipolar mode,  $A_{\rm E}$  is simply corrected by adjusting  $R_{\rm F}$ .

In the bipolar mode, gain adjustment is not quite so simple. Gain error will still cause the line to rotate about the photodiode Q point, but that point is no longer near the origin. Figure 8 shows that changing either  $R_F$  or  $R_{IN}$  will cause the transfer curve to rotate about the point where the input current is zero (as it does in the unipolar case). However, if the ratio  $R_F/R_{IN}$  is changed to make up for  $A_E$ , an  $I_{OS}$  term is introduced. This "Apparent  $I_{OS}$ " term is due to the fact that  $I_{REF2}$  will get divided by the gain error, but  $I_{REF}$ 

will not. The difference in reference currents, as seen at the input, will be the apparent offset error (see Figure 9). This effect makes the trimming of gain error a two step process for bipolar applications. First, either resistor is adjusted to correct the slope of the line, then the  $I_{os}$  is trimmed using the methods discussed earlier.

## **V**os ADJUSTMENTS

While both the input and output amplifiers of the IS0100 have provisions for adjusting offset voltage, it is generally not necessary to do so because the contribution to total error is small. Only  $V_{\rm OSI}$  has practical significance (in most applications), and then only when  $R_{\rm IN}$  is small. In most cases the output amplifier is configured so that it has a voltage

gain of one, and as such its  $V_{OS}$  contribution will be insignificant. The output adjustment range via the  $V_{OSO}$  control will be only a few millivolts.

The input offset voltage (V<sub>OSI</sub>) will affect the output only through its interaction with R<sub>IN</sub>. V<sub>OSI</sub> causes a current error equal to V<sub>OSI</sub>/R<sub>IN</sub> which is then scaled by R<sub>F</sub>. The output voltage is V<sub>O</sub> = V<sub>OSI</sub>(R<sub>F</sub>/R<sub>IN</sub>). To adjust V<sub>OSI</sub> see Figure 10. If R<sub>IN</sub> is a high value (because the amplifier is in a low gain or has a current source input) the output contribution of V<sub>OSI</sub> will be minimal. Even in a high gain, where V<sub>OSI</sub> has a larger effect on the output, the signal/offset ratio is constant.

If the system offset must be adjusted from the output side of the ISO100, the output amplifier can be placed in a gain configuration. As shown in Figure 11, the output voltage



FIGURE 7. Effect of Gain Error  $(A_E)$ .  $A_E$  will cause an error in the slope of the transfer function, rotating the line about a point determined by the quiescent current in  $D_1$  and  $D_2$ . Unipolar, this point is near the origin. In the bipolar mode, the internal references cause this point to shift to the right and up as shown above. In either case, the change in slope is the same.



FIGURE 8. Adjusting the Gain. Changing the ratio  $R_{F}R_{IN}$  will change the gain by rotating the transfer function about the point where  $I_{IN} = 0$ . This will be true for both the unipolar and bipolar cases.  $I_{SO}$  is zero in these examples.

offset ( $V_{OSO}$ ) is now multiplied by a gain of  $1 + (R_F/R_9)$ . If  $R_F = 1M$ , and  $R_9 = 1k\Omega$ , the output will be 1001 times  $V_{OSO}$ . This connection does not alter the input signal gain, but it does amplify all output stage errors including  $V_{OSO}$  and noise. It is also important to realize that adjusting offset voltage in the IS0100 (and most op amps) causes a change in the offset voltage drift of about  $3\mu V/^{\circ}C$  for each millivolt introduced. Offset drift will be amplified by the same gain factors (as the  $V_{OSI}$ ) above.

**Example 4—see Figure 12.** Using the methods described previously, the output errors of an ISO100 can be adjusted to zero. In this example, an ISO100BP is in the standard bipolar configuration with a gain of 100. Let  $R_F = 1M$ . From the data sheet, the maximum errors are:  $A_E = 2\%$ ,  $I_{os} = 70$ nA,  $V_{os} = 300\mu$ V.

 $I_{\rm OS}$  correction uses a variation of previous techniques. The adjustment not only trims the 70nA of  $I_{\rm OS}$ , but also the apparent  $I_{\rm OS}$  caused by the gain error. This additional current could be as large as 250nA  $[A_{\rm E}(I_{\rm REF}1)=0.02~(12\mu A)]$ . The total trim range should then be 70nA +250nA = 320nA. Because the input of the second amplifier is a virtual ground,  $R_{12}$  has the same voltage across it as  $R_{13}$ .  $R_{12}$  is then:

$$\begin{split} R_{12} &= [(R_{13}) \; (I_C) \div (I_{REF} - I_C)] \\ &= 10 M \Omega \; (320 n A) \div (10.5 \mu A - 320 n A) \\ &= 316 k \Omega \end{split}$$

The 10.5 $\mu$ A is the minimum I<sub>REF</sub> specification on the data sheet. Conservative design allows the R<sub>10</sub> divider to produce twice the compensation current of the R<sub>12</sub> divider. Therefore,

 $R_{10}$  must be twice  $R_{12}$ . The calculated value of  $R_{10}$  is  $632k\Omega$ , so a standard 1M pot is selected.

## SUMMARY OF CORRECTION TECHNIQUES—SEE FIGURE 12

To trim  $I_{os}$ , disconnect the input source and let it float. This minimizes voltage offset effects.  $R_{10}$  is then adjusted to bring the output to zero.

The gain error can be compensated by adjusting either  $R_F$  or  $R_{IN}$ . In most circuits it will not matter which is trimmed. In this case  $R_{IN}$  will be adjusted via  $R_G$ . Allowing for a 2% gain error,  $R_{IN}$  should be 2% low with  $R_G$  providing a 4% trim range. This makes  $R_{IN} = 9.8k\Omega$  with 400 $\Omega$  of trim. Using standard values,  $R_G$  would be a 500 $\Omega$  pot and the fixed resistor will be 9.76k $\Omega$ . The gain is corrected by making a known change in the input voltage, and by adjusting  $R_G$  for the correct change at the output. Remember that in the bipolar mode there is an interaction between the adjustment of  $A_E$  and  $I_{OS}$ . Repeat these adjustments until the desired accuracy is obtained.

The last step is to adjust  $V_{OS}$ . Because the output stage is in a gain of one,  $V_{OSO}$  can be ignored.  $V_{OSI}$ , on the other hand, is multiplied by 101 and should be trimmed.  $R_{14}$  is adjusted so that there is no shift in the output when the input side of  $R_{IN}$  is switched between floating and ground. Any shift is due to the offset voltage causing a current to flow in  $R_{IN}$ , which is then gained up to the output .

All errors should now be minimized.



 $\label{eq:FIGURE 9. Offset Introduced by Gain Error (Bipolar Only). \\ The gain error (A_E) will cause an apparent I_{OS} \\ term to appear when in the bipolar mode. A_E \\ causes the ideal transfer line A to rotate to \\ position B. Adjusting R_F or R_{IN} can correct the \\ slope, as suggested by line C. The line will rotate \\ about the point where I_{IB} = 0. The result is a line \\ with the correct slope, but having an offset equal \\ to I_{REF1} (A_E). This offset term can be adjusted out \\ in the same way as regular I_{OS}. \\ \end{array}$ 



FIGURE 10. Preferred Method for Voltage Offset Trim. In those rare applications where offset voltage is significant, it is best to adjust the input offset voltage,  $V_{OSI}$ , as shown above.  $V_{OSI}$  and its drift appear at the output multiplied by the factor  $R_F/R_{IN}$ .  $V_{OSO}$  will usually not be gained up, and thus will not need adjustment. Adjust  $V_{OSI}$  until opening up and closing  $S_x$  causes no shift in the output voltage.

## **TEST CIRCUIT**

A circuit is shown in Figure 13 that will allow all the major errors of the ISOI00 to be measured.



FIGURE 11. Alternate Method for Offset Voltage Trim. If the offset voltage has to be adjusted on the output side of the isolation barrier, the output amplifier can be put in an offset multiplying gain.  $V_{0SO}$ , drift of  $V_{0SO}$ , and output stage noise appear at the output, multiplied by  $(R_F/R_9) + 1$ . However, the signal is unaffected. Signal-to-noise ratio could be adversely affected.



FIGURE 12. Adjusting the Bipolar Errors (Example 4). Each of the errors are adjusted in turn. With  $V_{IN}$  = "open,"  $I_{OS}$  is trimmed by adjusting  $R_{10}$  to make the output zero.  $R_G$  is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting  $R_{14}$ .



FIGURE 13. Standard Test Configuration. Each of the major errors in the ISO100 can be measured with the circuit shown. The test circuitry is similar in concept to the methods used in the actual production test equipment. To make measurements, the switches are placed in the positions indicated in the table, and the input voltage is set accordingly. The voltage or current reading is then used to compute the error.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

#### **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated