Analog Engineer's Circuit Amplifiers

Inverting Amplifier Circuit

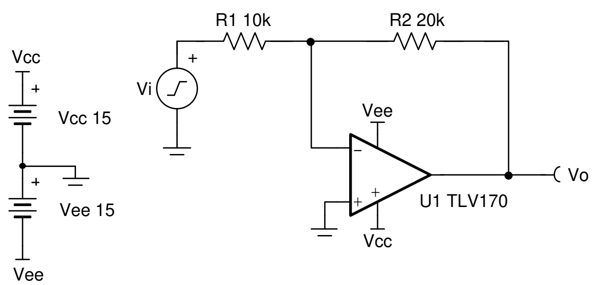
TEXAS INSTRUMENTS

Design Goals

Input		Output		Freq.	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
–7V	7V	–14V	14V	3kHz	15V	–15V

Design Description

This design inverts the input signal, V_i, and applies a signal gain of –2V/V. The input signal typically comes from a low-impedance source because the input impedance of this circuit is determined by the input resistor, R_1. The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



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Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the source output impedance.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_2. Adding a capacitor in parallel with R_2 improves stability of the circuit if high value resistors are used.
6. Large signal performance can be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the Design References section.

Design Steps

The transfer function of this circuit follows:

$$V_o = V_i \times \left(-\frac{R_2}{R_1}\right)$$

1. Determine the starting value of R_1. The relative size of R_1 to the signal source impedance affects the gain error. Assuming the impedance from the signal source is low (for example, 100Ω), set R_1 = 10kΩ for 1% gain error.

   $$R_1 = 10\ \mathrm{k\Omega}$$

2. Calculate the gain required for the circuit. Since this is an inverting amplifier, use V_{iMin} and V_{oMax} for the calculation.

   $$G = \frac{V_{oMax}}{V_{iMin}} = \frac{14\ \mathrm{V}}{-7\ \mathrm{V}} = -2\frac{\mathrm{V}}{\mathrm{V}}$$

3. Calculate R_2 for a desired signal gain of –2 V/V.

   $$G = -\frac{R_2}{R_1} \rightarrow R_2 = -G \times R_1 = -\left(-2\frac{\mathrm{V}}{\mathrm{V}}\right) \times 10\ \mathrm{k\Omega} = 20\ \mathrm{k\Omega}$$

4. Calculate the small signal circuit bandwidth to ensure it meets the 3-kHz requirement. Be sure to use the noise gain, or non-inverting gain, of the circuit.

   $$GBP_{TLV\ 170} = 1.2\ \mathrm{MHz}$$

   $$NG = \left(1 + \frac{R_2}{R_1}\right) = 3\frac{\mathrm{V}}{\mathrm{V}}$$

   $$BW = \frac{GBP}{NG} = \frac{1.2\ \mathrm{MHz}}{3\ \mathrm{V/V}} = 400\ \mathrm{kHz}$$

5. Calculate the minimum slew rate required to minimize slew-induced distortion.

   $$V_p = \frac{SR}{2 \times \pi \times f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

   $$SR > 2 \times \pi \times 3\ \mathrm{kHz} \times 14\ \mathrm{V} = 263.89\frac{\mathrm{kV}}{\mathrm{s}} = 0.26\frac{\mathrm{V}}{\mathrm{\mu s}}$$

   - SR_{TLV170} = 0.4V/µs, therefore, it meets this requirement.

6. To avoid stability issues, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

   $$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_2 \parallel R_1)} > \frac{GBP}{NG}$$

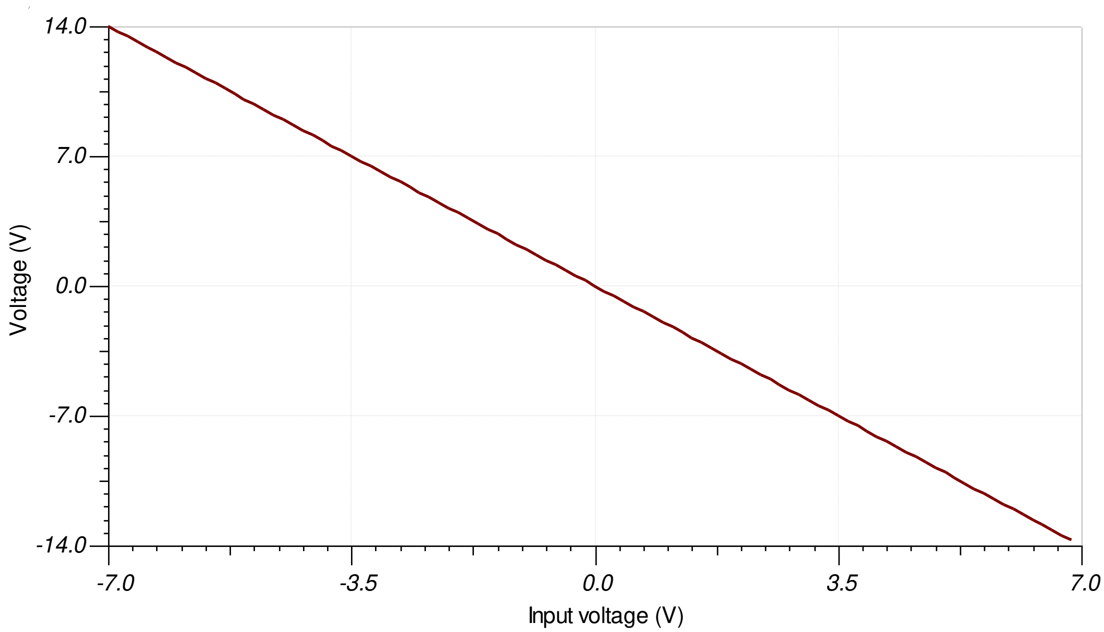
   $$\frac{1}{2 \times \pi \times (3\ \mathrm{pF} + 3\ \mathrm{pF}) \times \frac{20\ \mathrm{k\Omega} \times 10\ \mathrm{k\Omega}}{20\ \mathrm{k\Omega} + 10\ \mathrm{k\Omega}}} > \frac{1.2\ \mathrm{MHz}}{3\ \mathrm{V/V}}$$

   $$3.97\ \mathrm{MHz} > 400\ \mathrm{kHz}$$

- C_{cm} and C_{diff} are the common-mode and differential input capacitance of the TLV170, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

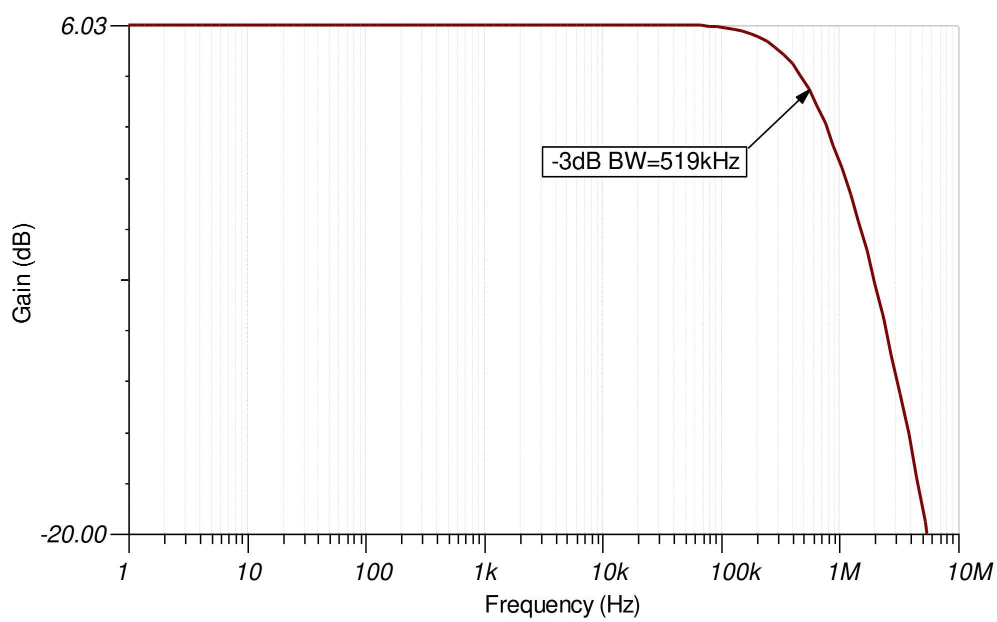
Design Simulations

DC Simulation Results



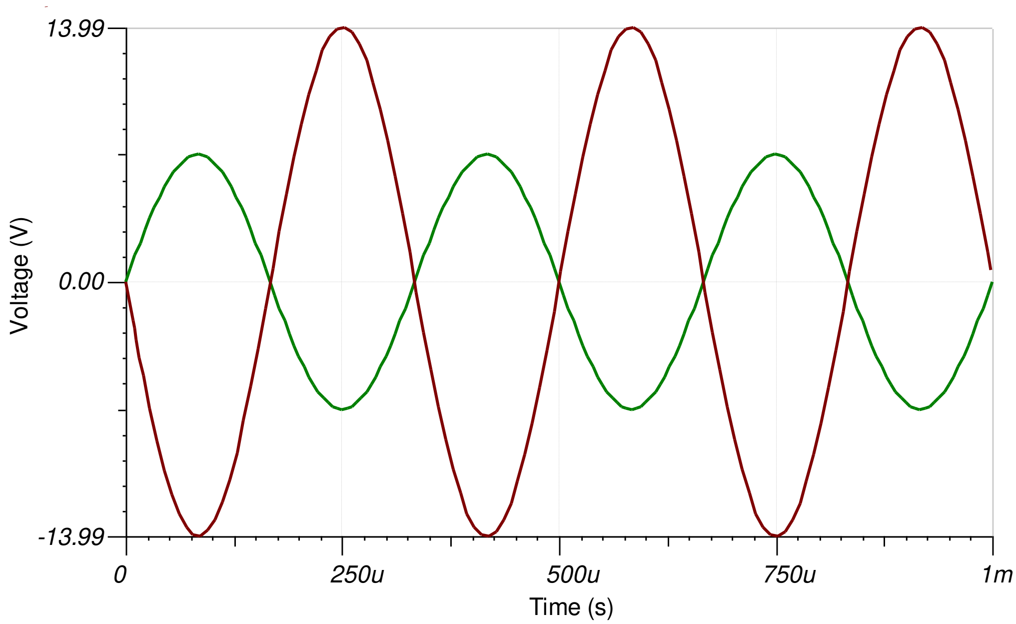
AC Simulation Results

The bandwidth of the circuit depends on the noise gain, which is 3V/V. The bandwidth is determined by looking at the –3-dB point, which is located at 3dB given a signal gain of 6dB. The simulation sufficiently correlates with the calculated value of 400kHz.



Transient Simulation Results

The output is double the magnitude of the input and inverted.



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC492
3. TI Precision Labs

Design Featured Op Amp

TLV170	
V_{ss}	±18 V (36 V)
V_{inCM}	(Vee-0.1 V) to (Vcc-2 V)
V_{out}	Rail-to-rail
V_{os}	0.5 mV
I_q	125 µA
I_b	10 pA
UGBW	1.2 MHz
SR	0.4 V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv170	

Design Alternate Op Amp

LMV358A	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	(V_{ee}–0.1 V) to (V_{cc}–1 V)
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	70 µA
I_b	10 pA
UGBW	1 MHz
SR	1.7 V/µs
#Channels	1 (LMV321A), 2 (LMV358A), 4 (LMV324A)
www.ti.com/product/lmv358A	

Revision History

Revision	Date	Change
C	December 2020	Updated result for Design Step 6.
B	March 2019	Changed LMV358 to LMV358A in the Design Alternate Op Amp section.
A	January 2019	Downstyle title. Added link to circuit cookbook landing page.