Core Voltage Accumulation

ABSTRACT

This document provides a description of the issue referred to as "V_{CORE} Accumulation", which impacts versions of the MSP430F543xA, MSP430F55xx, MSP430F550x, and CC430F61xx devices and their derivatives. This document also provides guidance in assessing whether the issue may affect a given application and to what extent.

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1 Overview

Under specific conditions, the core voltage of the device, V_{CORE}, may rise incrementally until it is beyond 2.0 V, which is the maximum allowable limit for digital circuitry internal to the MSP430. This increase may remain undetected in an application with no functional impact but could potentially result in decreased endurance and increased wear over the lifetime of the device, because the digital circuitry is continually subjected to overvoltage.

The root cause of V_{CORE} accumulation is understood and the implementation of the fix is already in progress. Device revisions incorporating this fix are currently being processed.

However, for released devices that are affected by this issue, this document provides details on the issue and helps the user assess the potential impact. The document also addresses the means by which the issue can be avoided by making changes to the application flow.

2 Affected Devices

The list of affected devices in the MSP430F543xA, MSP430F550x, MSP430F55xx, and CC430F61xx are shown in Table 1.

Table 1. Affected Devices

Family	Device Derivatives	Lot Trace Code
MSP430F543xA	F5438A	< 18xxxxx
	F5437A	
	F5435A	
	F5418A	
	F5419A	
	BT5190	
MSP430F550x	F5500	< 19xxxxx
	F5501	
	F5502	
	F5503	
	F5504	
	F5505	
	F5506	
	F5507	
	F5508	
	F5509	
	F5510	
MSP430F55xx	F5513	< 16xxxxx
	F5514	
	F5515	
	F5517	
	F5519	
	F5521	
	F5522	
	F5524	
	F5525	
	F5526	
	F5527	
	F5528	
	F5529	

Table 1. Affected Devices (continued)

Family	Device Derivatives	Lot Trace Code
CC430F61xx	F5133	Affected revisions are shown in errata document
	F5135	
	F5137	
	F6125	
	F6126	
	F6127	
	F6135	
	F6137	

3 Problem Description

The core voltage can rise up to the voltage rail of the device DV_{DD} if the device is periodically switching between low power mode 2/3/4 (LPM) and active mode (AM) at a very high frequency.

3.1 Accumulation of Core Voltage and Prolongation

The core voltage that powers the digital domain of the MSP430 is generated internally by two DV_{DD}-sourced LDOs that are a part of the Power Management Module (PMM). Depending on the power mode either the high-power LDO (AM, LPM0, LPM1) or the low-power LDO (LPM2, LPM3, LPM4) is used to source the core voltage. In LPMx.5 both LDOs as well as the core voltage is turned off.

The high-power LDO that generates the core voltage in AM, LPM0, and LPM1 is a regulator with a regulation time constant that is at least an order of magnitude larger than the minimum active time achievable by the MSP430 (greater than 2 µs).

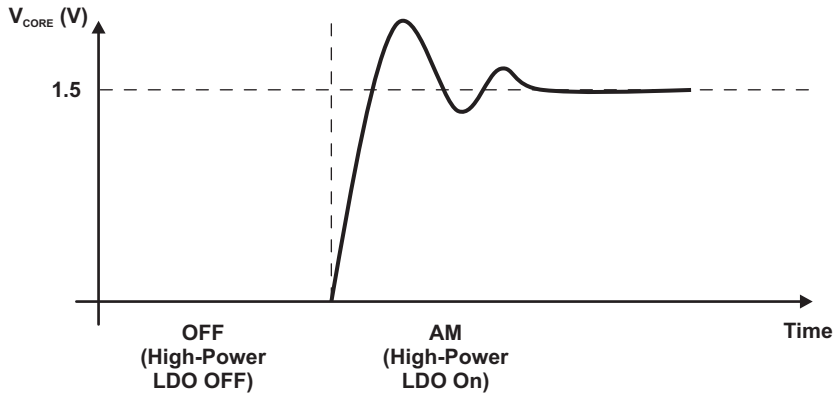

Figure 1. High-Power LDO Activation

Switching between active/LPM0/LPM1 and LPM2/3/4 causes the PMM to successively switch between the high-power and low-power LDOs. If this sequence occurs in short time intervals, the high-power LDO does not settle and there is a charge accumulation on the external capacitance connected to the V_{CORE} pin CV_{CORE} (470 nF). This results in an incremental increase in the core voltage until it is above the maximum allowable limit of 2.0 V.

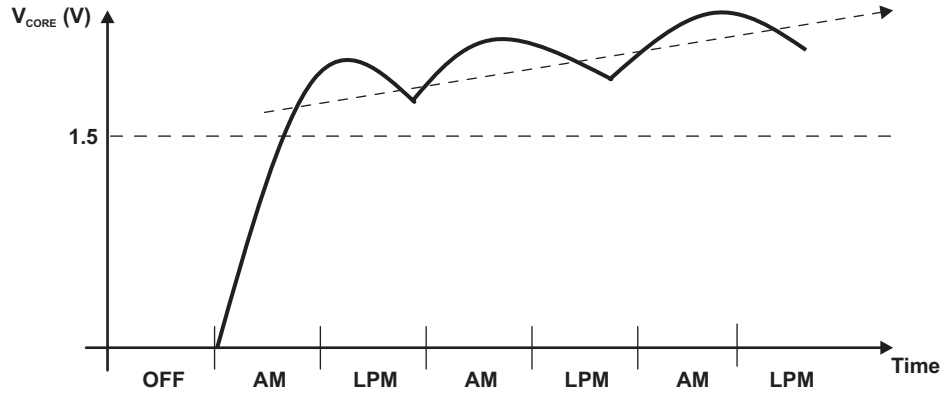

Figure 2. Voltage Accumulation With Repeated Switching Between AM and LPM

To prevent this effect, a prolongation mechanism is implemented in PMM that prolongs the active time of the PMM independent of the application. This prolongation mechanism is enabled by software at start up in the boot code. When switching at a high frequency, at every eighth instance of being in active mode, the PMM forces an active time of at least 1 VLO clock cycle to give the high-power LDO enough time to settle.

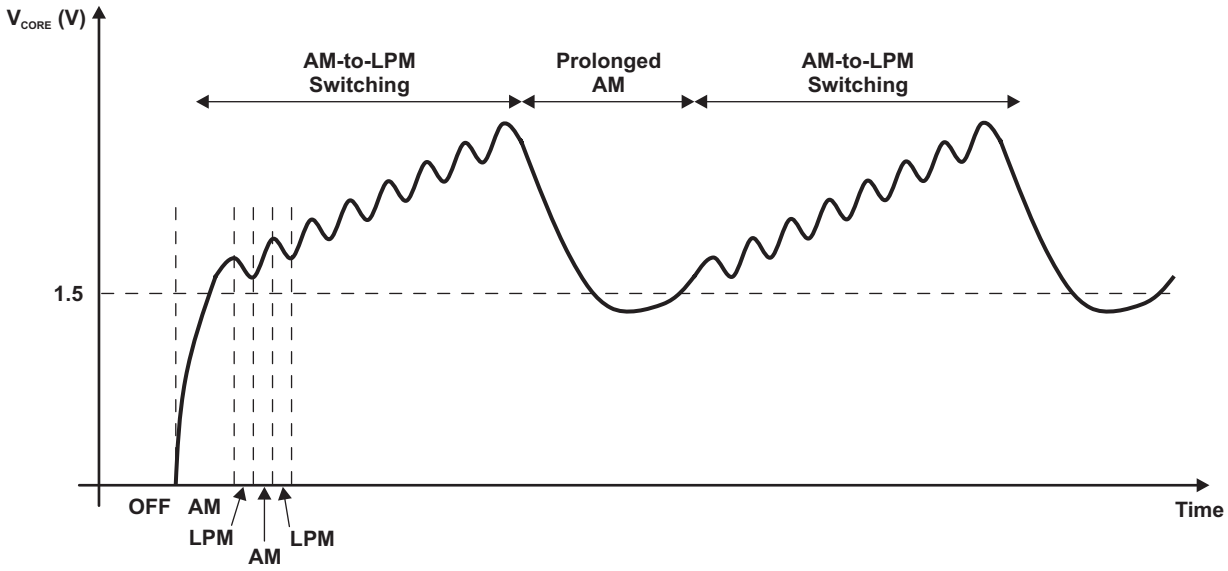

Figure 3. Prolongation Mechanism

In affected devices, the prolongation mechanism that prevents the accumulation of V_{CORE}, is not enabled. This results in an increased core voltage under specific conditions as described in Section 3.2.

3.2 Susceptible Conditions for V_{CORE} Accumulation

The effect of V_{CORE} accumulation can be seen when the device switches periodically between AM and LPM2/3/4 modes while remaining in both modes for very short time intervals. Figure 4 shows the timing budget window for which this effect can be seen:

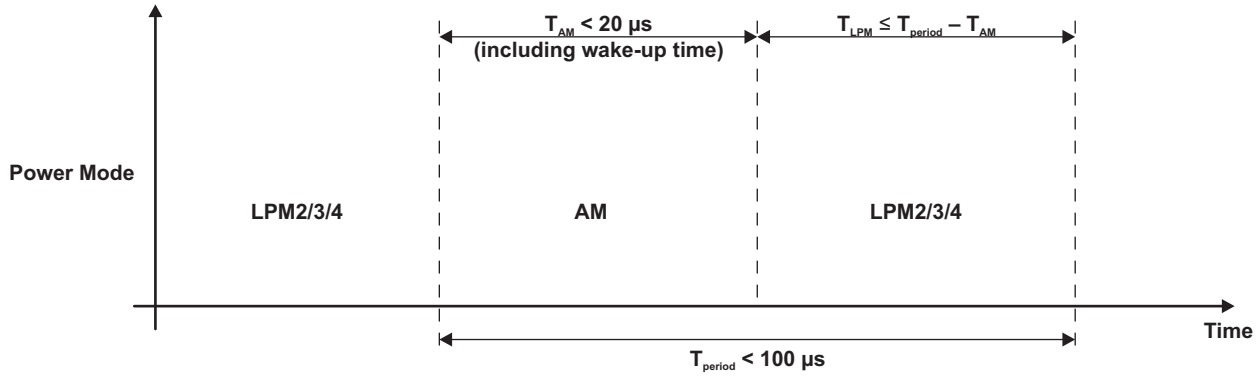

Figure 4. Conditions for Voltage Accumulation

From Figure 4, it can be seen that the device is required to be in active mode for a time period less than 20 µs, contributing to a total time period of less than 100 µs and limiting the time in LPM2/3/4 mode to less than or equal to 80 µs. The minimum T_{AM} includes the system wakeup time which is specified in the device datasheet as $t_{wake-up-FAST}$.

Due to a maximum susceptible AM time of 20 µs, only the $t_{wake-up-FAST}$ configuration of PMM low side is affected. If the PMM low side is configured to operate in $t_{wake-up-SLOW}$ (typically greater than 100 µs) the V_{CORE} accumulation would not occur.

3.3 Characteristics of V_{CORE} Accumulation

The following list describes the impact of V_{CORE} accumulation:

- With shorter T_{AM} and T_{LPM}, the resulting V_{CORE} can increase up to DV_{DD}:
  In testing, typical seen value was T_{AM} = 4.5 µs and T_{LPM} = 30 µs (for V_{CORE} = DV_{DD}).
- V_{CORE} increases approximately 5 to 10 mV per LPM-to-AM transition
- The ratio between T_{AM} and T_{LPM} has no significant influence
- The system frequency has no influence
- At lower temperatures, increased T_{AM} andT_{LPM} times are required to cause the issue
- If a nonstandard C_{VCORE} (470 nF) is used, note that a smaller C_{VCORE} reduces T_{AM} and T_{LPM} times.

3.4 System Effects of V_{CORE} Accumulation

When the core voltage increases beyond expected values and up to DV_{DD}, the following effects can be observed:

- A short term effect of V_{CORE} accumulation is seen as improper operation of the digital domain (CPU, Digital Peripherals). The device behavior is not predictable in this case.
- The long term effect of V_{CORE} accumulation can cause reduced endurance of the digital domain over the life time of the device.

4 How to Determine if the Application is Affected

The flowchart in Figure 5 highlights specific areas to assess within a given application to determine if the conditions previously outlined are present:

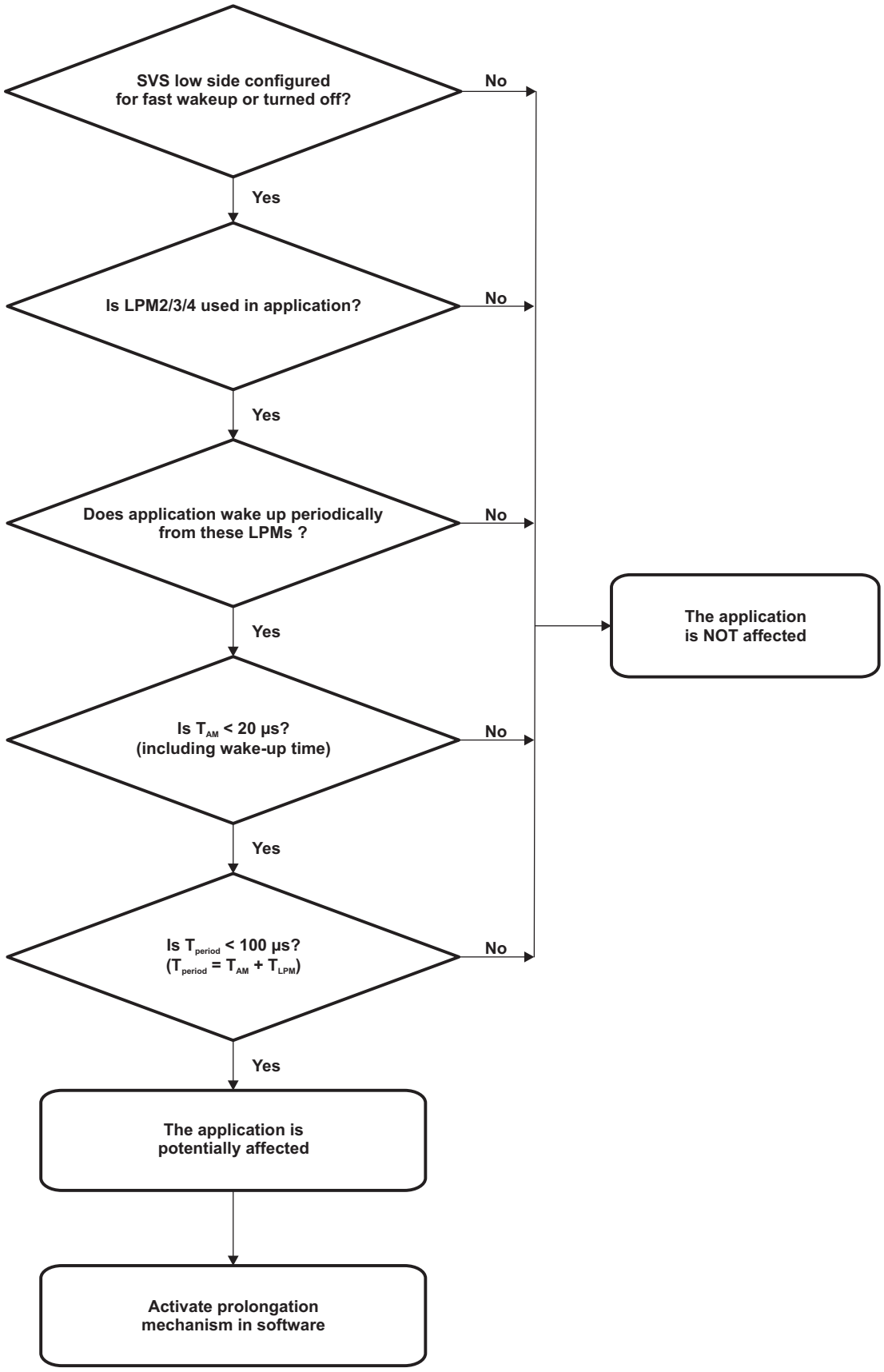

Figure 5. Determine If Application is Affected

5 Software Fix

The V_{CORE} accumulation is fixed by enabling the prolongation mechanism in software. The following lines of code need to be implemented before periodic execution of LPM-to-AM-LPM. It is recommended to execute the code at program start:

ASM code:

```
mov.w  #0x9602, &0110h;
bis.w  #0x0800, &0112h;
```

C code:

```
*(unsigned int*)(0x0110)=0x9602;
*(unsigned int*)(0x0112)|=0x0800;
```

The automatic prolongation mechanism is disabled with a BOR and must be enabled after each boot code execution.

5.1 Effects of Active Prolongation Mechanism

The prolongation mechanism has no impact on startup, wakeup, or system response times. Because the prolongation mechanism keeps the high-power LDO in PMM enabled every eighth LPM-to-AM cycle for at least one VLO cycle, independent of application code execution, the average current consumption over eight LPM-to-AM cycles might be increased based on application timing budget.

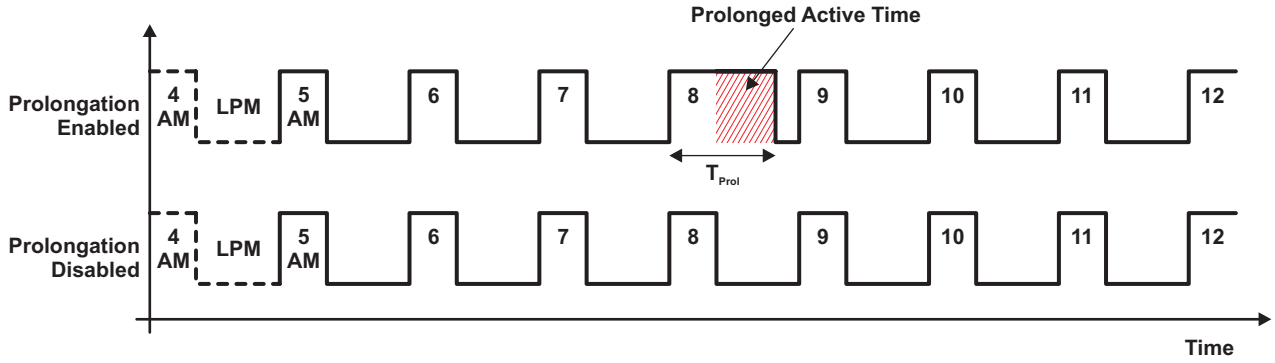

Figure 6. Prolonged Active Time

During prolonged active time, the system is in quasi LPM2/3/4 but the high-power LDO remains active to regulate the V_{CORE} voltage level. The prolongation delay is triggered with every eighth LPM-to-AM transition and keeps the high-power LDO enabled for:

1 VLO cycle × T_{Prol} < 2 VLO cycles

Depending on application code execution during the eighth AM, the prolonged active time can be 0 µs. During prolonged active time, the system consumes 20 µA to 40 µA (typically 33 µA) instead of the current specified in the device-specific data sheet for LPM2/3/4.

6 Summary

The information in this document provides the reader with information that can be applied in assessing the susceptibility of an application to the unintended accumulation of V_{CORE} voltage. A software solution is provided to fix the issue.

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