

V_{CC} vs System Speed of MSP430G2x44

ABSTRACT

This document provides analysis details and specific results of the CPU45 errata affecting the following devices:

MSP430G2744

MSP430G2544

MSP430G2344

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1 Issue Description

The system speed performance above 4.15 MHz versus minimum required V_{CC} as shown in Figure 1 from the data sheet can be met under certain specific conditions only. If these conditions are not fulfilled, the CPU status register and R4 through R15 register contents may become unintentionally changed during some CPU register operations. This behavior is dependent on voltage, frequency, and clock duty cycle with certain operand and instruction combinations. Such code sequences are common in C-compiler generated application code.

When a CPU register is affected, the resulting value in the CPU register cannot be predicted.

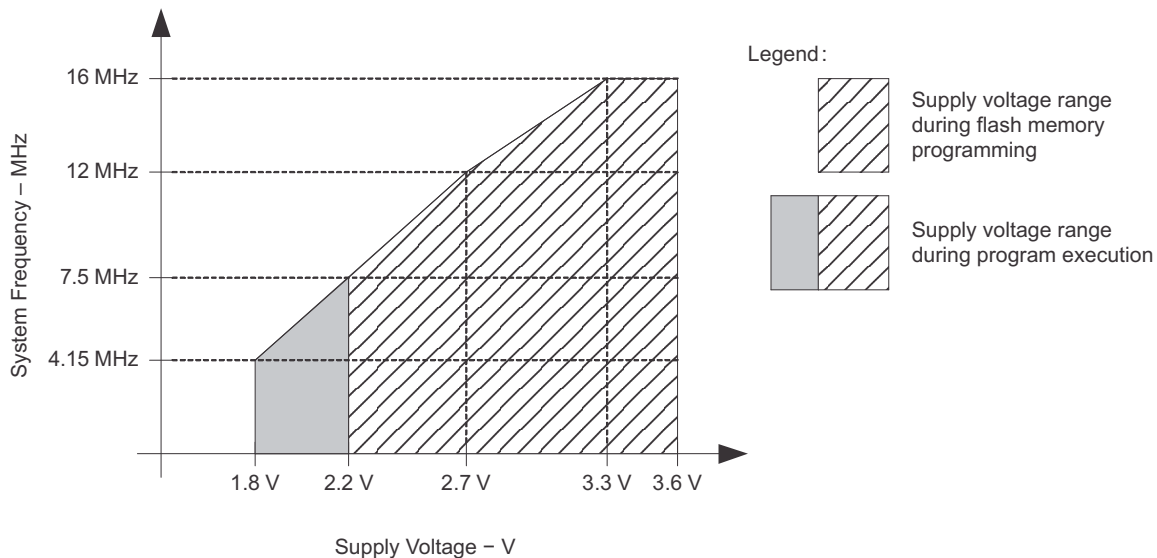


Figure 1. Recommended Operating Conditions for System Frequency vs Supply Voltage

2 Conditions

This section describes the safe operation conditions.

The following operating conditions should be considered to avoid the functional issue described above.

2.1 Clock Duty Cycle Conditions

For positive clock duty cycles of 50% or higher, the data sheet operating conditions hold fully true. This condition can be met with external positive 50% or higher duty cycle clocks or internally divided clocks including divided DCO clocks.

2.2 DCO Safe Operation Over All Temperature Conditions

Figure 2 shows the safe operation area for the system clock (MCLK or CPU clock) when using the DCO without an internal clock divider.

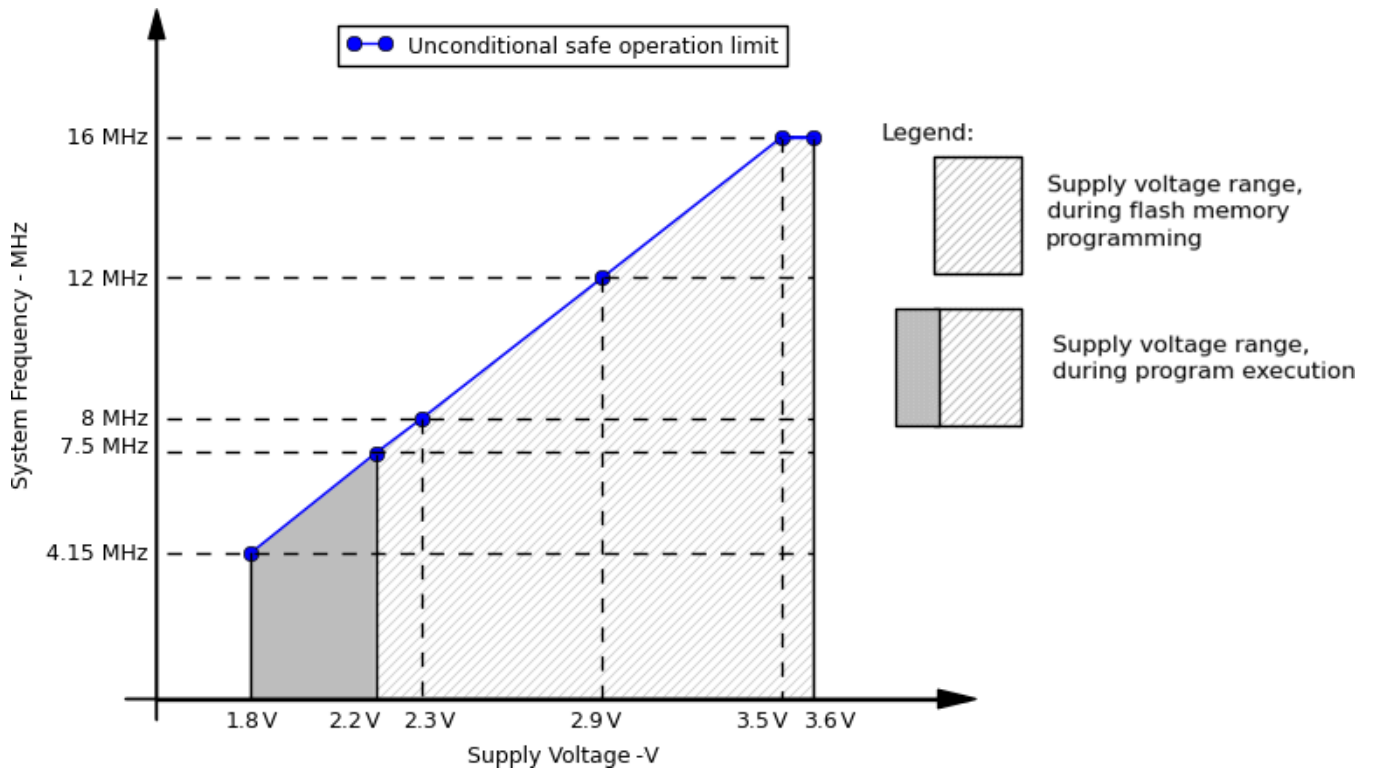


Figure 2. V_{CC} vs Frequency – Safe Operating Conditions for DCO and Calibration Settings

2.3 HFO or External Clock Safe Operation Over All Temperatures and Duty-Cycle Conditions

Figure 3 shows the safe operation area for the system clock (MCLK or CPU clock) when using an external clock or the device HFO without an internal clock divider.

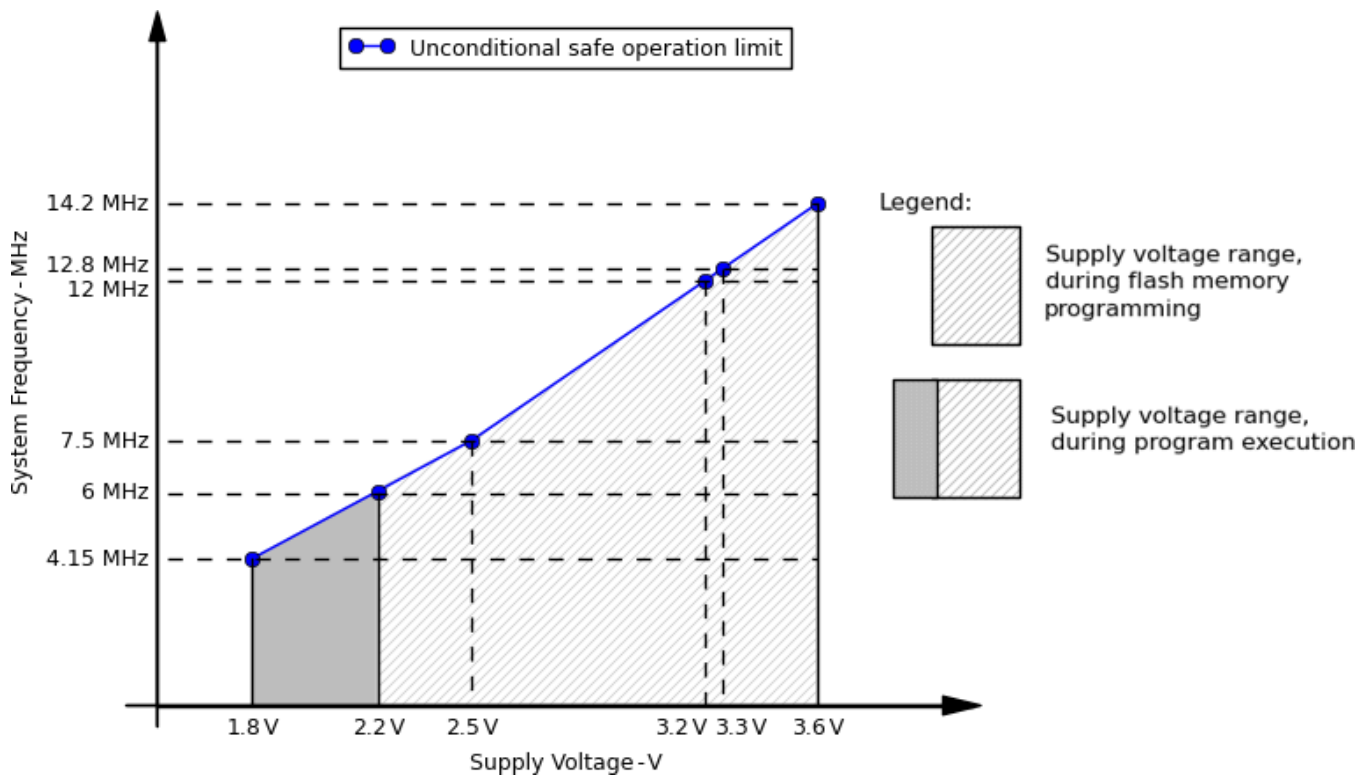


Figure 3. V_{CC} vs Frequency – Safe Operating Conditions for LFXT1 in HF Mode and for Digital External Clock Sources

3 Workarounds and Solutions

3.1 Application Related

- Reduce the system frequency (MCLK or CPU clock) according to the V_{CC} vs frequency graphs shown in Figure 2 and Figure 3.
- Increase V_{CC} according to the V_{CC} vs frequency requirements as shown in Figure 2 and Figure 3. Do not exceed the *Recommended Operating Conditions* as stated in the data sheet.
- Use internal dividers for the MCLK clock sources.
- Use external clock generators that provide a 50% or higher duty cycle.

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