Application Report

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PGA900 as a Capacitive Load Driver

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Enhanced Industrial and Precision Analog

ABSTRACT

Capacitive load drive is one of the most common causes of operational amplifier stability issues. The load capacitance, C_L, interacts with the open-loop output impedance of the amplifier, Z_O, by adding a single or double pole in the open-loop response. The additional pole or poles degrades the circuit phase margin, resulting in transient overshoot and ringing, ac gain peaking, reduced bandwidth, and possibly full oscillations. Therefore, the design requires phase compensation to stabilize the circuit so it produces an optimal output response. Finding the open-loop output impedance lets the designer select compensation components for occasions when the PGA900 DAC gain output is used as a capacitive load driver.

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1 Introduction

Capacitive load drive is one of the most common causes of operational amplifier stability issues. The load capacitance, C_L, interacts with the open-loop output impedance of the amplifier, Z_O, by adding a single or double pole in the open-loop response. The additional pole or poles degrades the circuit phase margin, resulting in transient overshoot and ringing, ac gain peaking, reduced bandwidth, and possibly full oscillations. Therefore, the design requires phase compensation to stabilize the circuit so it produces an optimal output response.

One way to stabilize an operational amplifier circuit for capacitive load drive is to add a resistor, R_{ISO}, between the amplifier's output and C_L. As this added resistor is outside the feedback path, this method is known as out-of-loop compensation. R_{ISO} acts with C_L and introduces a zero into the transfer function to cancel the phase shift from the poles caused by Z_O and C_L. The addition of the zero in the transfer function returns the phase margin to a stable level.

However, the R_{ISO} circuit suffers from accuracy issues when the amplifier is required to drive current due to the voltage drop formed across R_{ISO}. The errors could be corrected if the load is known and constant, but in cases when the circuit load is unknown or dynamic, move R_{ISO} inside the overall feedback path (see Figure 1). This configuration is known as in-loop compensation. In this configuration, dc and low-frequency feedback is provided from the load through R_F, restoring the dc and low-frequency accuracy of the circuit. Feedback capacitor, C_F, provides a high-frequency feedback path (FB_2) to bypass the feedback path formed from R_{ISO}, C_{LOAD}, and R_F (FB_1). This compensation method permits stable drive of any amount of capacitance load.

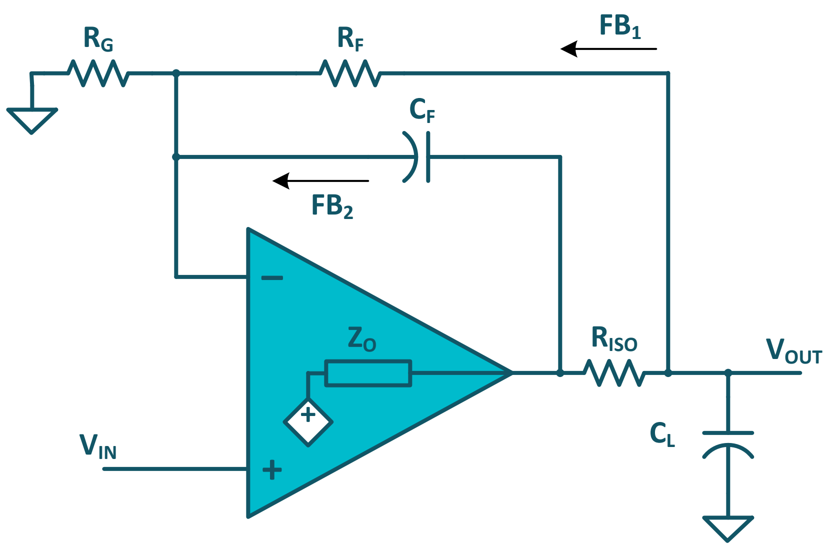


Figure 1. In-Loop Compensation: Circuit for Capacitive Load Drive

2 Selecting Compensation Components

As shown in Figure 2, the PGA900 DAC output amplifier, Z_O, displays complex frequency behavior. In the frequency range from DC up to amplifier bandwidth, Z_O behaves as a resistor, capacitor, and inductor. If Z_O is plotted with the different capacitance loads from 1 nF to 470 nF, intersections occur in the region where Z_O behaves as an inductor.

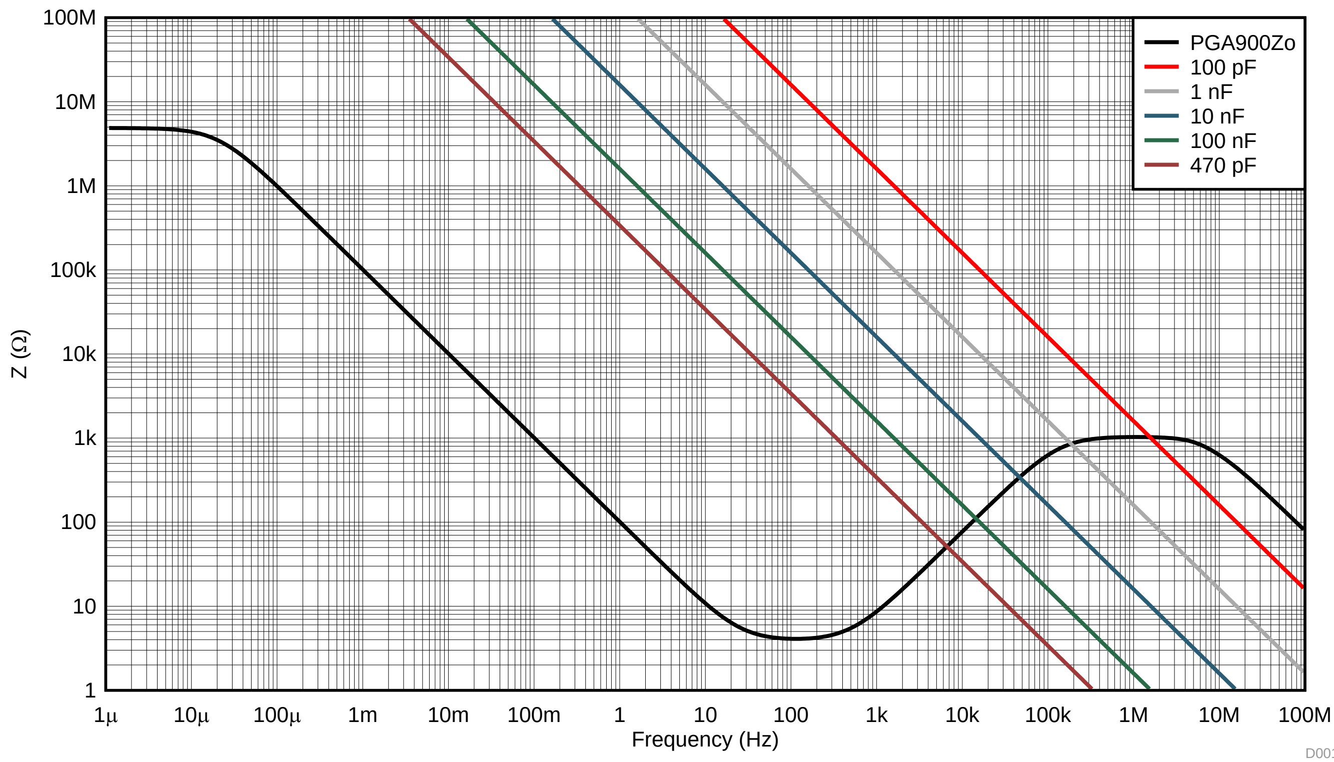


Figure 2. PGA900 Open-Loop Output Impedance Z_O and Capacitors Load Impedance Z_C Over Frequency

For stability analysis, replace Z_O with an equivalent open-loop output inductance, L_O = 1.2294 mH. By adding the isolating resistor, R_{ISO}, between the output of the amplifier (or L_O) and the load capacitance, C_L, the interaction results in the addition of a double pole, f_P, and a zero, f_Z, to the unloaded open-loop gain, A_{OL}. To maximize bandwidth and limit the feedback loop phase-shift at high frequencies to 90°, select R_{ISO} so that $f_P = f_Z$. Using this criteria, calculate R_{ISO} with Equation 1.

$$R_{ISO} = \sqrt{\frac{L_O}{C_L}} \tag{1}$$

The feedback path through C_F (FB_2) becomes the dominate feedback in the circuit after the frequency: f_P‘ = ½ π × (R_{ISO} + R_F) × C_F. FB_2 must be designed so it is the dominate feedback path before FB_1 begins to compromise the circuit stability. Transferring feedback control to the bypass loop removes the second-pole effects from the new controlling feedback, which preserves stability. For the system to have the fastest response (fastest approach to the final value) possible without overshoot, select damping factor ζ = 1. By definition, this system is critically damped. Therefore, the designer can calculate that f_P‘ must be ≤ ¼ f_P. To satisfy this condition, calculate the value of the feedback capacitor with Equation 2.

$$C_F = \frac{4 \times R_{ISO} \times C_L}{R_{ISO} + R_F} \tag{2}$$

3 PGA900 Compensation Components for Different C_L

PGA900 DAC gain stage has four fixed-gain selections: 2 V/V, 4 V/V, 6.67 V/V, and 10 V/V. These gain selections result in the feedback resistor values of 75 kΩ, 112.5 kΩ, 127.5 kΩ, and 135 kΩ, respectively. Figure 3 shows the PGA900 internal circuitry for a gain selection of X V/V.

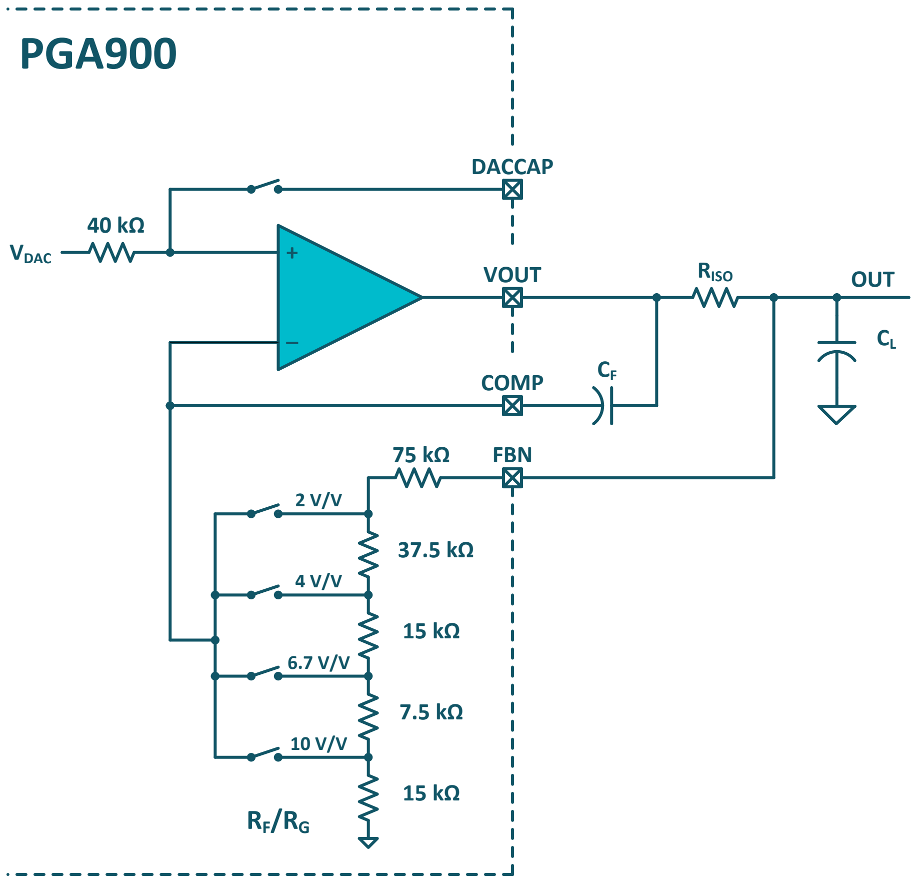


Figure 3. PGA900 Gain Selection Circuit With Capacitive Load Compensation

Using the previous procedure, select decoupling components R_{ISO} and C_F for different capacitive loads and gains. Table 1 to Table 4 show decoupling components that provide the highest bandwidth (BW) for 1-nF, 10-nF, 100-nF, and 470-nF capacitive loads, respectively.

Table 1. PGA900 Decoupling Components for 1-nF Capacitive Load

C_L (nF)	R_{ISO} (Ω)	Gain (V/V)	R_F (kΩ)	C_F (pF)	BW (kHz)
1	1100	2	75	56	37.3
1	1100	4	112.5	39	36.3
1	1100	6.67	127.5	33	37.8
1	1100	10	135	33	35.7

Table 2. PGA900 Decoupling Components for 10-nF Capacitive Load

C_L (nF)	R_{ISO} (Ω)	Gain (V/V)	R_F (kΩ)	C_F (pF)	BW (kHz)
10	348	2	75	180	11.7
10	348	4	112.5	120	11.8
10	348	6.67	127.5	120	10.4
10	348	10	135	100	11.8

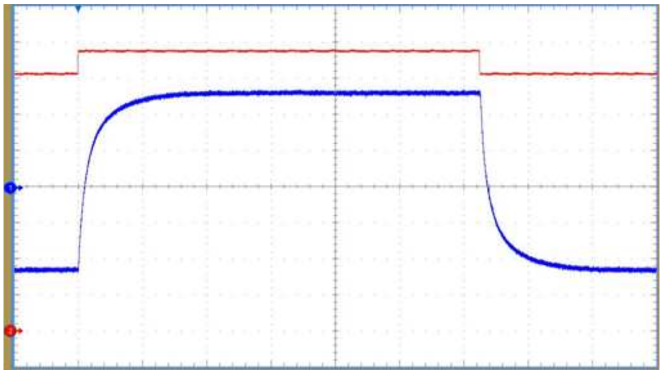
Table 3. PGA900 Decoupling Components for 100-nF Capacitive Load

C_L (nF)	R_{ISO} (Ω)	Gain (V/V)	R_F (kΩ)	C_F (pF)	BW (kHz)
100	110	2	75	560	3.8
100	110	4	112.5	390	3.6
100	110	6.67	127.5	330	3.8
100	110	10	135	330	3.6

Table 4. PGA900 Decoupling Components for 470-nF Capacitive Load

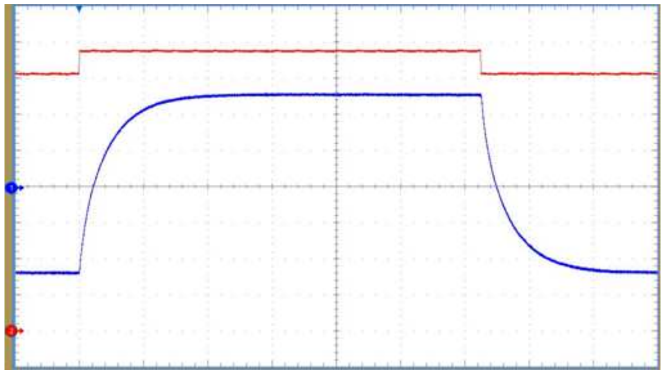
C_L (nF)	R_{ISO} (Ω)	Gain (V/V)	R_F (kΩ)	C_F (pF)	BW (kHz)
470	51.1	2	75	1200	1.8
470	51.1	4	112.5	820	1.7
470	51.1	6.67	127.5	820	1.5
470	51.1	10	135	680	1.7

Using values from Table 3 for a 100-nF capacitive load, small signal and large signal step response measurements were taken to verify stable circuit transient behavior. Figure 4 to Figure 11 show the results of these measurements. As predicted, all of these responses have similar response, critically damped, fast settling without overshoot.



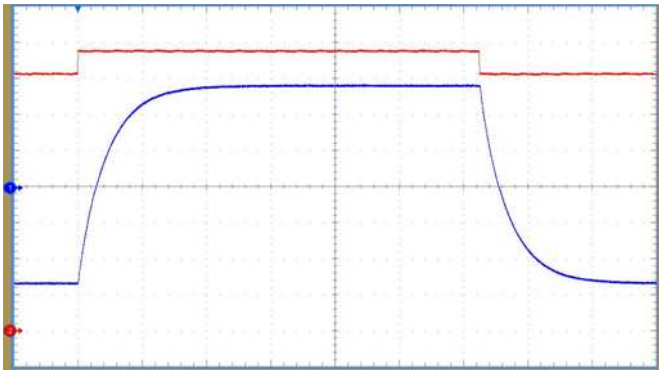
100 µs/div Blue line = 20 mV/div Red line = 80 mV/div

Figure 4. Small Signal Step Response G = 2, V_{IN} = 50 mV, V_{OUT} = 100 mV



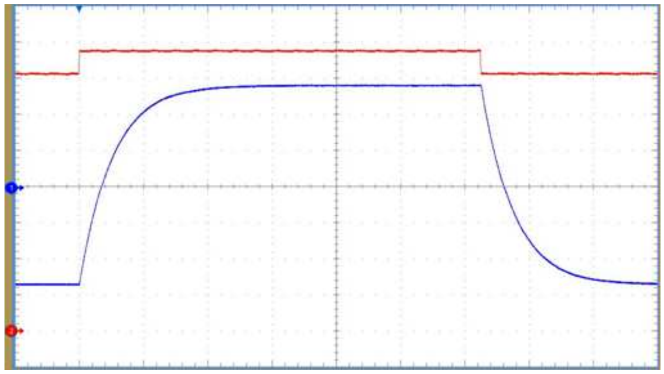
100 µs/div Blue line = 40 mV/div Red line = 80 mV/div

Figure 5. Small Signal Step Response G = 4, V_{IN} = 50 mV, V_{OUT} = 200 mV



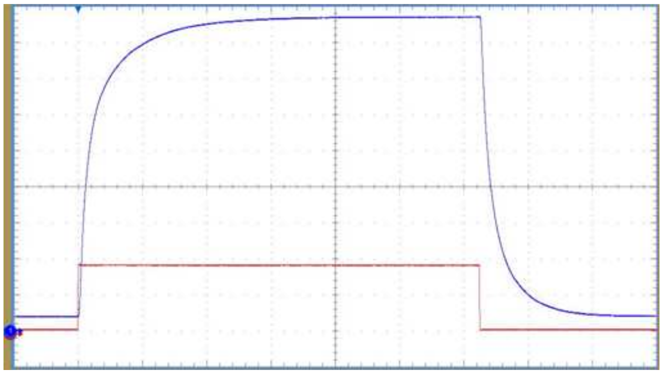
100 µs/div Blue line = 60 mV/div Red line = 80 mV/div

Figure 6. Small Signal Step Response G = 6.67, V_{IN} = 50 mV, V_{OUT} = 333 mV



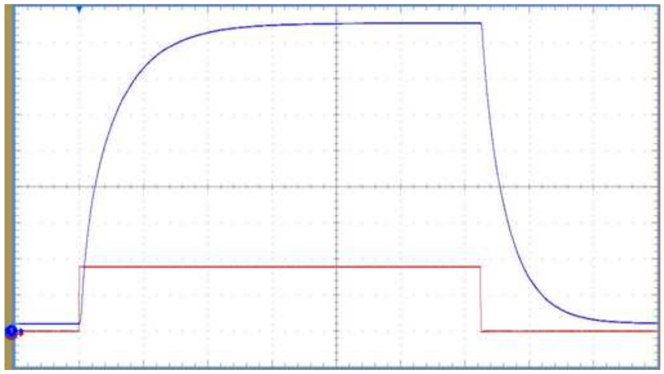
100 µs/div Blue line = 90 mV/div Red line = 80 mV/div

Figure 7. Small Signal Step Response G = 10, V_{IN} = 50 mV, V_{OUT} = 500 mV



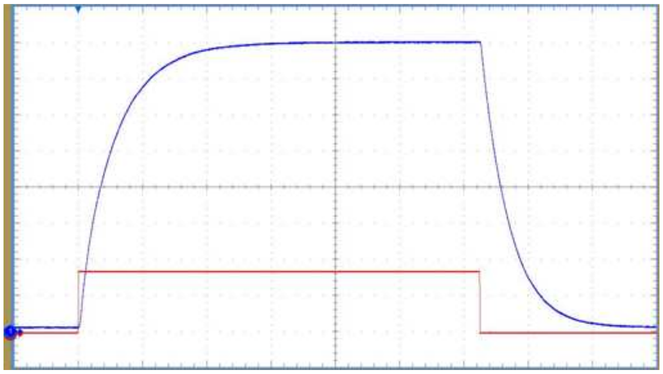
100 µs/div Blue line = 300 mV/div Red line = 700 mV/div

Figure 8. Large Signal Step Response G = 2, V_{IN} = 1.25 V, V_{OUT} = 2.5 V



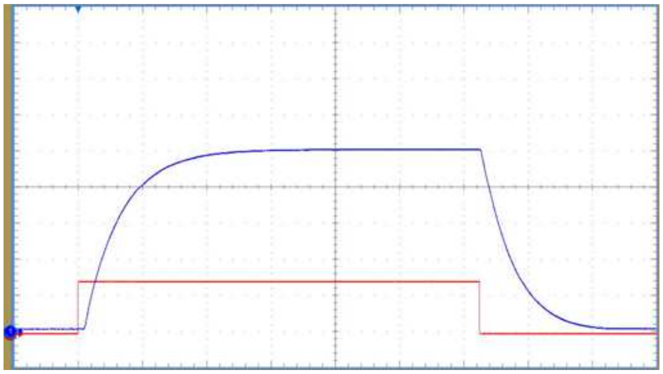
100 µs/div Blue line = 600 mV/div Red line = 700 mV/div

Figure 9. Large Signal Step Response G = 4, V_{IN} = 1.25 V, V_{OUT} = 5 V



100 µs/div Blue line = 1 V/div Red line = 700 mV/div

Figure 10. Large Signal Step Response G = 6.67, V_{IN} = 1.2 V, V_{OUT} = 8 V



100 µs/div Blue line = 2 V/div Red line = 700 mV/div

Figure 11. Large Signal Step Response G = 10, V_{IN} = 1 V, V_{OUT} = 10 V

4 Conclusion

Finding the open-loop output impedance lets the designer select compensation components for occasions when the PGA900 DAC gain output is used as a capacitive load driver. The component selection maximizes bandwidth and phase margin of the system for a specific capacitive load. Keeping the system response critically damped obtains the fastest output signal settling without overshoot. It is the designer's responsibility to adjust component values to ensure desired operation over the temperature range and the initial and life tolerances of the component.

5 References

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