Quick Start Guide

TDP0604 Configuration Guide

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ABSTRACT

The TDP0604 is an HDMI 2.0 redriver supporting data rates up to 6Gbps. The device is backwards-compatible to HDMI 1.4b. The high-speed differential inputs and outputs can be either AC-coupled or DC-coupled which qualifies the TDP0604 to be used as a DP++ to HDMI level shifter or HDMI re-driver.

This document is a quick start-up guide for the TDP0604 devices.

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1 Device Configuration Guide

1.1 General Configuration Pin

This section describes the general pin configurations.

EN: When low, TDP0604 will be held in reset. The EN pin has a internal 250-kΩ pullup to VIO. For passive circuitry implementation, add an external 0.22-µF pulldown capacitor on the EN pin.

VIO: The TDP0604 supports 1.2-V, 1.8-V, and 3.3-V LVCMOS levels depending on the source I/O voltage requirement. The VIO pin is used to select which voltage level is used for the following 2-level control pins: LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, and SDA/CFG1.

Table 1-1. VIO Voltage Base on the LVCMOS Signaling Level

VIO Pin	LVCMOS Signaling Level
VIO < 1.5 V	1.2 V
1.5 V < VIO < 2.5 V	1.8 V
VIO > 2.5 V	3.3 V

Mode (pin-strap or I2C mode): The MODE pin provides three modes of operation. There are two pin-strap modes and one I2C mode.

In pin-strap mode, if using the LV_DDC_SDA and LV_DDC_SCL for DDC snooping, the internal DDC buffer must be disabled. But if using the HV_DDC_SDA and HV_DDC_SCL for DDC snooping, the internal DDC buffer must be enabled.

In I2C mode, the DDC snoop feature is enabled by default but can be disabled by a register.

Table 1-2. Mode Pin Setting

Mode	Description
0	Pin-strap mode with internal DDC buffer enabled
R	Pin-strap mode with internal DDC buffer disabled
F	I2C mode

SCL/CFG0: In pin-strap mode, this is the CFG0 pin. Tie this pin to '0' for normal HDMI mode. In I2C mode, this is the SCL pin.

SDA/CFG1: In pin-strap mode, this is the CFG1 pin. The CFG1 pin needs to set to '0' for normal lane ordering, but set to '1' if the input/output lane order is swapped. In I2C mode, this is the SDA pin.

LINEAR_EN pin: In pin-strap mode, the LINEAR_EN sets the TDP0604 into either linear or limited re-driver mode. For HDMI 1.4 and 2.0, set the LINEAR_EN to '0' for HDMI source application and 'F' for HDMI sink application.

HPDOUT_SEL: The HPDOUT_SEL selects whether the HPD_OUT pin is push-pull, or open-drain. Since open-drain is not supported in the pin-strap mode, this pin needs to be NC or pulled to ground.

1.2 Transmitter Configuration

This section describes the transmitter configuration.

AC_EN: In pin-strap mode, the AC pin selects between AC-coupled or DC-coupled transmitter.

Table 1-3. AC_EN Pin Setting

AC_EN	Description
0	DC-coupled
1	AC-coupled

TXPRE: The TDP0604 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal preconditioning to offset interconnect losses between the TDP0604 transmitters and a TMDS receiver. Pre-emphasis and de-emphasis is not implemented on the clock lane. There are two methods to implement pre-emphasis, pin strapping or through I2C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode. When using pin-strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TDP0604 is operating in HDMI 1.4 or HDMI 2.0.

Table 1-4. TXPRE Pin Setting

TXPRE	Description
0	3.5 dB pre-emphasis
R	–2.5 dB de-emphasis
F	0 dB
1	6 dB pre-emphasis

TXSWG: The TDP0604 transmitter swing level can be adjusted in both pin-strap and I2C mode.

In I2C mode, TX swing settings are controlled independently for each lane (both clock and data) through registers. In addition, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14_VOD and HDMI20_VOD registers.

In pin-strap mode with limited re-driver option enabled, the TXSWG pin adjusts the default 1000-mV swing. In HDMI 1.4 the TXSWG pin controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the swing for data lanes while the clock lane will remain at default value.

Table 1-5. TXSWG Pin Setting

TXSWG	HDMI1.4 Limited Mode	HDMI2.0 Limited Mode
0	Default (1000 mVpp)	Default (1000 mVpp)
R	Default –5%	Default –5%
F	Default (1000 mVpp)	Default (1000 mVpp)
1	Default (1000 mVpp)	Default +5%

1.3 Receiver Configuration

This section describes the receiver configuration.

CTLEMAP_SEL: In pin-strap mode, CTLEMAP_SEL selects the TDP0604 CTLE map being used. Tie this pin to '1'.

Choose input receive equalization through ADDR/EQ0 and EQ1:
For fixed equalization options, see the *EQ settings* table in the *TDP0604* data sheet.

2 Summary

The parameters in this guide serve as a starting point for configuring the TDP0604 device for your application.

3 References

- Texas Instruments, *TDP0604 6-Gbps, DC or AC-Coupled to HDMI™ 2.0 Level Shifter Hybrid Redriver* data sheet

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