UNITRODE

Design Note

UCC3858 "Energy Star" PFC
Evaluation Board, Schematic, and List of Materials

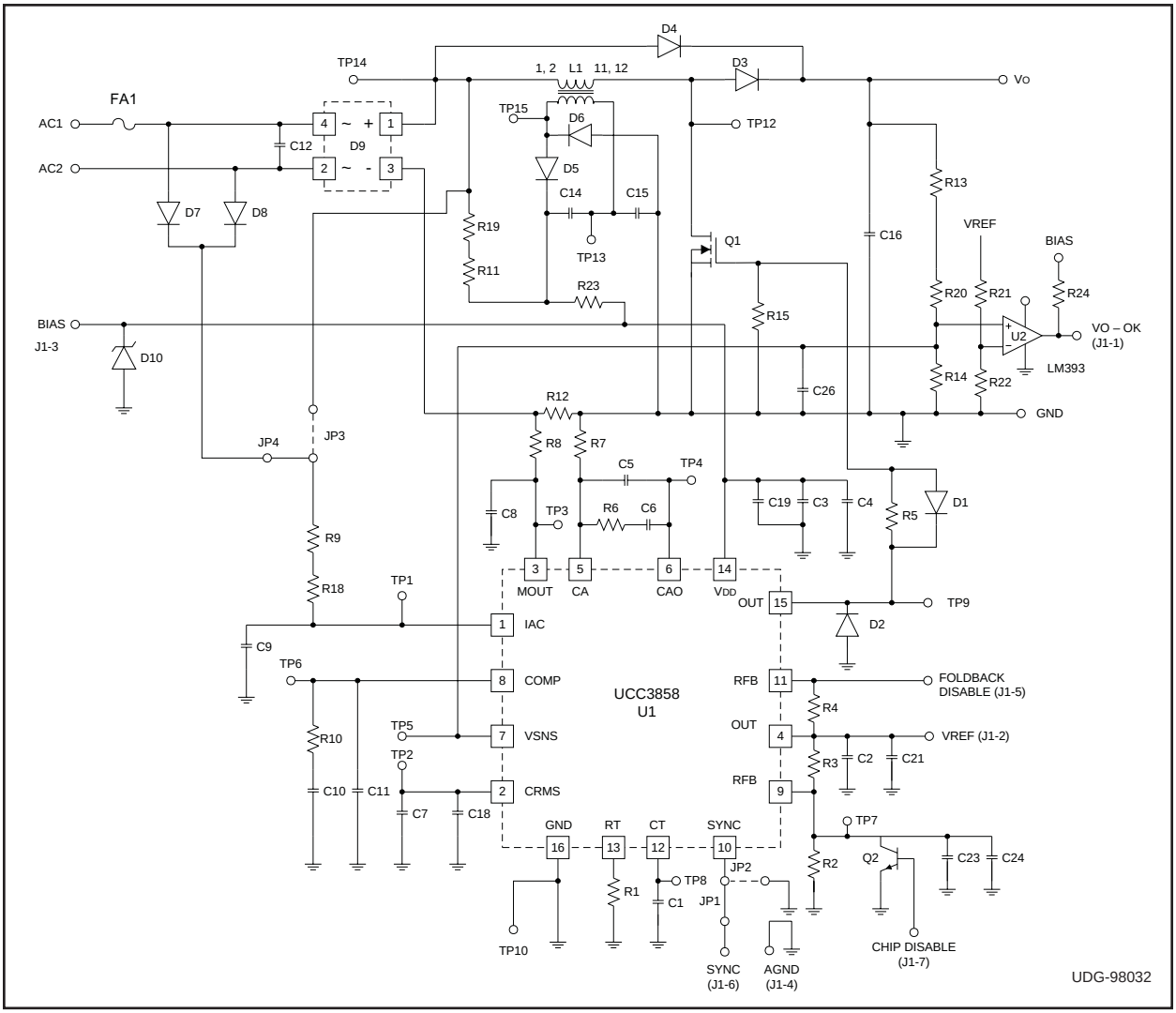
By Dhaval Dalal

Introduction

The UCC3858 provides all functions necessary for active power factor corrected preregulators which require high efficiency for low power operation. Its operation is similar to the previously designed Unitrode PFC preregulators with some added features. It has frequency foldback at light load operation for higher efficiency and leading edge modulation to allow better ripple cancellation on the boost output capacitor.

The UCC3858 demonstration board is designed to illustrate the performance of the IC in a 250W boost converter with power factor correction. The board is designed to handle a wide input operating voltage range (85-265 VAC) and a wide load range (5W-250W).

***Caution**: High voltage levels are present on the demo board whenever it is energized. Proper precautions must be taken when working with the board. The output capacitor has high levels of energy storage and it must be discharged before the load is removed.*



Operating Guidelines

The operating guidelines for the evaluation board are provided with reference to the schematic in Figure 1 and the parts list in Table 1.

Step 1. Bias Voltage Application

The demo board is shipped with self-biasing circuit enabled and bias voltage set at 16V. The board will become functional at approximately 90V RMS input when sufficient bias voltage develops. To use external bias voltage and remove self-biasing, R23 should be removed. The chip must be biased with a voltage between 10-18 V. On the demo board, the bias can be applied to J1-3 with respect to Ground (J1-4). For ideal performance ensure that VDD is maintained below 16V during the circuit operation.

For evaluating the demo board, apply external bias voltage first and ensure that the chip is operational. A valid VREF (7.5V) or a PWM signal on the Out pin (pin 15) can confirm the IC operation.

Step 2. Preset values and adjustments

If needed, the default settings of the board can be adjusted as follows.

The free running frequency of the oscillator is set at 92 kHz. If needed, the free running frequency can be adjusted by modifying R1 or C1.

Output voltage level is set at 375V nominal. It can be adjusted by changing R14.

The frequency foldback level is set to a load level of 75W and below. The foldback level can be altered by changing the resistive divider R3/R2.

The minimum switching frequency is set at 40 kHz, changing R4 will enable that to be adjusted.

If the foldback mode is not desired, pin 11 (J1-5) needs to be grounded.

Pulling J1-7 high can disable the chip operation. If not used, J1-7 should be held low to prevent noise susceptibility.

Vo-OK (J1-1) indicates that the output is above a set threshold (set by R21/R22).

Step 3. AC Voltage Application

AC voltage should be applied across terminals AC1 and AC2 after the chip operation has been verified. AC voltage should be applied only when some load is present across Vo and GND.

With the AC voltage within the input range, the output voltage should be regulated and the input current should track the input voltage shape with unity power factor. The operation of the circuit is verified over the line and load range and shows efficiency in 92% range. At lighter loads, there may be some distortion in the line current due to DCM operation. In the foldback mode, this distortion may be more pronounced as the available maximum duty cycle is reduced. At very light loads, the converter could go into pulse skipping mode - in the foldback mode, the pulse-skipping occurs at even lighter load.

Step 4. Synchronization

UCC3858 can be synchronized to a downstream converter for minimum ripple current on the bulk capacitor. A sync pulse can be applied to pin 10 of the IC (J1-6 on the board). To make synchronization work, move the jumper from JP2 position to JP1 position. The IC synchronizes to the leading edge of the incoming pulse and turns off the PWM output. PWM is turned on again when PWM comparator output goes high. This synchronized leading edge modulation scheme minimizes the ripple current on the bulk output capacitor (C16). Sync signal is TTL compatible, but can be as high as 14V. The sync frequency has to be higher than the free running frequency of the oscillator.

Debugging Hints

The demo board has been verified for operation over line and load range. However, the due to the complexity of the board some debugging may be required for a different operating environment/condition.

The Iac pin (pin 1) is sensitive to noise coupling. It has been adequately bypassed, but it may show irregular behavior if it is probed or is in a noisy environment. If this pin sees irregular behavior or current spikes near zero crossings, it can make the converter misbehave. Pin 2 can be monitored to detect if there are any missed or double pulses. It is essential that the IC be properly bypassed (VDD to GND) to minimize noise sensitivity. Putting the IC in a socket for evaluation or reducing the bypass capacitor C3 from 1μF could lead to irregular operation. In some situations, the sync pulse can inject noise into the system. In that case, it may help to slow down the rise time of the sync pulse. Other decoupling techniques (heavier bypassing on FBLVL pin) may also help.

While the demo board is primarily intended for use with an AC input, in some cases it may be necessary to evaluate it with DC input voltage. In these

instances, the different RMS sensing scheme of the UCC3858 requires special handling. As described in the datasheet, the RMS sensing scheme requires a periodic zero crossing signal on the Iac pin (pin 1). With a DC input, Iac has to be manually pulsed to ground (at least twice) to clock in the voltage on Crms pin (pin 2) into the register for further processing. It also requires a resistive divider from the input voltage going into the Crms pin. With every change in input voltage, the Iac pulsing has to be repeated to ensure that the multiplier inputs are properly programmed.

Additional Information

For more information, pin description and specifications for the UCC3858 "Energy Star" PFC, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

Reference Designator	Part Description	Manufacturer	Part Number
C1	330pF, 63V, Ceramic capacitor, CT		
C2	0.47µF, 50V, Film capacitor, bypass		
C3	1µF, 50V, Film Capacitor, bypass		
C4	100 µF, 25V, Aluminum Capacitor, bias		
C5	47pF, 100V, Ceramic Capacitor		
C6, C9	270pF, 63V, Ceramic Capacitor		
C7	82nF, 50V, Film Capacitor		
C8	47pF, 100V, Ceramic Capacitor		
C10	2.2µF, 63V, Z5U, Ceramic Capacitor		
C11	0.39µF, 50V, Film Capacitor		
C12	1.5 µF, 400V, Metal film Capacitor		
C14, C15	1µF, 50V, Film Capacitor		
C16	330µF, 450V, Output Aluminum Capacitor		
C18	82pF, 100V, Ceramic Capacitor		
C19, C21, C23	4.7µF, 25V, Tantalum Capacitor		
C24	.68µF, 50V, Film Capacitor		
C26	150 pF, 50V, Ceramic Capacitor		
C13, C17, C20, C22, C25	Not used		
D1	Not used		
D2, D5, D6	30V, 1A Schottky Diode		1N5818
D3	600V, 8A Ultrafast Diode	International Rectifier	HFA08TB60
D4	600V, 6A Diode - 400A Surge	General Instrument	GI756CT
D7, D8	600V, 1A, Fast Recovery Rectifier		1N4937
D9	6A, 600V Bridge Rectifier		PB66
D10	18V, 0.5W Zener		1N5248
FH1,FH2	Fuse Holders		
FA1	Fuse, 6A, 250VAC		F124
L1	1mH, 5.5A pk, Boost choke, 18:1 turns ratio	Coiltronics	CTX08-13679-02

Table 1. Parts List

Reference Designator	Part Description	Manufacturer	Part Number
Q1	500V, 0.4 MOSFET	International Rectifier	IRFP450
Q2	npn Transistor		2N3903
R1	24k (Note 1)		
R2	2k		
R3	7.5k		
R4	100k		
R5	20		
R6	63k		
R7, R8	27k		
R9	2M		
R10	39k		
R11,R19	51k, 3W (Note 2)		
R12	.25 , 5W		
R13	560k		
R14	10k		
R15	47k		
R18	3M		
R19	Not used		
R20	670k		
R21	33k		
R22	20k		
R23	Not used		
R24	51k		
U1	High Efficiency, High power factor preregulator	Unitrode	UCC3858
U2	Comparator		LM393
HS1	Heat Sink	Aavid	513201
J1	Connector, 8-pos. .156 center	AMP	A1969

Table 1. Parts List (continued)

Notes:
1. Unless otherwise specified, all resistors are ¼W , Metal Film, 5%.
2. One resistor to take the place of both R11 and R19

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

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