Application Report
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Using the UC3832 Linear Controller with an NMOS Pass Element

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ABSTRACT

This application note describes the design of a linear power supply solution using the UC3832 linear controller and an N-channel pass FET. Setting the current limit, FET selection, voltage loop compensation, setting the RC timer, and configuring the Vadj pin are detailed. A design example shows the UC3832 in a practical application.

Note: Pin numbers referred to in this application note are referenced to the DW (SOIC-16) package. Pin numbers can be different on the other package options.

Setting the Current Limit

The current limit is designed to not limit the current until the output current is above the maximum required load current. Thus, even under worst case conditions of tolerances and temperature, etc., the system is able to deliver full operating current.

First the sense resistor is sized:

$$R_{sense} < \frac{Offset_{Comp\text{-}Min}}{I_{Load\text{-}Max}} \quad (1)$$

where $Offset_{Comp\text{-}Min}$ is the UC3832 minimum internal current limit comparator trip voltage, which is specified in the datasheet. The second step is to choose a value of the current sense resistor that satisfies Equation 1.

The final step is to calculate the maximum and minimum trip currents, based on worst case tolerances of the UC3832 and sense resistor.

$$I_{CurrentLimit\text{-}Max} = \frac{Offset_{Comp\text{-}Max}}{R_{sense\text{-}Min}} \quad (2)$$

$$I_{CurrentLimit\text{-}Min} = \frac{Offset_{Comp\text{-}Min}}{R_{sense\text{-}Max}} \quad (3)$$

$I_{CurrentLimit\text{-}Min}$ should still be greater than $I_{Load\text{-}Max}$. If not, pick a smaller sense resistor.

Selecting a FET

The critical NMOS FET characteristics are $R_{DS(on)}$, current capability, and the power dissipation capability of the package. Considering the minimum and maximum input voltage, the output voltage, and the maximum load current, the FET must have an $R_{DS(on)}$ that satisfies this equation:

$$R_{DS(on)} < \frac{V_{in\text{-}Min} - V_{out}}{I_{Load\text{-}Max}} \quad (4)$$

If the maximum resistance is greater than this, the output voltage will sag under heavy load due to

dropout. Note that this $R_{DS(on)}$ must be attainable with the minimum guaranteed gate to source voltage which equals the minimum FET drive voltage ($V_{Drive-Min}$) minus the output voltage. $V_{Drive-Min}$ is the voltage on pin 8 of the UC3832 (see Figure 1) and equals the voltage on pin 1 of the UC3832 ($V_{Bias-Min}$) minus the maximum transconductance amplifier output voltage (1.3V maximum below $V_{Bias-Min}$ according to the datasheet) minus the base to emitter drop across Q1 (around 0.7V).

In a linear regulator, almost all of the power is dissipated in the pass transistor. This is calculated using Equation 5.

$$P_{diss} = \left(V_{in-Max} - V_{out}\right) \times I_{CurrentLimit-Max} \quad (5)$$

where $I_{CurrentLimit-Max}$ is the maximum trip current of the system, which was calculated from Equation 2. The selected transistor must be large enough to dissipate P_{diss} or additional heat sinking will have to be used.

Voltage Loop Compensation

A simplified schematic of the voltage loop of the UC3832 is shown in Figure 1.

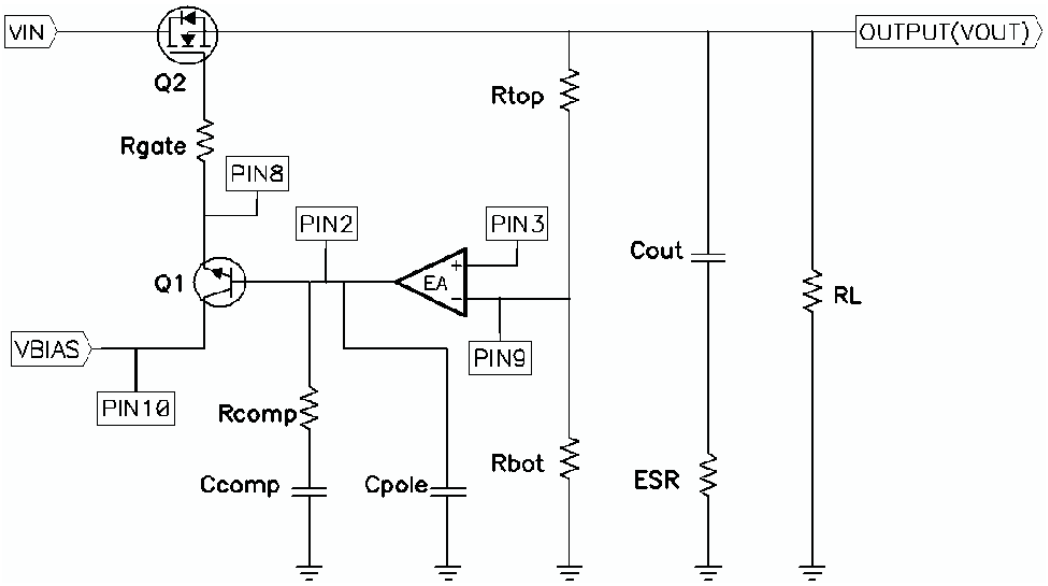

Figure 1. Simplified Voltage Loop of the UC3832

The models shown in this application note should be verified in the lab using Bode plots, or similar means to verify the design in the midst of circuit parasitics and variations in circuit parameters due to loading. This application note is only intended to give a starting point for selecting the compensation components. There is no substitute for lab verification.

In order to calculate the overall gain of the voltage loop, the designer must calculate the gain of each piece of the loop. The small signal component of the output voltage starts at the output voltage. The small signal travels through the output voltage divider (R_{top} and R_{bot}). It then encounters the transconductance error amplifier and the compensation components. Lastly, it travels through the pass transistor (Q2) and returns to the output voltage.

First, there is the DC gain of the voltage divider (output voltage to pin 9):

$$A_{DC} = \frac{R_{bot}}{R_{top} + R_{bot}} \quad (6)$$

Second, continuing through the loop, the small signal encounters the gain of the transconductance error amplifier, G_{M-TA}, times its output impedance and then the gain of the compensation network (pin 9 to pin 8):

$$A_{comp} = G_{M\text{-}TA} \times Z_{out} \times \frac{\frac{f \times j}{F_{CompZero}} + 1}{\left(\frac{f \times j}{F_{OriginPole}} + 1\right) \times \left(\frac{f \times j}{F_{CompPole}} + 1\right)} \quad (7)$$

Thus, the compensation zero is at:

$$F_{CompZero} = \frac{1}{2 \times \pi \times R_{comp} \times C_{comp}} \quad (8)$$

And the compensation pole is at:

$$F_{CompPole} = \frac{1}{2 \times \pi \times R_{comp} \times \left(\frac{C_{comp} \times C_{pole}}{C_{comp} + C_{pole}}\right)} \quad (9)$$

The error amplifier has a pole near the origin, which can be calculated from Equation 10:

$$F_{OriginPole} = \frac{1}{2 \times \pi \times Z_{out} \times (C_{comp} + C_{pole})} \quad (10)$$

In the above equations, Z_{out} is the output impedance of both the voltage and current error amplifiers combined in parallel. The impedance of each amplifier by itself is calculated by Equation 11, where the open loop gain and transconductance are read from the lowest frequency points on the graphs in the datasheet. The impedances are then combined in parallel to get Z_{out}.

$$Z_{Out\text{-}TA} = \frac{Gain_{Open\text{-}Loop}}{G_{M\text{-}TA}} \quad (11)$$

Lastly, there is the gain of the output stage (pin 8 to the output voltage):

$$A_{output} = \frac{RL}{RL + \frac{1}{gmFET}} \times \frac{\frac{f \times j}{F_{OutputZero}} + 1}{\left(\frac{f \times j}{F_{OutputPole}} + 1\right) \times \left(\frac{f \times j}{F_{GatePole}} + 1\right)} \quad (12)$$

Where,

$$F_{OutputZero} = \frac{1}{2 \times \pi \times C_{out} \times ESR} \quad (13)$$

$$F_{OutputPole} = \frac{1}{2 \times \pi \times C_{out} \times \left(\frac{RL \times \frac{1}{gmFET}}{RL + \frac{1}{gmFET}} + ESR\right)} \quad (14)$$

$$F_{GatePole} = \frac{1}{2 \times \pi \times C_{GateDrain} \times Z_{Gate}} \quad (15)$$

$C_{GateDrain}$ is the gate to drain capacitance of the NMOS pass FET. Z_{Gate} is the impedance looking into the emitter of the drive transistor (Q1 in Figure 1) and is empirically determined to be 15 kΩ. RL is the load resistance. The worst case loop phase margin usually occurs at minimum load (maximum RL), where the output pole frequency is lowest. The transconductance (gmFET) of the pass transistor is sometimes known, but usually has to be approximated using Equation 16.

$$gmFET = \frac{2 \times I_{load}}{V_{gs} - V_t} \quad (16)$$

where I_{load} is the minimum load, V_{gs} is the gate source voltage at that load (which will have to read from

the FET datasheet or in some cases measured), and V_t is the threshold voltage of the FET. (See the design example section for a measured value of gmFET for the example circuit). As the load varies, the transconductance changes and thus the control loop changes. This is one reason why these models must be simulated and verified at several different load conditions. With this information, the gain of the voltage loop can be approximated by:

$$A_{Loop} = A_{output} \times A_{comp} \times A_{DC} \tag{17}$$

Setting the RC Timer

The UC3832 incorporates an RC timer (pin 14) that reduces the duty cycle applied to the pass transistor in the event of a gross over current event. The R sets the duty cycle of the gate drive during an over current condition and the C sets the time (period). To ensure that the UC3832 can start into the output capacitance and full load after an over current event, the timing cap must be sized sufficiently large:

$$C_t > \frac{C_{out} \times R_{L\text{-}Min}}{10\ k\Omega \times 0.693} \times \ln\left[\left(1 - \frac{V_{out}}{K_k \times I_{CurrentLimit\text{-}Min} \times R_{L\text{-}Min}}\right)^{-1}\right] \tag{18}$$

$R_{L\text{-}Min}$ is the minimum load resistance, corresponding to the maximum load current. The 10 kΩ resistor is internal to the UC3832 and K_k equals the worst case current sense amplifier offset (110 mV) divided by the worst case current sense comparator offset (107 mV). The applied on time is equal to $0.693 \times 10\ k\Omega \times C_t$ and the off time equals $0.693 \times R_t \times C_t$. Thus, the duty cycle applied to the pass transistor during a gross overcurrent condition equals:

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{10\ k\Omega}{10\ k\Omega + R_t} \tag{19}$$

200 kΩ is an acceptable value for R_t for most applications, yielding a duty cycle of the FET gate drive of roughly 5%.

Configuring the Vadj Pin

As shown in the data sheet (SLUS387), the current limit of the UC3832 is programmable with the voltage applied to the Vadj pin (pin 12). The higher this voltage, the lower the current limit. Figure 2 shows that an RC circuit can be added from the bias voltage to the Vadj pin to create a time varying current limit. In this particular circuit, once the bias voltage is applied (i. e. start up), the voltage on Vadj will start at 0V and slowly charge up to the bias voltage. Thus, the current limit will be highest at startup (to allow greater inrush currents) and lower during steady state operation. A diode can be added to reset this RC circuit in the case of a quick disconnect/reconnect of the bias voltage.

Design Example

This example design converts 1.5V to 1.2V at 10 A maximum load. This is a perfect application for a linear controller, as the voltage differential is low and the load current is high. With this input and output voltage, efficiency should be 80%. A higher voltage is also needed to provide a bias voltage for the UC3832's control circuitry and gate drive. Since the $R_{DS(on)}$ of a FET depends on the gate to source voltage, this bias needs to be high enough to drive the selected NMOS FET into saturation to achieve a low enough $R_{DS(on)}$ to satisfy Equation 4 and ensure the circuit does not dropout at high load currents. So, a 5V bias, found in most systems, is used.

Setting the Current Limit

The maximum design current is 10A. From Equation 1, R_{sense} should be 9.3 mΩ. So, a value of 9 mΩ is selected to give some margin in the current trip point. Assuming a 2% tolerance on the sense resistor and from Equation 2 and Equation 3, the maximum trip current is 12.1A and the minimum trip current is 10.1A.

A current sense filter (formed by C11 and R4 in Figure 2) is added to filter the current sense circuit from other noise sources in the system. Increasing the RC product decreases the frequency of the pole formed by R4 and C11. This is not needed for most applications but will increase the noise immunity of the current limit circuit.

Selecting a FET

From Equation 4, a FET with an $R_{DS(on)}$ of less than 30 mΩ is needed. The FET must also be able to carry 12.1A. From Equation 5, the FET must be able to dissipate 3.6W. The FET must do all of this with a gate to source voltage of only 5V-1.3V-0.7V-1.2V = 1.8V. Two Fairchild FDD3706's in parallel were chosen to meet these requirements.

Voltage Loop Compensation

Since the output voltage is lower than the reference, the voltage divider is attached between the reference (pin 4) and the positive terminal of the transconductance amplifier (pin 3). The output voltage is connected through a resistor to the negative terminal (pin 9) of the transconductance amplifier. Thus for Equation 6, $R_{bot} = \infty$ and $R_{top} = 0$, leaving the DC gain from the voltage divider (A_{DC}) equal to 1. G_{M-TA} is in the datasheet and is typically 4.3 mS, but was measured to be 0.64 mS on the chip used for this testing.

Using open loop gain values of 100 dB for the voltage amplifier and 80 dB for the current amplifier and transconductances of 0.64 mS for the voltage amplifier and 45 mS for the current amplifier, the Z_{out} (from using Equation 11 twice and then combining those impedances in parallel) was calculated to be 222 kΩ.

3 x 100 µF of ceramic output capacitors in parallel were used on the output. Their ESR was estimated to be 5 mΩ each. The minimum load (maximum RL) is 0.1A, for an RL_{max} of 12Ω. Using Equation 16, the transconductance of the pass FET (gmFET) was calculated to be 0.8 S. Since there are 2 FETs, the transconductance calculated from Equation 16 needs to be multiplied by a factor of 2. Thus, the output pole frequency ($F_{OutputPole}$ from Equation 14) at minimum load is at 891 Hz.

A zero must be placed near this frequency to cancel this pole and ensure a single pole roll-off at the crossover frequency. This zero can be either $F_{OutputZero}$ (from Equation 13) or $F_{CompZero}$ (from Equation 8).

For this design, the compensation zero was chosen to cancel the output pole. R_{comp} was chosen to be 12.1 kΩ and C_{comp} was chosen to be 0.015 µF, placing the zero at 877 Hz. The designer does have flexibility when choosing a value for R_{comp}. Larger values result in higher gain but less stability, while smaller values limit the gain of the loop and result in lower crossover frequencies. A value around 10 kΩ is a good starting point for R_{comp}.

C_{pole} is used to ensure that the loop rolls off above the crossover frequency or to compensate for the output capacitor zero ($F_{OutputZero}$).

For this design, the output capacitance's ESR is so low that the $F_{OutputZero}$ is high enough (calculated to be above 300 kHz) to not need to compensate. So, C_{Pole} is left open. But for tantalum or aluminum electrolytic capacitors with higher ESR's, this is usually not the case. Approximately 15 pF of stray capacitance is present at that node (where C_{pole} would be) and so there is a pole formed, from Equation 9, at around 878 kHz.

The FET's gate pole ($F_{GatePole}$ from Equation 15) is calculated to be at 26 kHz. Note that with 2 FETs in parallel, the gate to drain capacitance ($C_{GateDrain}$) needs to be multiplied by 2 and comes out to be 402 pF total.

Setting the RC Timer

From Equation 18 and an $R_{L\text{-}Min}$ of $\frac{1.2\ V}{10\ A} = 0.12\ \Omega$, C_t is chosen to be 0.022 µF and R_t is chosen to be 200 kΩ.

Measured Results

Schematic

Based on the above design calculations, the following circuit was built:

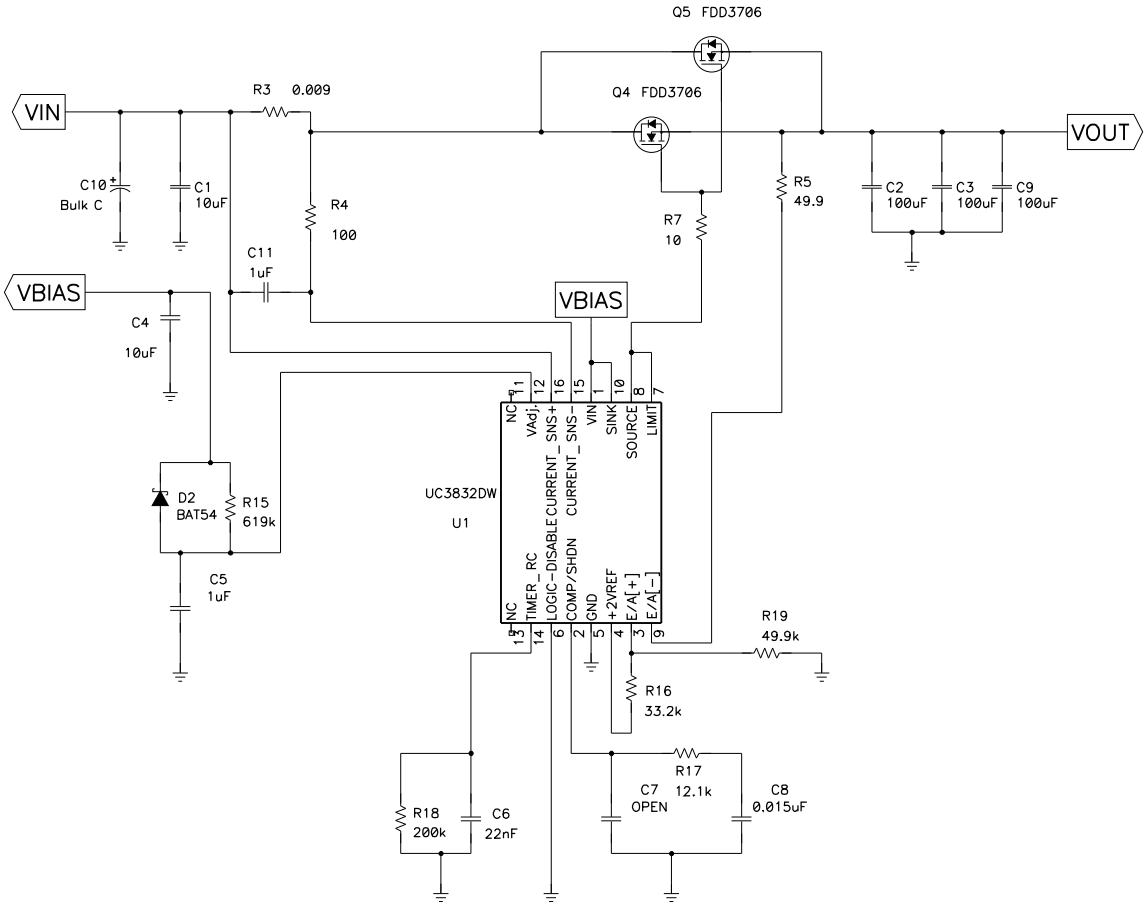

Figure 2. Schematic of the UC3832 Circuit Used for Testing

Voltage Loop Measurements

Since the frequency of the output pole varies with load, Bode plots were taken at minimum and maximum loads to verify the stability of the system over the entire load range:

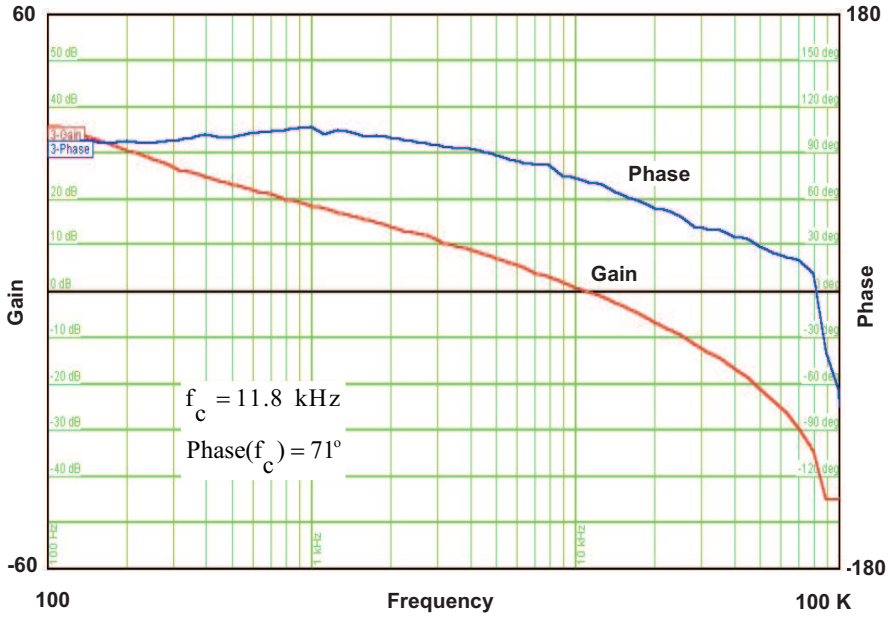

Figure 3. Bode Plot of the Circuit in Figure 2 at 0.1 A Load

In Figure 3, since the compensation zero was placed at 877 Hz and the output pole is at 891 Hz, the two effectively cancel as they were designed to do. Thus, the single pole roll-off at the crossover frequency.

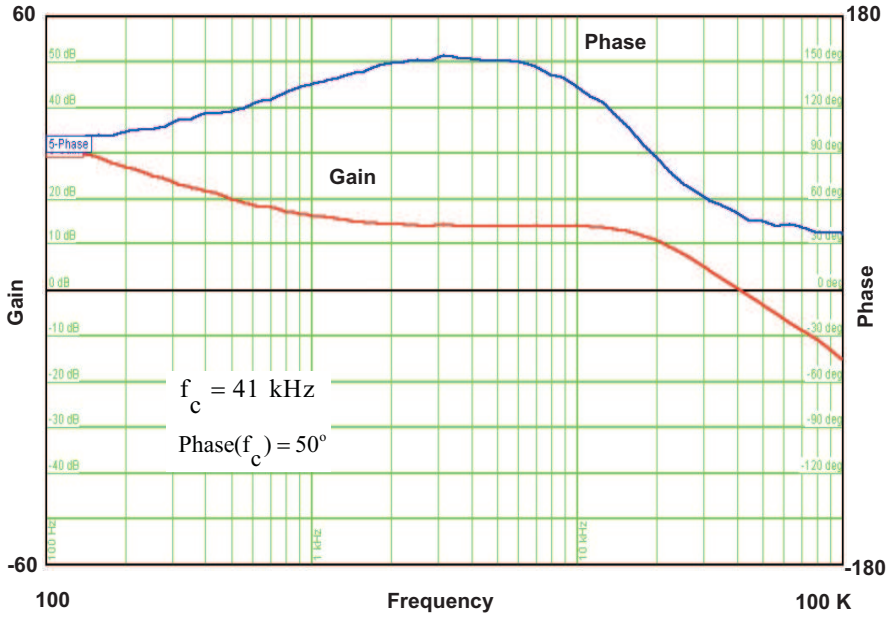

Figure 4. Bode Plot of the Circuit in Figure 2 at 10 A Load

In Figure 4, taken at 10A load, the output pole is calculated to be pushed out to 33 kHz, while the compensation zero remains at 891 Hz. Thus, the gain levels off beginning at around 1 kHz due to the zero, while the gain goes down again at around 20 kHz, due to the dual effect of the output pole and FET gate pole (at 26 kHz).

Both of these plots (and several taken at intermediate load conditions) show phase margins of greater than 45°. This indicates stability.

Load Transient Response

The stability of the circuit can be further validated by observing the nature of the output voltage deviation when subjected to a load step.

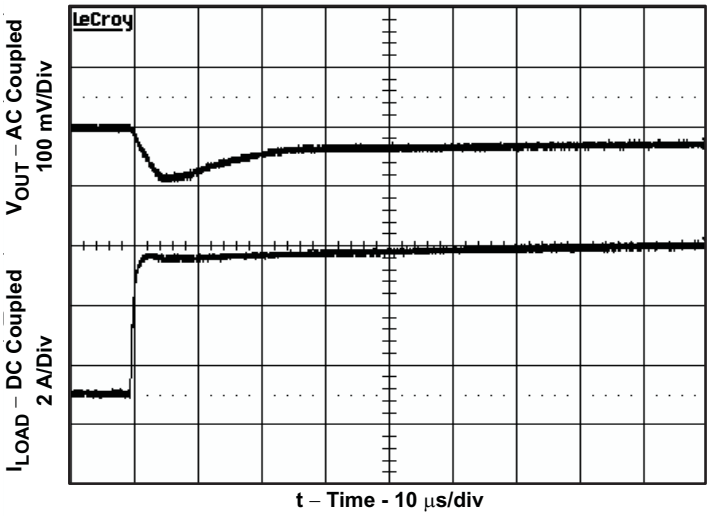

Figure 5. 1A to 6A Load Step of the Circuit in Figure 2

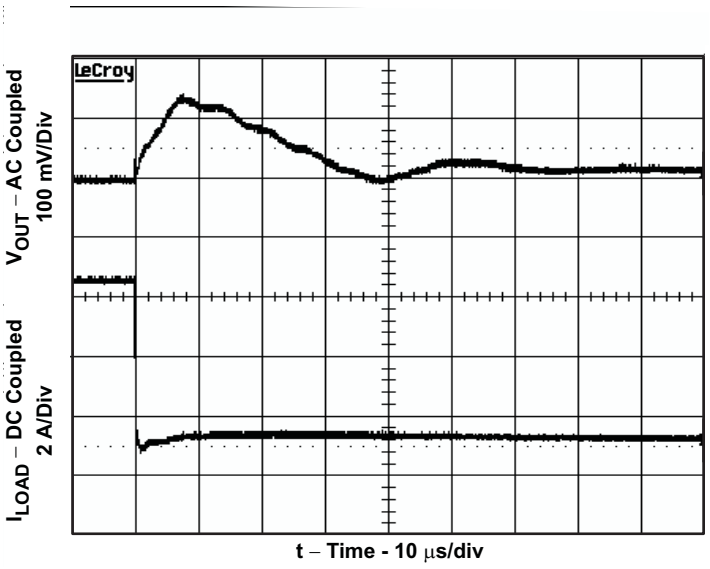

Figure 6. 6A to 1A Load Step of the Circuit in Figure 2

Since there is no ringing on the turn on step, and since there are less than 4 rings on the turn off step, the circuit is sufficiently damped.

Conclusion

This application note has detailed the design of a linear power supply using the UC3832 family of linear controllers. Design equations have been given for the critical pieces of the circuit and a design example has shown the UC3832 in a practical application.

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