Application Note

Understanding Output Voltage Ripple in DCM Operation of D-CAP Buck Converters

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ABSTRACT

Output voltage ripple is a key parameter for buck converter, which can make great impact on system application and should be paid more attention on. The principle for generation of output voltage ripple for buck converter in CCM operation is well illustrated in many text books and application notes. However, when focusing on the output voltage ripple in DCM operation, not many detailed description on it. This application note can introduce a method for estimating output voltage ripple in DCM operation for buck converter with D-CAP, D-CAP2 and D-CAP3 mode. Results of bench tests can be given based on TPS56837. Error analysis is also included to illustrate what kind of factors can affect test results. In the conclusion of this paper, a comparison between output voltage ripple in DCM operation and CCM operation in D-CAP buck converters can be made.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Review of CCM Output Voltage Ripple in Buck Converter

Output voltage ripple is a key parameter for buck converter, which could make great impact on system application and should be paid more attention on. The principle for generation of output voltage ripple for buck converter is well illustrated in many text books and application notes. A brief review of CCM output voltage ripple in buck converter will be given first.

For CCM operation, inductor current increases from its valley value at the beginning of switch cycle, reaching its peak value when high-side FET is OFF and going back to its valley value when the switch cycle is finished. The average inductor current is loading current.

When only considering impacts of output capacitors, output voltage ripple is raised by charging and discharging process of output capacitors. Excessive energy marked with Q1 in Figure 1-1 will be charged to C_{OUT}, leading to the rise of voltage on C_{OUT}. When the inductor current is lower than loading current, C_{OUT} will discharge to maintain V_{OUT} stable. So output voltage ripple will be calculated by Equation 1 and Equation 2.

$$Q1 = \frac{\Delta IL \times T_{SW}}{8} \tag{1}$$

$$\Delta V_{OUT} = \frac{Q_1}{C_{OUT}} = \frac{\Delta IL \times T_{SW}}{8 \times C_{OUT}} \tag{2}$$

Q1: Excessive energy

T_{SW}: Switching period

ΔV_{OUT}: Output voltage ripple

C_{OUT}: Value of output capacitors

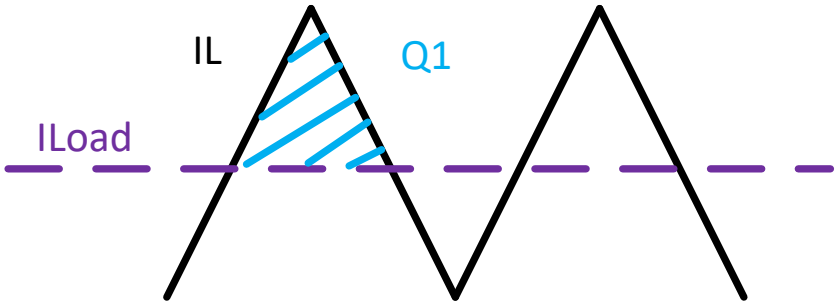

Figure 1-1. Inductor Current Illustration for CCM Operation

2 Calculation of DCM Output Voltage Ripple in D-CAP Buck Converter

However, method of CCM output voltage ripple calculation is not designed for DCM operation. So it is necessary to know behavior in DCM operation first.

DCM operation is widely used in ECO-mode buck converters, which is an operation mode for having high efficiency in light loading operation. When inductor current decreases to 0A, high-side FET and low-side FET will be OFF. The converter will enter working period called *Idle time*, when No FET will be conducted during Idle time and output voltage keeps decreasing. This is quite different with CCM operation in buck converter. For D-CAP converter, when Vout drops to the level that V_{FB}-V_{REF}=0, internal on-timer will work and make high side MOSFET conduct for constant on-time, starting the next switch cycle. D-CAP2 and D-CAP3 control works similarly with D-CAP but equipped with internal ripple injection network, making converters easy to be used. For more details about D-CAP control mode, please refer to following application note: D-CAP Mode With All-Ceramic Output Capacitor Application.

Due to the existence of Idle time, there can be period that inductor current becomes zero, meaning the formula used for calculating output voltage ripple in DCM operation can be different with that in CCM operation. The following part will introduce method for calculating output voltage ripple in DCM operation.

When mainly considering the effects of output capacitors, the key item for calculating output voltage ripple in DCM operation is the same with CCM operation: finding charged electric in output capacitors.

A typical DCM operation is used as analyzed case, whose inductor operation illustration is shown in Figure 2-1. And during following analysis, only capacitive output voltage ripple is taken into consideration.

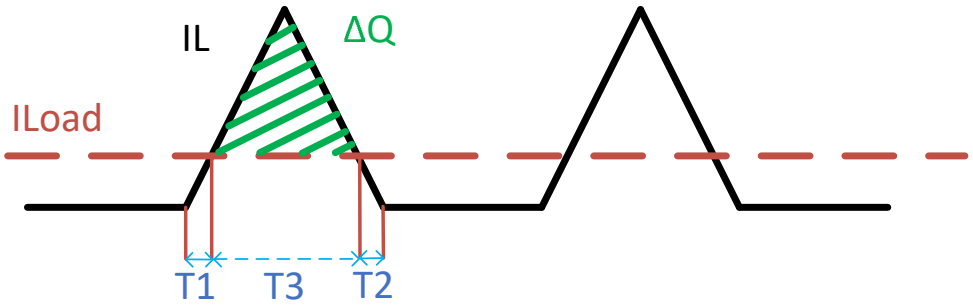

Figure 2-1. Inductor Current Illustration for DCM Operation

One critical item can be highlighted before analysis is time period for one pulse, or called switching period, which represents period that high-side FET on time plus low-side FET on time (ignoring deadtime in rising and falling edge). For D-CAP control, on time for high-side FET is fixed with rising and falling slew rate of inductor current once Vin and Vout are fixed, meaning the inductor peak current and on time for low-side FET is fixed whatever in DCM operation or CCM operation. So time period for one pulse is fixed both in CCM and DCM operation, which will be represented by in following description.

In Figure 2-1, brown line represents loading current ILoad. For the period when inductor current exceeding ILoad, excessive charge ΔQ will pour into output capacitors, leading to output voltage ripple.

ΔQ is the integration of time and inductor current when inductor current exceeds ILoad, which is the area of marked green shadowed triangle in Figure 2-1. The height and width of bottom edge in green shadowed triangle can be achieved in order to acquire the value of its area, which is ΔQ. The height is easily to be achieved by following equation: Height = IL_{PEAK} – ILoad, while IL_{PEAK} is the peak value of inductor current. In DCM operation, since inductor increases from 0 to its peak value, so IL_{PEAK} equals to ΔIL in DCM operation.Equation 3 is used to get ΔQ.

$$\Delta Q = 0.5 \times (\Delta IL - ILoad) \times T3 \quad (3)$$

The bottom edge of triangle is time period marked with T3. For D-CAP control, when Vin and Vout are fixed, on-time of high-side FET and on-time of low-side FET are fixed, whatever CCM or DCM operation. So the sum of T1, T2 and T3 equals to the switching period of normal CCM operation. Rising slew rate and falling slew rate of inductor current are fixed as well, meaning T1 can be achieved with dividing inductor rising slew rate by ILoad

as shown in Equation 4. T2 can be calculated using same method with T1 calculation, which is illustrated in Equation 5. After getting T1 and T2, Equation 6 can be used to achieve T3.

$$T1 = \frac{ILoad}{SR\_rising} = \frac{ILoad \times L}{V_{IN} - V_{OUT}} \tag{4}$$

$$T2 = \frac{ILoad}{SR\_falling} = \frac{ILoad \times L}{V_{OUT}} \tag{5}$$

$$T3 = T_{SW} - T1 - T2 = T_{SW} - \frac{ILoad \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})} = \frac{1}{F_{SW}} - \frac{ILoad \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})} \tag{6}$$

So ΔQ can be calculated by using Equation 7:

$$\Delta Q = 0.5 \times \left(\frac{V_{OUT} \times (1 - D)}{L \times F_{SW}} - ILoad\right) \times \left(\frac{1}{F_{SW}} - \frac{ILoad \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})}\right) \tag{7}$$

Where D is duty cycle of buck converter, F_{SW} is switching frequency in CCM operation.

Once getting value of ΔQ, the output voltage ripple ΔV_{OUT} can be calculated by Equation 8:

$$\Delta V_{OUT} = \frac{\Delta Q}{C_{OUT}} = \frac{0.5}{C_{OUT}} \times \left(\frac{V_{OUT} \times (1 - D)}{L \times F_{SW}} - ILoad\right) \times \left(\frac{1}{F_{SW}} - \frac{ILoad \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})}\right) \tag{8}$$

Please be aware that above analysis only consider capacitive ripple. If ESR is also included in calculation of output voltage ripple, Equation 9 can be implemented:

$$\Delta V_{OUT} = \frac{0.5}{C_{OUT}} \times \left(\frac{V_{OUT} \times (1 - D)}{L \times F_{SW}} - ILoad\right) \times \left(\frac{1}{F_{SW}} - \frac{ILoad \times L \times V_{IN}}{V_{OUT} \times (V_{IN} - V_{OUT})}\right) + ESR \times \left(\frac{V_{OUT} \times (1 - D)}{L \times F_{SW}} - ILoad\right) \tag{9}$$

It can be emphasized that effective value of C_{OUT} needs to be used in calculation, meaning DC bias effect is needed to be considered. Above method for calculating ΔV_{OUT} in DCM operation is designed not only for D-CAP parts, but also for D-CAP2 and D-CAP3 parts.

3 Bench Test Results and Error Analysis

3.1 Bench Test Results

TPS56837 is selected for bench tests. The TPS56837 is a high-efficiency, easy-to-use, synchronous buck converter with a wide input voltage range of 4.5-V to 28-V, and supports up to 8-A continuous output current at output voltages between 0.6-V and 13-V. This switch mode power supply (SMPS) IC is optimized for applications requiring very low power consumption, such as printers, DTV, monitor and some industrial applications, by providing an Eco-mode (pulse-skipping).

Bench tests are conducted on the TPS56837EVM. For details, see the *TPS56837EVM Evaluation Module User's Guide*. The bench test setup and configuration is listed in Table 3-1.

Table 3-1. Bench Setup for TPS56837

V_{IN}(V)	V_{OUT}(V)	L (µH)	Cout (µF)	CFF (pF) / C15	RFF (kΩ) / R14	Rtop (kΩ) / R9	Rbot (kΩ) / R8	Mode
24	5	3.3	2 × 22 µF (1210, 25V)	150	0	73.2	10	PSM / 500 kHz

Results are summarized in Table 3-2. All tests are conducted with 24Vin to 5Vout with 500kHz setting. Loading is changed from 0A to 0.8A. DC bias effect is considered and effective value of C_{OUT} is used in calculation. Equation 9 is used for calculation and 7 comparisons are conducted between calculated value, bench test value and Webench simulated value.

Table 3-2. DCM V_{OUT} Ripple Comparisons

V_{IN}(V)	V_{OUT}(V)	I_{OUT}(A)	Calculated ΔV_{OUT}(mV)	Tested ΔV_{OUT}(mV)
24	5	0	65.38	64.4
24	5	0.1	60.14	58.8
24	5	0.2	55.11	51.6
24	5	0.3	50.31	46.0
24	5	0.4	45.73	40
24	5	0.6	37.22	30.8
24	5	0.8	29.58	23.4

It is clear from the table that calculations do not have much error compared with bench test results, meaning it can be used for estimating output voltage ripple in DCM operation of D-CAP parts. For Webench simulation, simulated results do show not much deviation in most of loading conditions and can be used for design reference.

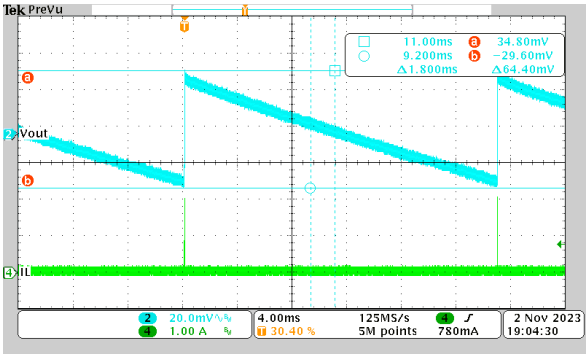

Figure 3-1. V_{OUT} Ripple Under I_{OUT}= 0A

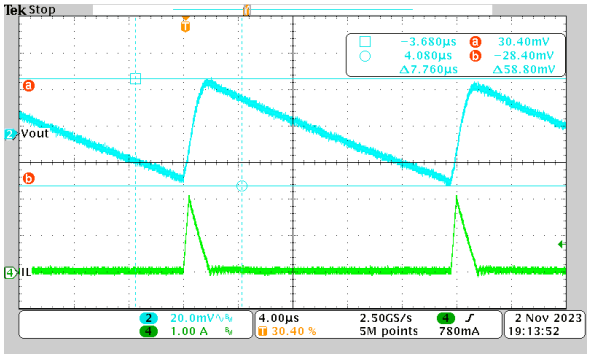

Figure 3-2. V_{OUT} Ripple Under I_{OUT}= 0.1A

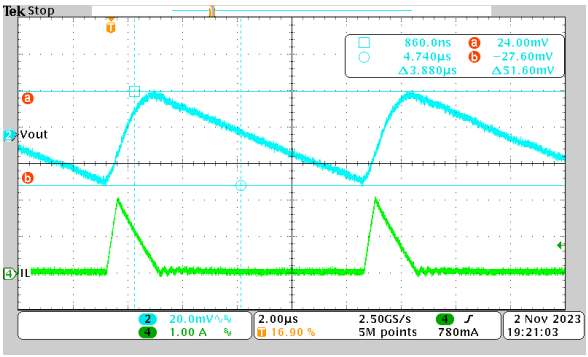

Figure 3-3. V_{OUT} Ripple Under I_{OUT}= 0.2A

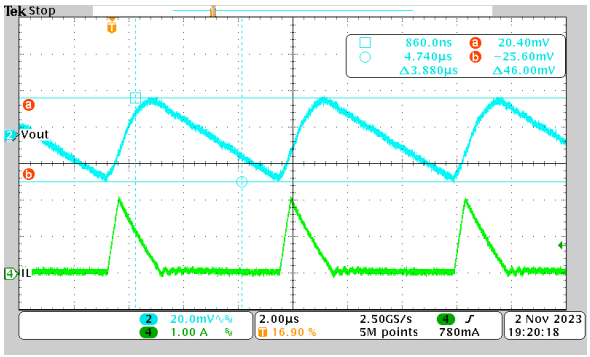

Figure 3-4. V_{OUT} Ripple Under I_{OUT} = 0.3A

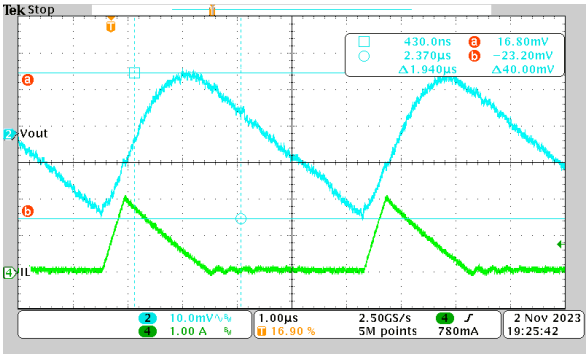

Figure 3-5. V_{OUT} Ripple Under I_{OUT} = 0.4A

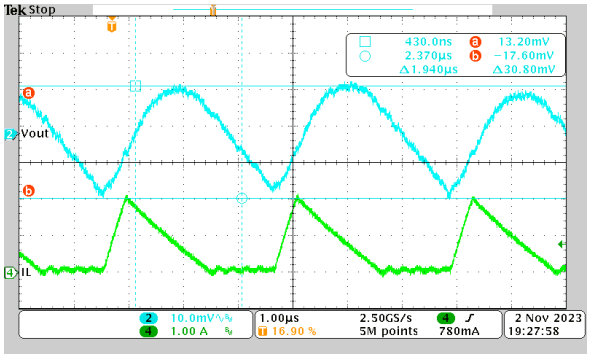

Figure 3-6. V_{OUT} Ripple Under I_{OUT} = 0.6A

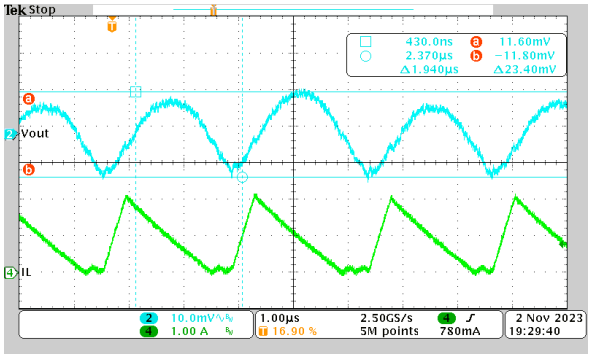

Figure 3-7. V_{OUT} Ripple Under I_{OUT} = 0.8A

3.2 Error Analysis

Although calculations have good match with bench test results, there is still error existed. Reasons for the existence of error can be analyzed and other factors that could raise error can be given.

3.2.1 Variation in High-Side FET on Time

Table 3-1 shows that bench test results are smaller than calculated results. The factor can make such impact is high-side FET on time. Although it is fixed once Vin and Vout are fixed in D-CAP control, non-ideal characteristic of internal circuit can make it match with calculation not precisely. Varied high side FET on time can make inductor current rise to different peak value than estimated, resulting in different output voltage ripple as well.

Figure 3-8 shows real high-side FET on time in test. Calculated high-side FET on time is about 417ns, while real test shows 410ns. Such shrink in high-side FET on time can make output voltage ripple smaller than calculated value, which matches the trend shown in Table 3-1.

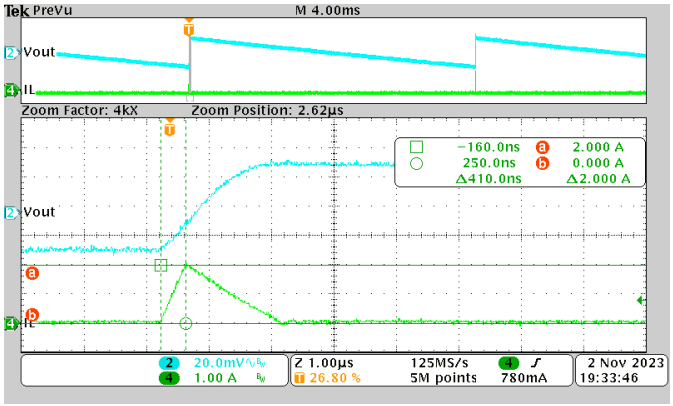

Figure 3-8. Real High-Side FET on Time in Test Under 0A Loading

3.2.2 Variation in Component Value

There would be other factors needed to consider in application. Since used components are not ideal components, there would exist deviation in their mass production

Used C_{OUT} in bench test is default capacitor assembled on EVM, whose part number is GRM32ER71E226KE15L. Based on its specification, its typical value has ±10% variation in mass production. Capacitance has ±15% change rate when only working temperature changes.

Aside from output capacitors, the inductance value also has variation due to non-ideal characteristic. Used inductor is also EVM default one, whose part number is 744325330. The inductor has ±20% variation on its inductance, which could lead to different peak value of inductor current and output voltage ripple.

All of previous mentioned variation can result in mismatch of calculated output voltage ripple and tested output voltage ripple.

4 Comparison Between DCM and CCM Output Voltage Ripple in D-CAP Buck Converter

The comparison between DCM ripple and CCM ripple is often mentioned. From bench test results, DCM ripple is higher than CCM ripple but few materials give fundamental analysis on it. This section will analyze why DCM ripple is higher than CCM ripple in D-CAP buck converter.

Figure 4-1 illustrates inductor current in DCM operation and CCM operation. Based on above analysis of DCM ripple calculation, excessive charge flowing into output capacitor, which is area of shadow marked triangle, determines the value of output voltage ripple.

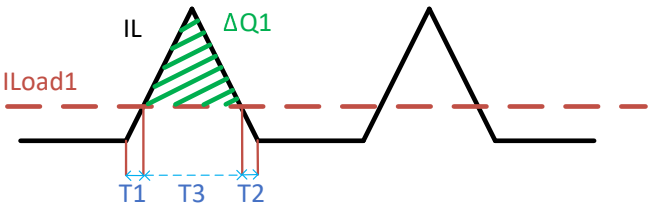

Figure 4-1. Inductor Current Illustration for DCM Operation

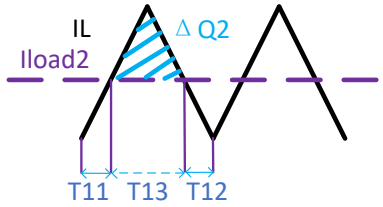

Figure 4-2. Inductor Current Illustration for CCM Operation

Time period for one pulse (T1+T2+T3 and T11+T12+T13, shown in Figure 4-1 and Figure 4-1) is same in CCM and DCM operation, which is show in Equation 10.

$$T_{SW} = T1 + T2 + T3 = T11 + T12 + T13 \quad (10)$$

Meanwhile, inductor rising slew rate and falling slew rate are same in CCM and DCM operation, meaning the ΔIL is same as well. For CCM operation, excessive charge is ΔQ2, which is achieved by using Equation 12,and its loading ILoad2 equals to 0.5ΔIL. While for DCM operation, excessive charge is ΔQ1 and it could be calculated by Equation 11.

$$\Delta Q1 = 0.5 \times (\Delta IL - ILoad1) \times T3 \quad (11)$$

$$\Delta Q2 = 0.5 \times ILoad2 \times T3 \quad (12)$$

For DCAP control, converter enters DCM operation once loading is lower than 0.5ΔIL, so ΔIL-ILoad1 > 0.5 ΔIL, leading to ΔIL-ILoad1 > ILoad2.

Based on calculations mentioned in previous section, since ILoad2 is higher than ILoad1, the rising time and falling time of ILoad2 is higher than that of ILoad1, leading to following comparison results:

$$T11 + T12 > T1 + T2 \quad (13)$$

$$T_{SW} - (T1 + T2) > T_{SW} - (T11 + T12) \quad (14)$$

$$T3 > T13 \quad (15)$$

From previous analysis, it is clear that ΔQ1 > ΔQ2, meaning more energy is charged to Cout in DCM operation. So DCM output voltage ripple is higher that in CCM operation in D-CAP buck converter.

5 Summary

In conclusion, this application note introduces method to estimate output voltage ripple in DCM operation for D-CAP control mode device. Error analysis is conducted to show elements that could affect correlation. In the end, comparison between output voltage ripple in DCM operation and CCM operation is conducted as well as fundamental analysis, giving theoretical proof that DCM V_{OUT} ripple is higher than CCM Vout ripple in D-CAP buck converters.

To emphasize, this article is not only designed for D-CAP buck converter, but also designed for D-CAP2 and D-CAP3 buck converter.

6 References

1. Texas Instruments, *TPS56837 4.5-V to 28-V Input, 8-A Synchronous Buck Converter*, data sheet.
2. Texas Instruments, *D-CAP Mode With All-Ceramic Output Capacitor Application*, application note.
3. Texas Instruments, *TPS56837 Buck Converter Evaluation Module*, user's guide.

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