Photo Flash Capacitor Charger Design With TPS65573

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ABSTRACT

The TPS65573 offers a complete solution for a charging photo flash capacitor and flashing xenon tube with an insulated gate bipolar transfer (IGBT) driver. This device has an integrated voltage reference, power switch (SW), comparators for peak current detection/power SW turn on detection/charge complete detection, an IGBT driver, and control logics for charging applications/driving IGBT applications.

Compared with discrete solutions, this device reduces the component count, shrinks the total solution size, and erases the difficulty of design for xenon-tube applications.

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1 Introduction

The TPS65573 offers a complete solution for a charging photo flash capacitor and flashing xenon tube with an insulated gate bipolar transfer (IGBT) driver. This device has an integrated voltage reference, power switch (SW), comparators for peak current detection/power SW turn on detection/charge complete detection, an IGBT driver, and control logics for charging applications/driving IGBT applications. Compared with discrete solutions, this device reduces the component count, shrinks the total solution size, and erases the difficulty of design for xenon-tube applications.

Additional advantages are a fast charging time and high efficiency because this device is optimized pulse-width modulation (PWM) control algorithm for photo flash capacitor charging. Also this device has high accuracy of detecting peak current at primary side and high accuracy of detecting charge completion. It achieves to reduce the distribution of charging time.

Other provisions of the device includes sensing the output voltage at primary side, programmable peak current at primary side, protection features (thermal shutdown and overcurrent), an output terminal for Charge completion detection and input pins for charge enable, flash acceptable and flash on.

- The peak current at the primary side can easily be programmed. The peak current can be set from IPEAK1 to IPEAK3 by using the I_PEAK terminal of the TPS65573 as shown in Figure 8. These values (IPEAK1 and IPEAK3) are specified in product datasheet.
- The target output voltage is set by the turn ratio of transformer. The TPS65573 stops charging when the voltage at photo flash capacitor achieves the target voltage. The TPS65573 can detect it at primary side of the transformer via transformer.
- VFULL, which is the target voltage on the primary side, is specified in product datasheet.
- The TPS65573 has two protection features (thermal shutdown and overcurrent).

The TPS65573 is particularly well-suited for portable device applications like digital still cameras (DSC), digital video cameras (DVC), optical film cameras, mobile camera phones and PDAs with cameras. The typical application circuit is shown in Figure 1.

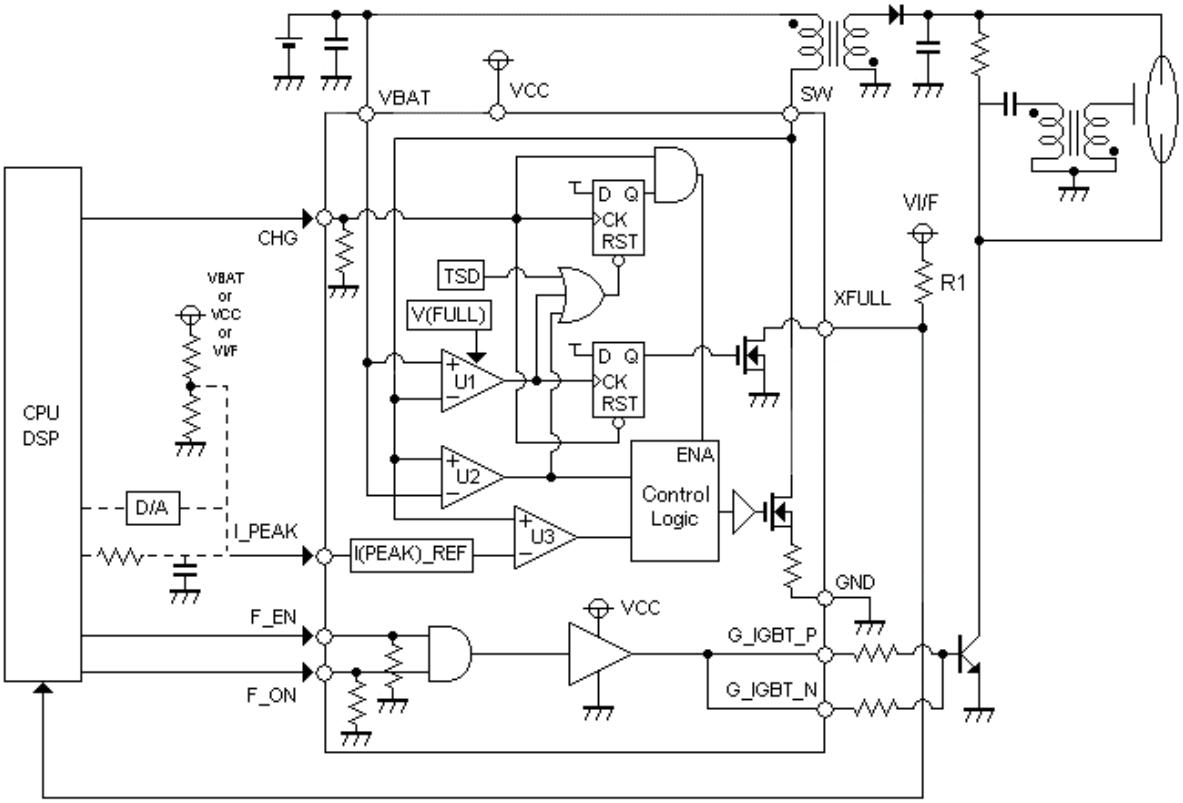

Figure 1. Typical Application Circuit

2 Basic Operation

2.1 How to Start and Stop Charging

TPS65573 has an enable/disable terminal for charging, named CHG. The only way to start charging is to input high level signal into CHG terminal (see Time A and Time C in Figure 3). This high level signal is latched by internal D-FF shown in Figure 2. Internal ENA signal goes up with some delay shown in Figure 4 to avoid malfunction with pulsed noise at CHG terminal.

To stop charging, there are three trigger events:

1. Forced stop by inputting low level at CHG (see Time B in Figure 3).
2. Automatic stop by detecting full charge; VOUT achieves the target value (see Time D in Figure 3).
3. Protected stop by detecting the condition of overcurrent (OCP) on the SW terminal or thermal shutdown (TSD).

It is acceptable to start re-charging after a forced stop controlled by CHG terminal (see Time C in Figure 3).

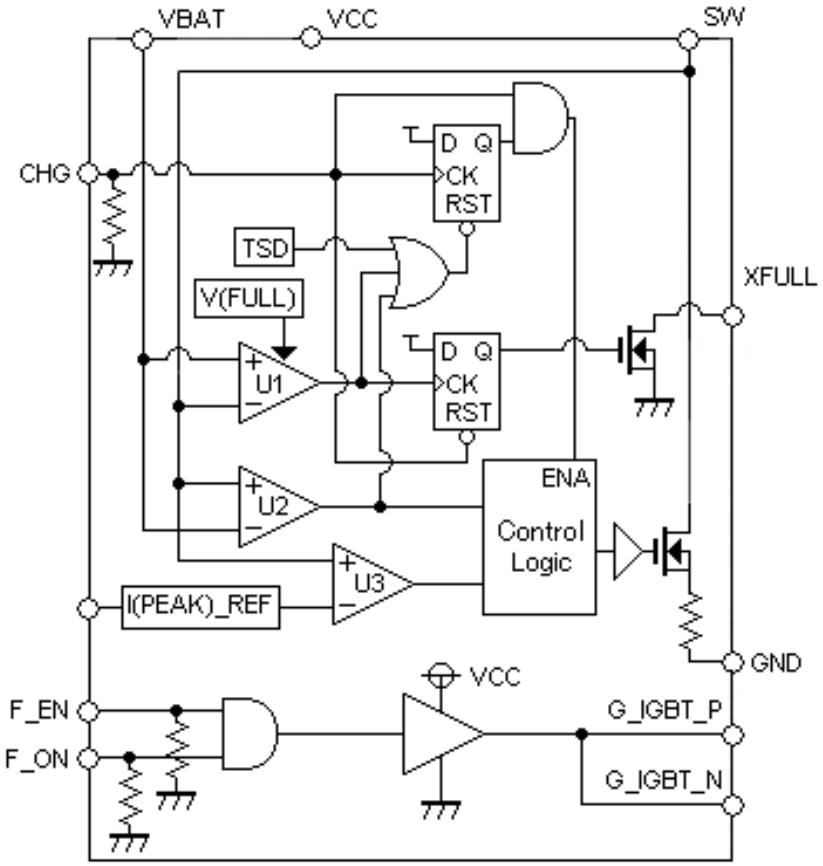

Figure 2. Block Diagram

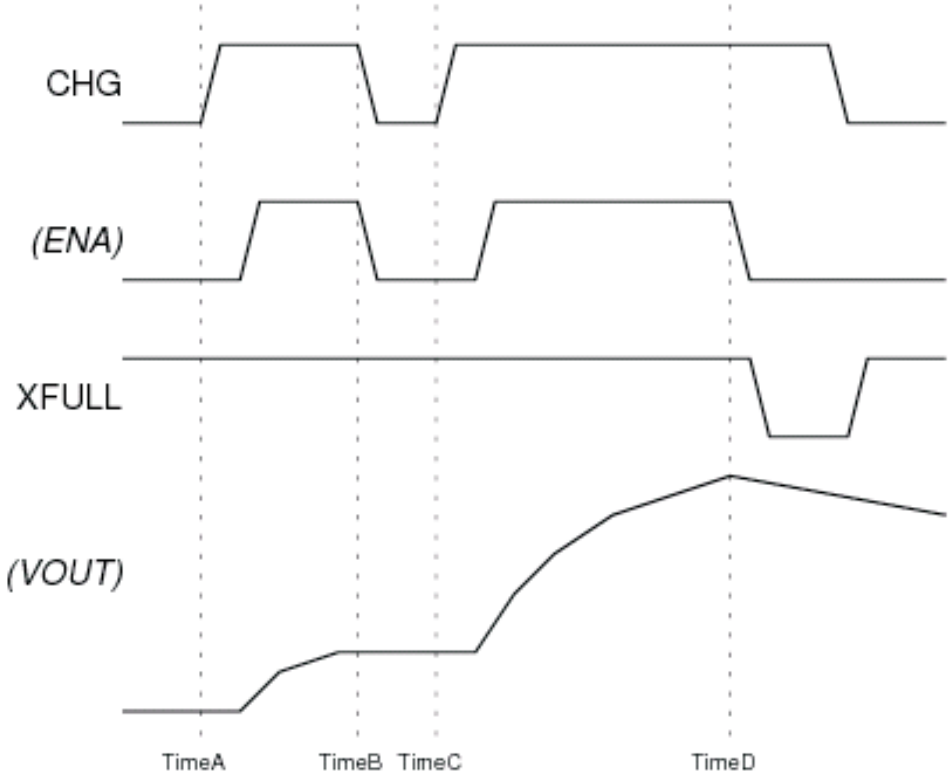

Figure 3. Sequence for Charging

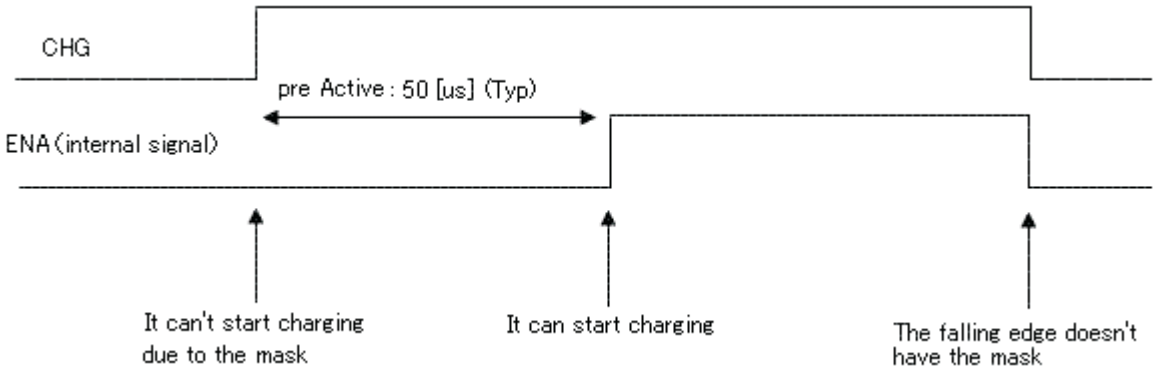

Figure 4. CHG Delay Time at Starting Charge Operation

2.2 Principle of Charge Operation

The TPS65573 application circuit is based on a flyback power supply topology and the charge operation is controlled by the external signal inputted from CHG terminal and the protections.

When the signal of CHG terminal is high, the charge operation is started with some delay shown in Figure 4. At first, the internal FET switch turns on and the current at SW terminal goes up. When the current achieves the target current defined by the voltage at I_PEAK terminal, the internal FET switch turns off and the voltage at SW terminal goes up due to kick-back voltage at the transformer. When the internal FET switch is on, the inductance at the primary side of the transformer stores energy which depends on the current at the primary side of the transformer.

When the internal FET switch turns off, the stored energy is transferred to the secondary side of the transformer. At that moment, the current flows in the secondary side from secondary side of the transformer to the photo flash capacitor via the fast recovery diode (FRD) as shown in Figure 1.

The TPS65573 uses three comparators, U1, U2, and U3 in Figure 1 and Figure 2 to determine the state of the internal FET switch. Below are the descriptions for these comparators.

- U1 (VFULL comparator): Detects charge completion
- U2 (V_{ZERO} comparator): Detects the turning ON timing
- U3 (I_PEAK comparator): Detects the turning OFF timing

While internal FET switch is on, U3 monitors I_{SW} which is the current flowing through the SW terminal to PGND. When ISW exceeds the target current defined by the voltage of I_PEAK terminal, internal FET switch turns OFF. At the same time, U2 monitors the voltage difference between SW terminal and VBAT terminal for OCP. When U2 detect more than 100-mV (TYP) difference, the TPS65573 disables all functions.

When the internal FET switch turns OFF, the energy at the primary of the transformer is transferred to the secondary side. Meanwhile, U2 monitors the kickback voltage at the SW terminal. As the energy is discharging, the kickback voltage is increasing according to the increase of V_{OUT}. When most all of the energy is transferred from primary side to secondary side, the system cannot continue rectification via the diode, and the current at secondary side goes to zero. After rectification stops, the small amount of energy left in the transformer is released via parasitic paths, and the kickback voltage reaches zero. In the actual circuit, this period does not appear due to the small amount of energy left. During this period, U2 makes the internal FET switch turn ON when (V_{SW} - V_{BAT}) is smaller than the threshold named V_{ZERO} specified in product datasheet.

The ON time of internal FET switch depends on the target current defined by the voltage of I_PEAK terminal. The ON time is calculated by Equation 1. The reverse recovery time (Trr) of FRD placed on the secondary side is not a constant value because the reverse recovery time depends on ambient temperature, forward current and the voltage difference of the FRD between Anode and Cathode. Section 3.3.1 discusses this influence in detail.

$$T_{ON(n)} = L_P \frac{I_PEAK}{V_{BAT}} + Trr(n) \quad (1)$$

Where:

- $T_{ON(n)}$ - ON time at n cycle switching
- L_P - Primary inductance
- I_PEAK - Peak current at primary side
- V_{BAT} - Battery voltage
- Trr(n) - Reverse recovery time at n cycle switching

On the other hand, the OFF time depends on the voltage at photo flash capacitor because the voltage at secondary side depends on it via FRD. The OFF time at each cycle is calculated by Equation 2.

$$T_{OFF(n)} = N \bullet L_P \frac{I_PEAK}{V_{OUT(n)}} \quad (2)$$

Where:

- $T_{OFF(n)}$ - OFF time at n cycle switching
- N - Turn ratio of transformer
- $V_{OUT(n)}$ - Voltage at the photo flash capacitor during n cycle switching

When U1 detects the target voltage at primary side, the TPS65573 stop charging operation. At that time, the voltage at photo flash capacitor is calculated by Equation 3.

$$V_{OUT} = N \bullet V_{FULL} + V_f \quad (3)$$

Where:

- V_{OUT} - Volage at the photo flash capacitor at charge completion
- N - Turn ratio of transformer
- V_{FULL} - Charge completion voltage (specified by product data sheet)
- V_f - Forward voltage of FRD

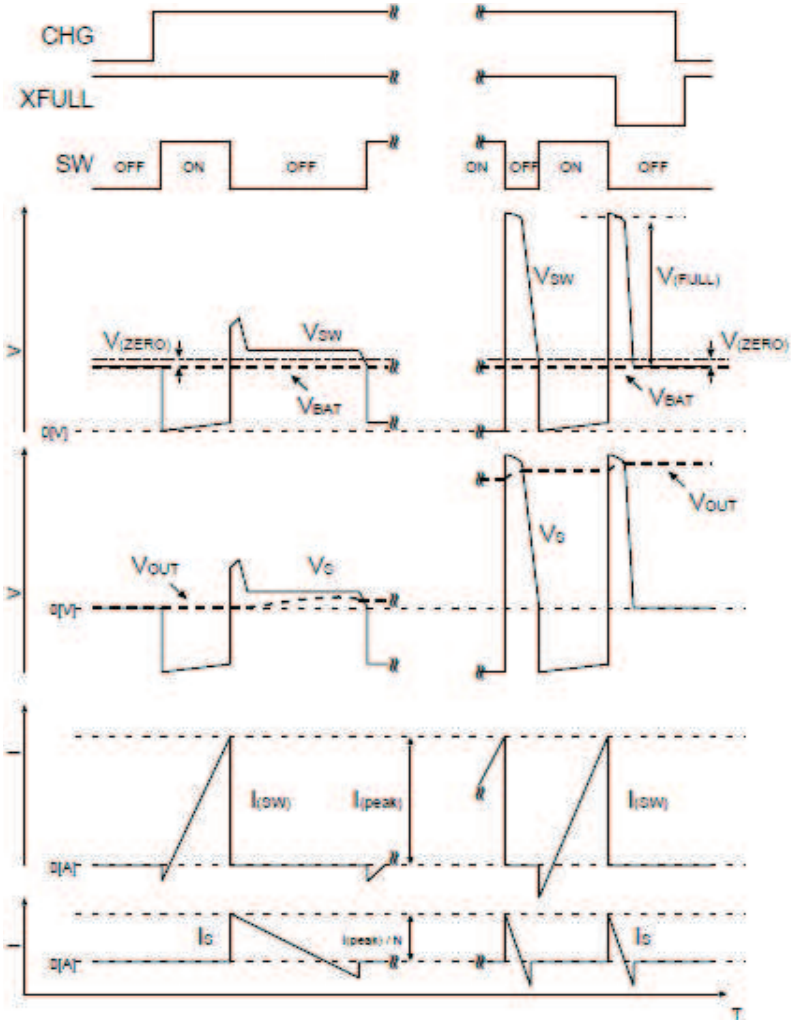

Figure 5. Timing Diagram at Beginning/End

2.3 Principle of Flash Operation

The TPS65573 integrates IGBT driver for flashing the xenon tube. After charge completion, the xenon tube is able to turn ON with IGBT driver. If the earlier flashing should be needed before charge completion, it should need to confirm the lowest allowable flashing voltage applying to the xenon tube.

It is recommended that G_IGBT_P and G_IGBT_N terminals are connected to the gate of IGBT as close as possible to avoid the miss-operation of flashing or broken the gate of IGBT. The output voltage of G_IGBT_P and G_IGBT_N terminals voltage depends on VCC. The rise time of G_IGBT_P terminal and fall time of G_IGBT_N terminal are almost same because the TPS65573 doesn't include pull-up/pull-down resistors to adjust them. The rise time and fall time must be satisfied with the value specified in the datasheet of IGBT to avoid breaking the IGBT.

This IGBT drive has two logic inputs, one is flash acceptable (F_EN) and the other is flash enable (F_ON). To turn on the xenon tube, high-level signal should be inputted into both F_EN and F_ON. It is acceptable to connect both F_EN and F_ON if simple control is preferable.

2.4 Protections

The TPS65563A has two protection mechanisms; thermal shutdown (TSD) and over current protection (OCP).

2.4.1 Thermal Shutdown (TSD)

Once the TPS65573 die temperature reaches the specific temperature, the operation is immediately latched off. To recover the operation, TPS65573 die temperature should be lower than specific temperature and forced to a low level at CHG terminal after protection occurred.

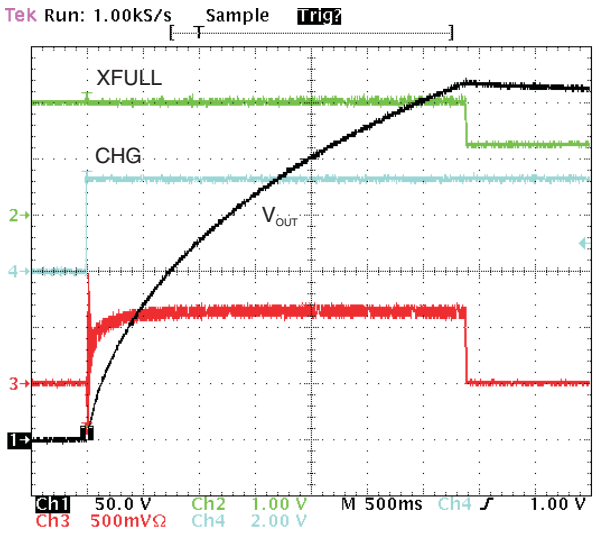

Figure 6. Waveform at Normal Operation

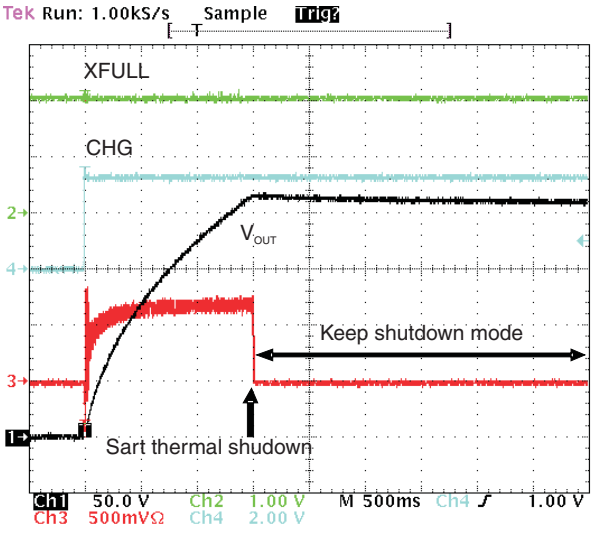

Figure 7. Waveform at Thermal Shutdown

2.4.2 Over Current Protection (OCP)

The TPS65573 have OCP at SW terminal. The TPS65573 is latched off if SW pin is dropped to compare VBAT pin voltage during the switch ON time. The threshold is specified in “Over Current protection trigger Voltage at SW” in ELECTRICAL CHARACTERISTICS. To recover the operation, CHG level is forced to a low level after protection occurred and peak current is less than threshold.

3 How to Design the System With TPS65573

3.1 Peak Current Definition

The TPS65573 provides a method to program the peak current at primary side with a voltage applied to the I_PEAK terminal. Figure 8 shows the relationship between the voltage of I_PEAK terminal and the peak current at primary side of the transformer. This function has the analog slope controlled by the voltage of I_PEAK terminal.

Typical usages of this function are:

1. Having the dependency of battery voltage. When battery voltage is down, the peak current goes down. The easiest way is to connect a resistive divider with battery voltage. This saves the battery life.
2. Reducing peak current at primary side when the DSC/DVC system operates with large load current like powering a zooming lens motor. This avoids inadvertent shutdowns due to large current from the battery.

Three optional connections to I_PEAK are shown in Figure 1.

1. Use the controller to input PWM signal with the RC filter.
2. Use a D/A converter.
3. Use a resistive divider to input fixed value like VCC into I_PEAK terminal.

Method 1 and 2 make it possible to delicately control peak current at primary side. For example, set higher current during initial charging, but set the lower current just before complete charging. This effectively saves the battery life.

At a lower voltage of battery, there is some range not to flow the peak current due to line impedance at primary side of the transformer. Normally, the waveform of the current at primary side is very similar to a triangle wave but the slope is slow when line impedance is large and battery voltage is lower as shown in Figure 9. Due to this, the I_PEAK comparator cannot detect the turn-off timing and internal FET switch remains on until CHG terminal turns to low.

To avoid this, it is very important to reduce the line impedance including DC resistance of the transformer as much as possible if the peak current is defined as more than 1.2 A when battery voltage is selected from 1.4 V to 2.0 V.

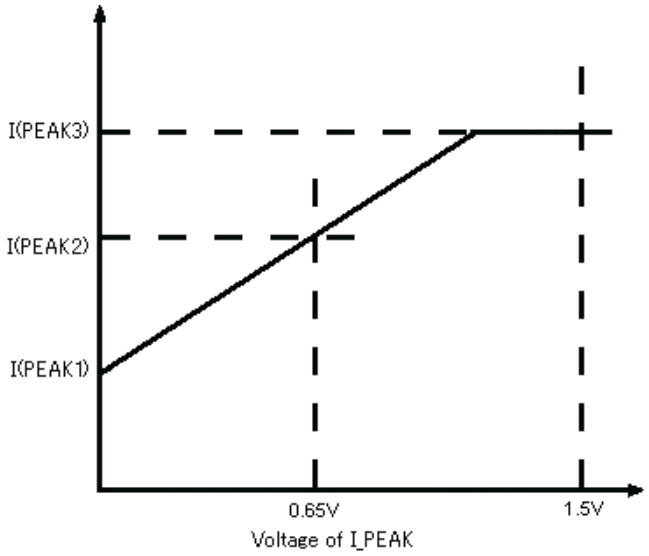

Figure 8. I_PEAK Terminal Voltage vs. Peak Current at Primary Side

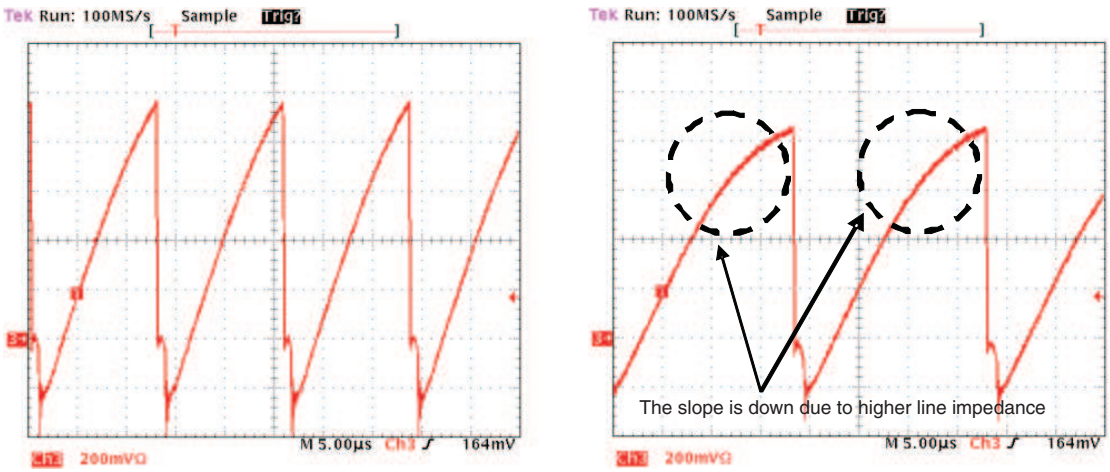

Figure 9. The Affect from Line Impedance at Primary Side

3.2 Design Transformer

3.2.1 How to Determine Turn Ratio and Primary Inductance

Before starting the design of transformer, the target output voltage at photo flash capacitor should be defined. To define it, Equation 4 is required.

$$N = \frac{V_{OUT} + V_f}{V_FULL} \tag{4}$$

Where:

- N - Turn ratio of transformer
- V_f - Forward voltage of FRD
- V_{OUT} - Target output voltage
- V_FULL - Primary target voltage

When the target output voltage is defined, it can calculate the turn ratio of the transformer with Equation 4. For example, the turn ratio of the transformer is around 10.9 when the target output voltage defined as 320 V at photo flash capacitor and forward voltage of FRD is 4 V. The recommended range of the turn ratio of transformer is from 10 to 12.

After that, the inductance of primary side is defined. The recommended inductance at primary side of the transformer depends on the peak current definition and battery voltage. The reason is to secure more than 300-ns pulse width at SW terminal for detecting target output voltage with U1 comparator when the internal FET switch is off. If the pulse width at SW terminal is less than 200 ns, U1 comparator cannot detect to stop charge operation and might cause the photo flash capacitor to break. To calculate the pulse width, the inductance at primary side of the transformer should meet Equation 5. The recommendation range of primary side inductance is from 7 µH to 15 µH for high efficiency.

$$L_P \geq \frac{200\ ns \bullet V_{OUT}}{N \bullet I_PEAK} \tag{5}$$

Where:

- L_P - Primary inductance
- N - Turn ratio of transformer
- V_{OUT} - Target output voltage
- I_PEAK - Peak current at primary side

3.2.2 Leakage Inductance

A transformer with too much leakage inductance at the primary side will break the internal FET switch because large voltage spikes (over 50 V) are inputted into the SW terminal as shown in Figure 10.

The leakage inductance of the transformer is determined by the coefficient of coupling, K, of the transformer (see Equation 6). For best results, the coefficient coupling should be more than 0.97.

$$K = \frac{L_P - L_{Pl}}{L_P} \tag{6}$$

Where:

- L_P - Primary inductance
- L_{Pl} - Primary leakage inductance

Table 1 shows the allowable maximum leakage inductance to protect the internal FET switch from inductive spikes when the internal FET switch turned off.

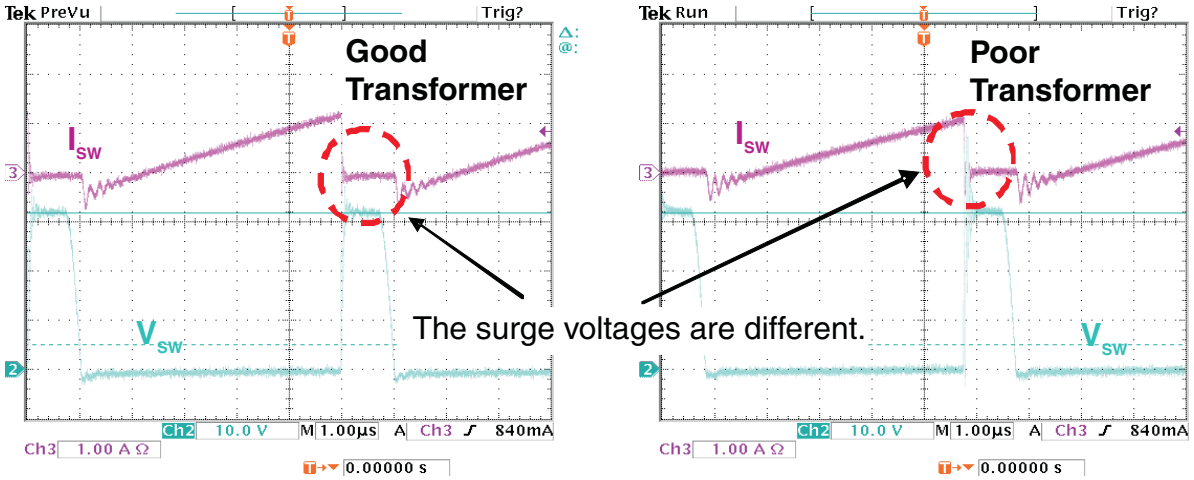

Figure 10. Surge Voltage at SW Terminal

Table 1. Guideline About Leakage Inductance

I_PEAK RANGE	MAX LEAKAGE INDUCTANCE (µH)
0.5 A to 1.1 A	0.20
1.1 A to 1.3 A	0.16
1.3 A to 1.5 A	0.14
> 1.5 A	0.12

3.2.3 DC Resistance

The DC resistance is determined by the number of turns of wire in the transformer and the wire's cross sectional area. A higher DC resistance increases the over all losses of the transformer. To get higher efficiency, you should select the transformer with the lower DC resistance.

3.3 Select FRD

3.3.1 Principle of Reverse Current

The most important factor in selecting FRD is the reverse recovery time (Trr). It affects both charging time and efficiency because it causes the reverse current at primary side. When FRD is recovery mode, the current in the secondary side should be flowing from the capacitor to the transformer. The mechanism of reverse current is described in the following steps (see Figure 11 and Figure 12).

1. Internal FET switch is on (status 1 and 6 at Figure 11)
   When the internal FET switch is on, the current at primary side is flowing forward and starts to store the energy at primary side. At that time, the voltage at cathode of FRD is smaller than the voltage at anode of FRD. It means that FRD is off and no current flows at secondary side.
2. Internal FET switch turns off (status 2 at Figure 11)
   When the Internal FET switch turns off, the current at primary side stops immediately, the voltage at the secondary side becomes positive thus forward biasing the FRD, the FRD turns on and secondary current flows to the photo flash capacitor.
3. E_{TRANS} is almost zero and reverse current flows (status 3 and 4 at Figure 11)

The stored energy at primary side (E_{TRANS}) transfers from the primary side to secondary side via transformer. While the current at secondary side flows forward into FRD, the energy transferring is continue. When the transferring completes, U2 comparator in Figure 2 detects the timing to turn on the internal FET switch and internal FET switch is on. However, FRD can not turn off immediately because of the reverse recovery time. Hence, reverse current at secondary side flows through FRD during reverse recovery time.

4. Recovery FRD (status 5 at Figure 11)

   After reverse recovery time, the voltage at cathode of FRD is larger than the voltage at anode of FRD. It makes FRD turn off and recover its operation.

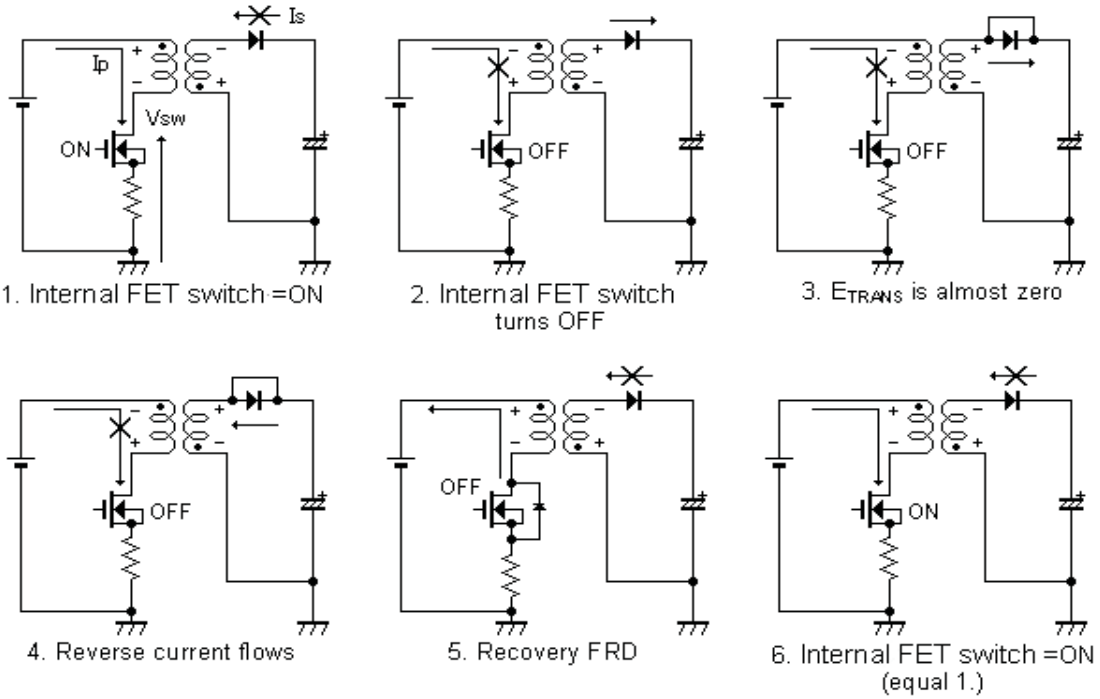

Figure 11. Mechanism of Reverse Current

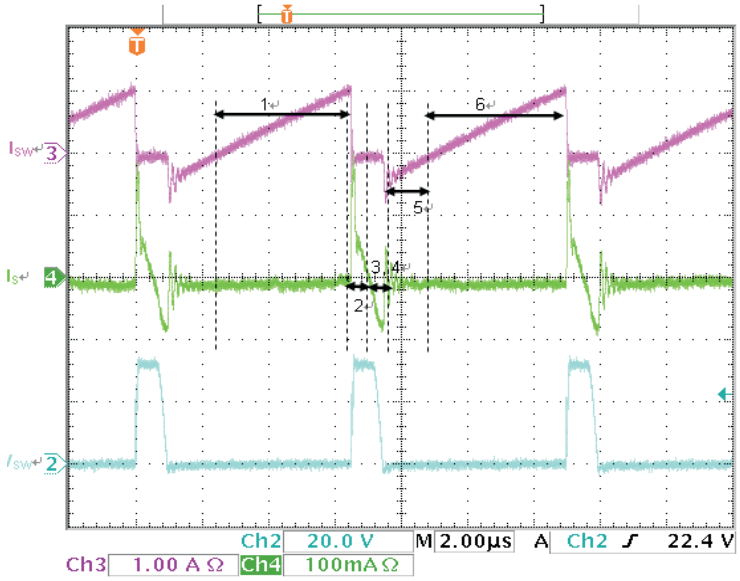

Figure 12. Diagram of Reverse Current

3.3.2 Important Reminders for Selecting FRDs

To select the proper FRD for the photo flash capacitor charger, consider the following guidelines.

1. Use a diode with faster Trr. The recommended value is less than 100 ns for getting higher efficiency.
2. Current through the FRD must not exceed the absolute maximum current flow of the forward current (I_{diode}). I_{diode} can be calculated by Equation 7.

$$I_{diode} = \frac{I_PEAK}{N} \quad (7)$$

Where:

- I_PEAK - Peak current at primary side
- N - Turn ratio of transformer

3. The absolute maximum reverse voltage (V_R) must not be exceeded. It can be calculated by Equation 8. The recommended value is more than 600 V.

$$V_R = V_{OUT} + N \bullet V_{BAT} \quad (8)$$

Where:

- V_{OUT} - Output voltage
- V_{BAT} - Battery voltage
- N - Turn ratio of transformer

3.4 Detect Charge Completion

When the TPS65573 detects the timing of charge completion, it makes the XFULL terminal low level. To communicate with controller to find charging completion, connect the XFULL terminal to the controller with a pull-up resistor (see Figure 13). The recommended value is 10 kΩ. It is strongly recommended that the CHG terminal should turn low level immediately after charging completion.

It is possible to drive an LED with the XFULL terminal for visual indication of charging status. The method is easy; connect the anode to the interface voltage ($V_{I/F}$) and the cathode to XFULL (see Figure 14). Figure 15 shows the current capability of MOSFET at the XFULL terminal.

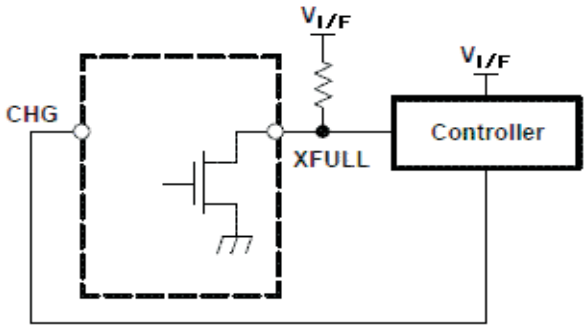

Figure 13. Connect Controller to XFULL

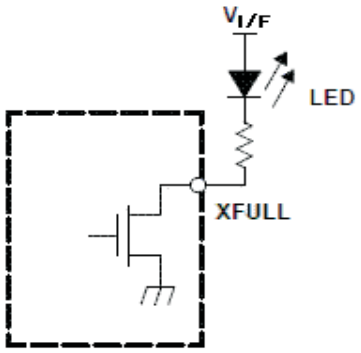

Figure 14. Connect LED to XFULL

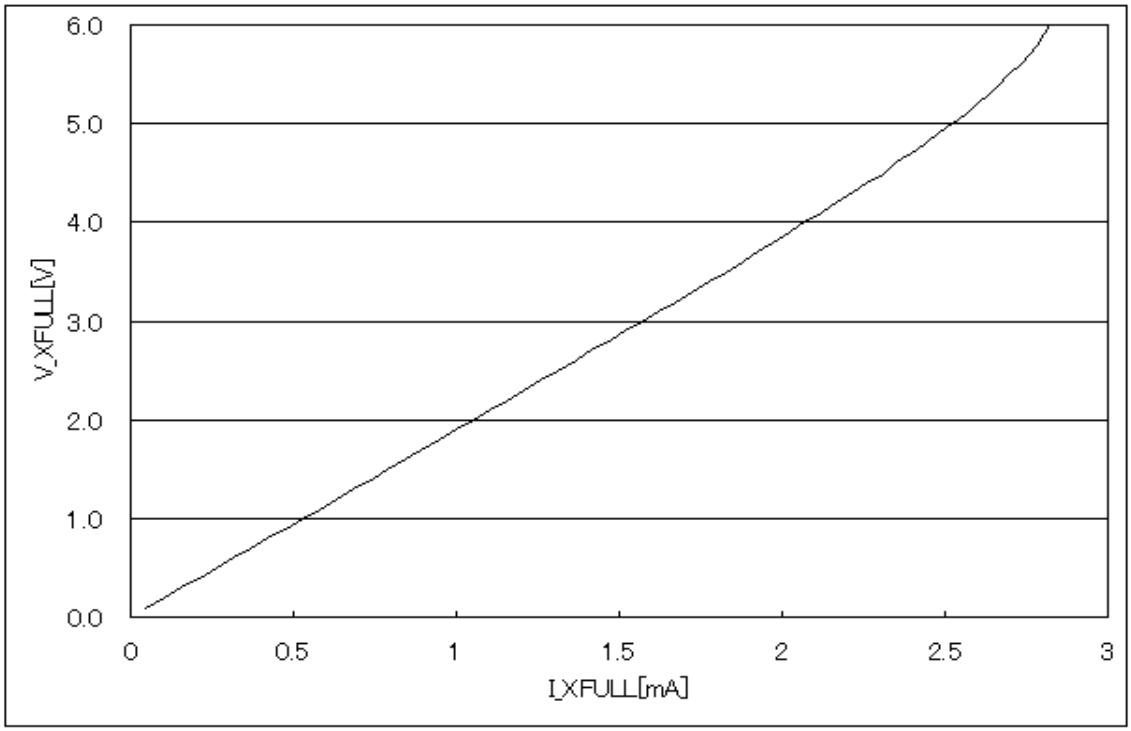

Figure 15. XFULL Terminal Current Capability

3.5 Photo Flash Capacitor

Ensure that the photo flash capacitor is a large-value type compared to that used in a forward converter. This is because the discharging energy of a flyback transformer is greater than that of a forward transformer. Equation 9 shows the computation for determining the photo flash capacitor value. Using a larger value than the one derived by this computation could burn out the flash element.

$$C_1 \leq \frac{2 \bullet E}{V_{OUT}^{\ 2}} \tag{9}$$

Where:

- C_1 - Photo flash capacitor value
- E - Absolute maximum energy for xenon tube
- V_{OUT} - Target output voltage

3.6 Design IGBT Driver

The TPS65573 must have external resistors at the G_IGBT_P and G_IGBT_N terminals to adjust the rise time and fall time at the gate of IGBT. Adjusting the rise time results in a faster response of the xenon flash and adjusting the fall time prevents the IGBT from being broken.

When IGBT is turned on, the voltage at gate of IGBT inputted from G_IGBT_P terminal should be over the threshold voltage specified by the datasheet of each IGBT. For example, VCC must be over 2.5 V when 2.5 V drive IGBT is used. At that time, the G_IGBT_P terminal should have current capability around 500 mA as peak current to charge the parasitic capacitor at the gate of IGBT for turning on as shown in Figure 16. It depends on the parasitic capacitance at the gate of IGBT and the input voltage of VCC.

When IGBT is turned off, the voltage regulation between emitter and corrector of IGBT must not be over the target specified by the datasheet of each IGBT. For example, the resistor connected to the G_IGBT_N terminal should be more than 68 Ω when IGBT is selected TIG032TS or TIG052TS as shown in Figure 17 and Figure 18. It shows the voltage waveform with connecting 68 Ω to the G_IGBT_N terminal.

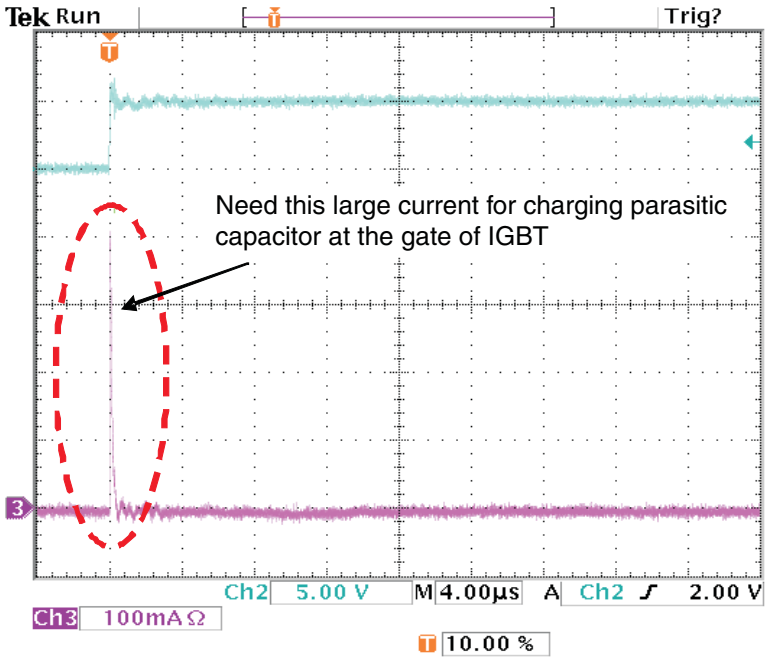

Figure 16. Current at G_IGBT_P Terminal when Xenon Lamp is On

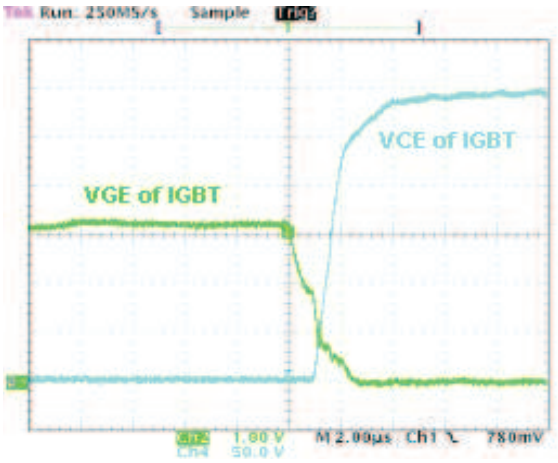

Figure 17. Waveform With TIG032TS

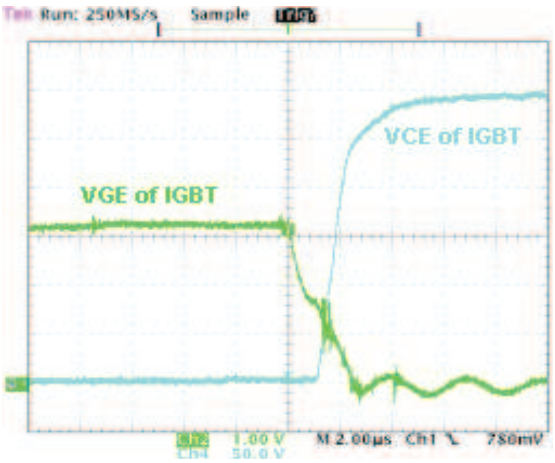

Figure 18. Waveform With TIG052TS

4 The Performance of TPS65573

4.1 Peak Current vs the voltage of I_PEAK Terminal

4.1.1 Peak Current Depends on the Delay at I_PEAK Comparator

The TPS65573 has an approximate 75-ns delay which is specified as “SW OFF after ISW exceeds the threshold defined by I_PEAK” in the product datasheet. Due to this, there is difference between the target peak current defined by the voltage of I_PEAK terminal and the actual peak current at SW terminal even though the voltage of I_PEAK terminal is same condition.

The difference depends on inductance at the primary side of transformer and battery voltage. The slope of the current at the primary side can be defined by these parameters.

$$I_PEAK = \frac{V_{BAT}}{L_P} T_{ON(n)} + Trr(n) \quad (10)$$

Where:

- $T_{ON(n)}$ - ON time at n cycle switching
- L_P - Primary inductance
- I_PEAK - Peak current at primary side
- V_{BAT} - Battery voltage
- Trr(n) - Reverse recovery time at n cycle switching

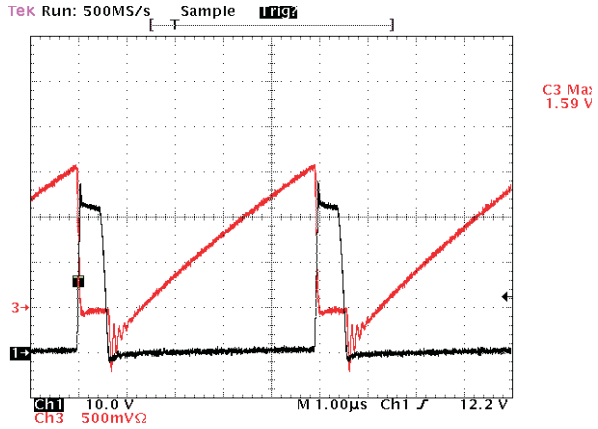

Figure 19. Peak Current (L_P = 7 µH, V_{BAT} = 4.2 V, I_PEAK = 1.5 V)

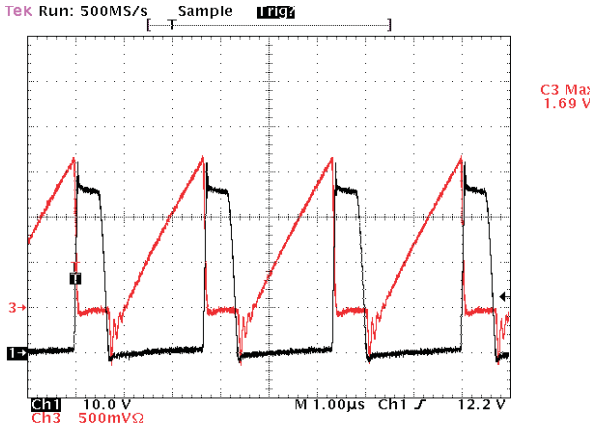

Figure 20. Peak Current (L_P = 7 µH, V_{BAT} = 8.4 V, I_PEAK = 1.5 V)

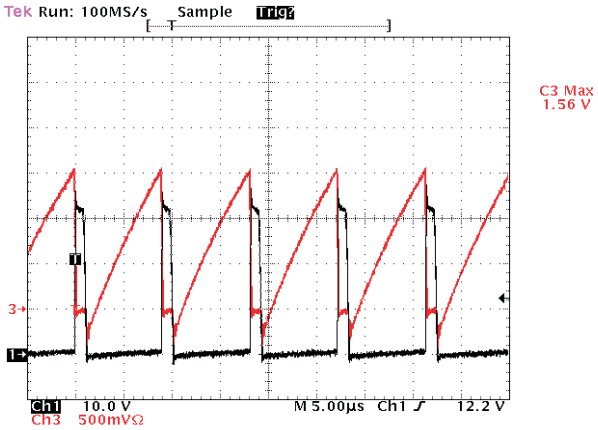

Figure 21. Peak Current (L_P = 15 µH, V_{BAT} = 4.2 V, I_PEAK = 1.5 V)

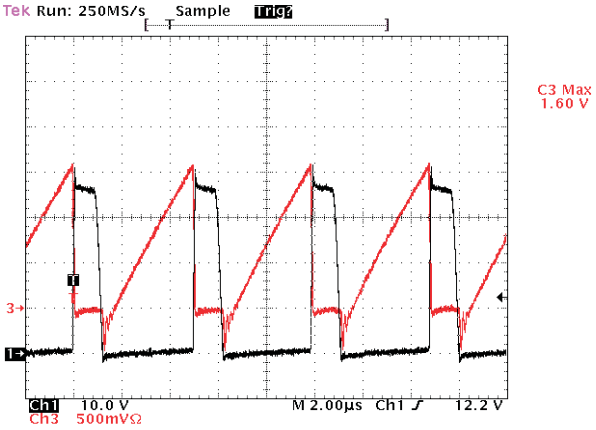

Figure 22. Peak Current (L_P = 15 µH, V_{BAT} = 8.4 V, I_PEAK = 1.5 V)

4.2 Efficiency and Charging Time

4.2.1 How to Calculate Average Current

Average current from the battery is the key parameter to calculate efficiency of the system. Below is the method of the calculation for average current from the battery.

At one switching, the charge comes from the battery and is calculated as shown in Equation 11.

$$\Delta Q = \int \frac{V_{BAT}}{L_P} dt = \frac{V_{BAT}}{2L_P} T^2_{ON(n)} \tag{11}$$

Where:

- ΔQ - Charge from battery at one switching
- L_P - Primary inductance
- V_{BAT} - Battery voltage
- $T_{ON(n)}$ - ON time at n cycle switching

The average current from the battery is calculated as shown in Equation 12.

$$I_{BATave} = \int_0^{T_c} \frac{\Delta Q}{T_{ON(n)} + T_{OFF(n)}} dt \tag{12}$$

Where:

- T_C - Charging time
- $T_{ON(n)}$ - ON time at n cycle switching
- $T_{OFF(n)}$ - OFF time at n cycle switching
- I_{BATave} - Average current from battery

Efficiency is defined as the output power divided by the input power as shown in Equation 13.

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{13}$$

Where:

- η - Efficiency
- P_{IN} - Input power
- P_{OUT} - Output power

The store power at primary side of the transformer (P_P) is calculated as shown in Equation 14.

$$P_P = V_{BAT} \bullet I_{BATave} \tag{14}$$

Where:

- P_P - Store power at primary side of transformer
- V_{BAT} - Battery voltage
- I_{BATave} - Average current from battery

The power at secondary side of the transformer (P_S) is equal to the energy discharged by the photo flash capacitor. It is calculated as shown in Equation 15.

$$P_S = \frac{1}{2 \bullet T} C_{OUT} \bullet (V_{OUT} - V_{ini})^2 \tag{15}$$

Where:

- C_{OUT} - Photo flash capacitor
- V_{OUT} - Output voltage after charging
- V_{ini} - Output voltage before charging
- T - Charging time

Therefore, efficiency is calculated as shown in Equation 16.

$$\eta = \frac{P_S}{P_P} = \left(\frac{1}{2} C_{OUT} \bullet (V_{OUT} - V_{ini})^2 \right) \Big/ V_{BAT} \bullet I_{BATave} \bullet T \quad (16)$$

Equation 16 computes measured efficiency with ideal conditions. However, the efficiency also depends on parameters such as DC resistance of the transformer, battery line impedance and reverse recovery time (Trr) of the FRD.

4.2.2 Evaluation Results Regarding STOP Voltage

The following evaluation data is checked with TPS65573EVM.

Parameters:

- V_{CC} = 3.3 V
- Ambient temperature (T_A) = 25°C
- Voltage of I_PEAK terminal = 0.0 / 0.4 / 0.8 / 1.2 / 1.5 V
- Target output voltage (V_{OUT}) = 320 V
- Photo flash capacitor (C_{OUT}) = 90 µF

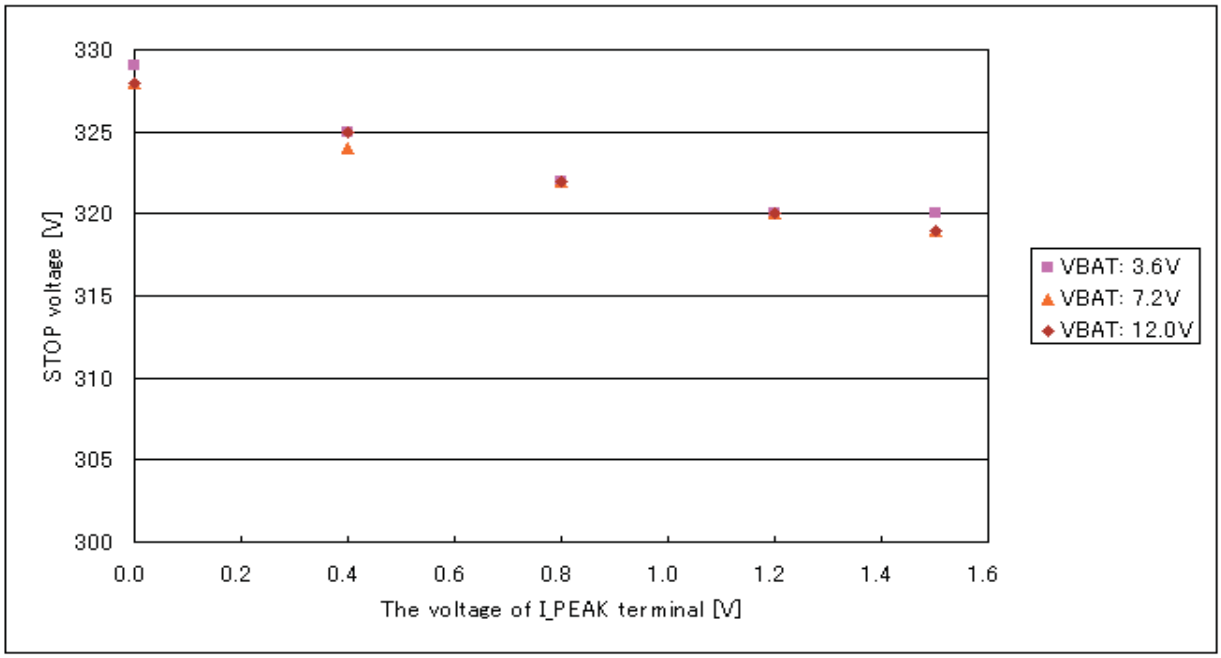

Figure 23. STOP Voltage With TPS65573EVM

4.2.3 Evaluation Results Regarding Efficiency

The following evaluation data is checked with TPS65573EVM.

Parameters:

- V_{CC} = 3.3 V
- Ambient temperature (T_A) = 25°C
- VBAT = 3.6 / 7.2 / 12.0 V
- Voltage of I_PEAK terminal = 0.0 / 0.4 / 0.8 / 1.2 / 1.5 V
- Target output voltage (V_{OUT}) = 320 V
- Photo flash capacitor (C_{OUT}) = 90 µF

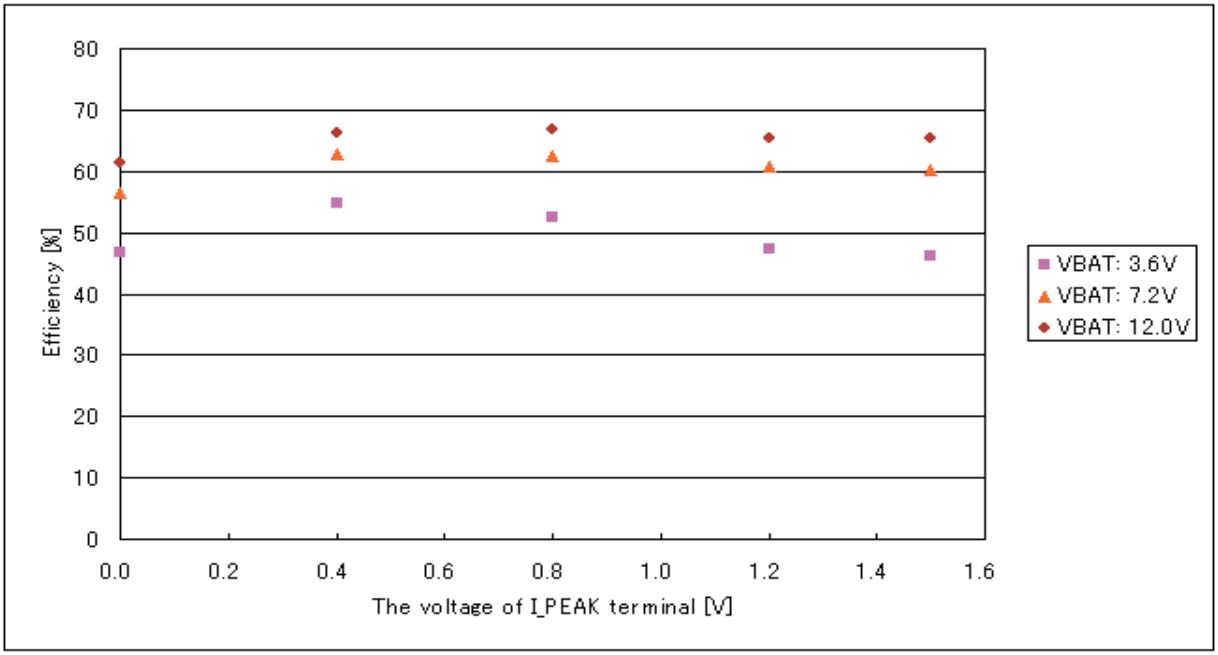

Figure 24. Efficiency With TPS65573EVM

4.2.4 Evaluation Results Regarding Charging Time

The charging time is defined by measuring the time from turning CHG terminal to a high level with less than 100 mV at the photo flash capacitor to turning XFULL to a low level.

The following data is checked with TPS65573EVM.

Parameters:

- V_{CC} = 3.3 V
- Ambient temperature (T_A) = 25°C
- VBAT = 3.6 / 7.2 / 12.0 V
- Voltage of I_PEAK terminal = 0.0 / 0.4 / 0.8 / 1.2 / 1.5 V
- Target output voltage (V_{OUT}) = 320 V
- Photo flash capacitor (C_{OUT}) = 90 µF

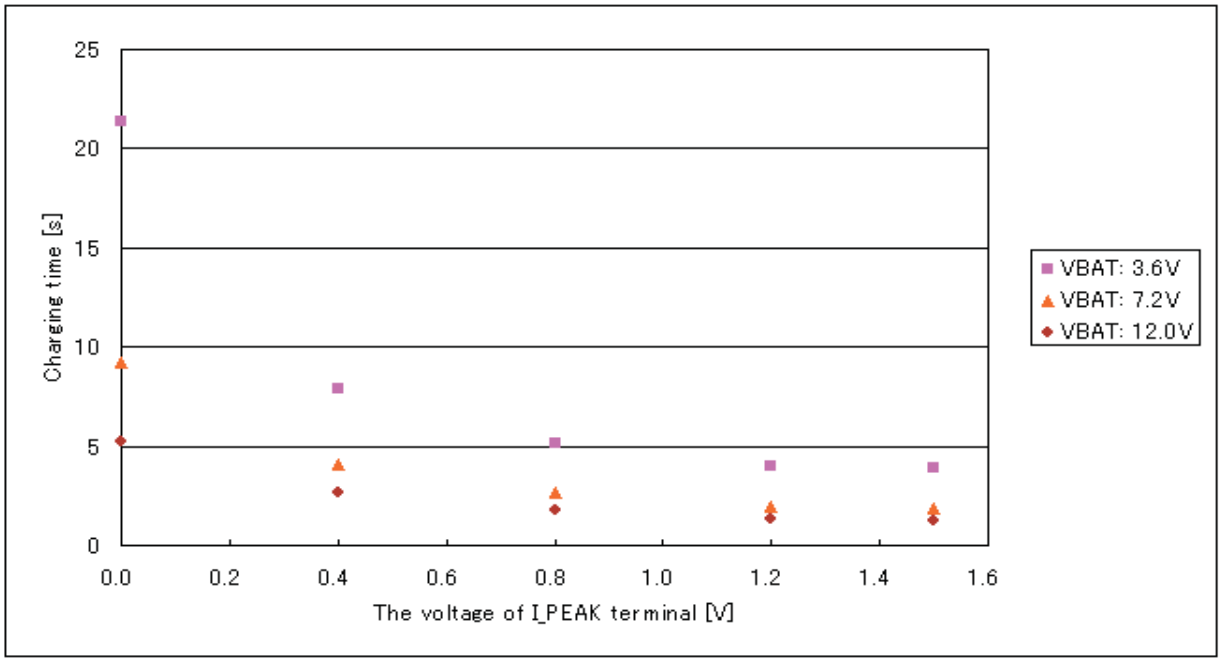

Figure 25. Charging Time With TPS65573EVM

4.3 How to Get Better Performance With TPS65573

Power loss is not only on resistance at internal FET, but transformer, line impedance and FRD also have power loss factors as shown below.

- Transformer

  The transformer has two main factors regarding power loss; copper loss and the core loss. Larger diameter wire is the only way to reduce the copper loss. It means that total size of the transformer should be larger for high efficiency.

  Changing the core material may also result in better performance. The key parameters are better frequency characteristics, increasing the effective core area or increasing the number of turns in the winding. These factors also increase the size of the transformer.
- Line impedance

  To improve the efficiency, the line impedance should be reduced as much as possible. This can be accomplished by using wide traces on the circuit board.
- FRD

  The efficiency depends on the parametric capacitance and the reverse recovery time.

  Smaller Trr and parametric capacitance can achieve higher efficiency.
- Photo flash capacitor/target output voltage

  A smaller output voltage value is effective to reduce the charging time, but this value is dependent on the brightness of the xenon lamp since the flash brightness depends on the energy stored in the photo flash cap. The required flash intensity should be defined first.

5 Recommended External Components

5.1 Transformers

Table 2. Recommended Transformer (Tokyo Coil Engineering)(1)

TYPE NO.	SIZE W x D x H (mm)	L_P (µH)	I_{SW} (MAX) (A)	R_{PRI} (m)	R_{SEC}	TURN RATIO
TTRN-0530H	5.0 x 5.0 x 3.0	13	1.5	500	45	1:11

(1) Values referenced are for design purposes.

Contact information (Tokyo Coil Engineering):

- TEL: +81-426-56-6262
- FAX: +81-426-56-6336
- E-mail: tce@tokyo-coil.co.jp
- Web: http://www.tokyo-coil.co.jp/

5.2 Fast Recovery Diode (FRD)

Table 3. Recommended FRD (Origin ELECTRIC CO., LTD.)

TYPE NO.	MAX RESERVE VOLTAGE (V)	FORWARD VOLTAGE (V)	MAX FORWARD CONTINUOUS CURRENT (A)	Trr(1) (ns)	SIZE W x D x H (mm)
FV02R80	800	4	200	40	2.50 x 1.25 x 0.55

(1) The measured condition is IF = IR = 100 mA.

Contact information (Origin ELECTRIC CO., LTD.):

- TEL: +81-3-5954-9117
- FAX: +81-3-5954-9122
- E-mail: h_teramoto@origin.jp
- Web: http://www.origin.co.jp/

Table 4. Recommended FRD (SANYO Semiconductor Co., Ltd.)

TYPE NO.	MAX RESERVE VOLTAGE (V)	FORWARD VOLTAGE (V)	MAX FORWARD CONTINUOUS CURRENT (A)	Trr(1) (ns)	SIZE W x D x H (mm)
RE0208DA	800	4	200	55	1.25 x 1.25 x 0.9

(1) The measured condition is IF = IR = 100 mA.

Contact information (SANYO Semiconductor Co., Ltd.):

- TEL: +81-276-61-8055
- FAX: +81-276-61-8854
- E-mail: Products_Hd@sanyo.com
- Web: http://www.semic.sanyo.co.jp/index_e.htm

5.3 Insulated Gate Bipolar Transistor (IGBT)

Table 5. Recommended IGBT (SANYO Semiconductor Co., Ltd.)

TYPE NO.	VCES (V)	ICPA (A)	DRIVE VOLTAGE (V)	Cies (pF)	SIZE
TIG032TS	400	180	2.5 / 4.0	5100	3.0 x 6.4 x 1.0
TIG052TS	400	180	2.5	3800	3.0 x 6.4 x 1.0

Contact information (SANYO Semiconductor Co., Ltd.):

- TEL: +81-276-61-8055
- FAX: +81-276-61-8854
- E-mail: Products_Hd@sanyo.com
- Web: http://www.semic.sanyo.co.jp/index_e.htm

6 Important Notice for PCB Design

The following PCB layout considerations can also result in better performance.

- **NOTE 1:** Any design factor resulting in a large leakage inductance value on the primary side should be avoided because it can lead to device failure due to over voltage at the SW terminal. Section 3.2.2 illustrates the guide line of leakage inductance.
- **NOTE 2:** The loop indicated by the line in red in Figure 26 should be connected as close as possible to reduce voltage spikes at the SW terminal. If this loop is not close, the parasitic inductance might cause device failure.
- **NOTE 3:** The parasitic resistance in the power path from the battery to primary-side turn of the transformer should not be ignored because the large current flows from the battery to primary-side turn of the transformer. The TPS65573 has a single-point ground connection inside the TPS65573 at GND terminal. Therefore, the PCB layout should also keep a single point ground connection at the GND terminal of TPS65573. A bypass capacitor (C1 in Figure 26) is required to avoid noise introduced by grounding, the recommended value is 1 μF. Also the distance from C1 and VCC (GND) should be minimized.
- **NOTE 4:** To operate the TPS65573 at a lower battery voltage (the voltage of VBAT terminal is less than 2.0 V), two bypass capacitors (C2 and C3 in Figure 26) should be required to reduce the waggle at the VBAT terminal. C2 is the bypass capacitor from VBAT terminal to GND, the recommended value is 10 μF, put it as close as possible to the VBAT terminal. C3 is the bypass capacitor from battery line to GND, the recommended value is 10 μF, put it as close as possible to the transformer.

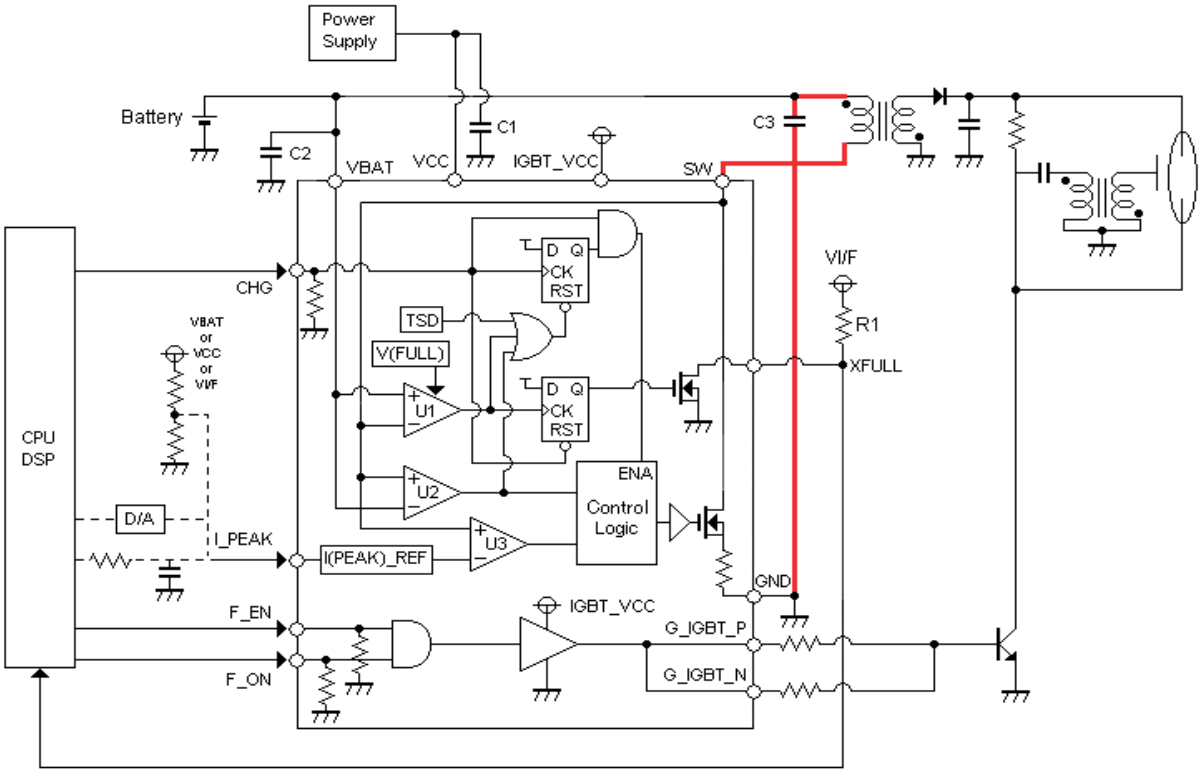

Figure 26. PCB Design Guideline

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