Application Report
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High Integration, High Efficiency Power Solution Using DCDC Converters for TMS320C2834x Microcontrollers

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ABSTRACT

This reference design is intended for users designing with theTMS320C2834x Microcontrollers. This design, employing sequenced power supplies, describes a system with an input voltage of 5V, and uses a high-efficiency DCDC Converter with integrated FETs for a simple and integrated design.

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1 Introduction

In multi-voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and obtain reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power up and power down operations.

Sequencing refers to the order, timing, and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first failure represents a threat to the long term reliability of the dual voltage device, while the second failure poses the possibility of immediate damage to interface circuits in the processor or system devices such as memory, logic, or data converter ICs.

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up, which may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

The power-on sequencing for TMS320C2834x Microcontrollers are shown in the Power Requirements table below. As mentioned in the table, all voltage rails should be powered up within 5ms.

2 Power Requirements

The power requirements are as specified in Table 1.

Table 1. TMS320C2834x Power Specs

	PIN NAME(s)	VOLTAGE (V)	Imax (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
Core	VDD	1.1 / 1.2 (1)	1000 (2)	±5%	1	All voltage rails should be powered up within 5ms
I/O	VDD18	1.8	80	±5%	2	
I/O	VDDIO	3.3	200	±5%	2	

(1) CVDD = 1.2V for 300MHz devices; CVDD = 1.1V for 200MHz.
(2) Max current on VDD at 300MHz is 1000mA; max current on VDD at 200MHz is 600mA.

3 Features

The design uses the following high-efficiency DCDC Converter with integrated FETs.

Devices:	TPS65000
Power supply specs:	
Vin	5 V ± 10%
Vout1	1.1 V/1.2 V ± 5% at 1000 mA
Vout2	1.8 V ± 5% at 80 mA
Vout3	3.3 V ± 5% at 200 mA
Sequencing	1) Vout1 2) Vout2 and Vout3

TPS65000

- Step-Down Converters
  - Spread Spectrum Clock (SSC) Generation
  - For Reduced EMI
  - 2.25MHz Fixed Frequency Operation
- LDOs
  - Adjustable output voltage
  - Up to 300mA Output Current
  - Separate power Input and Enable

More information on the Devices can be found from the datasheet.

TPS65000 SLVS810

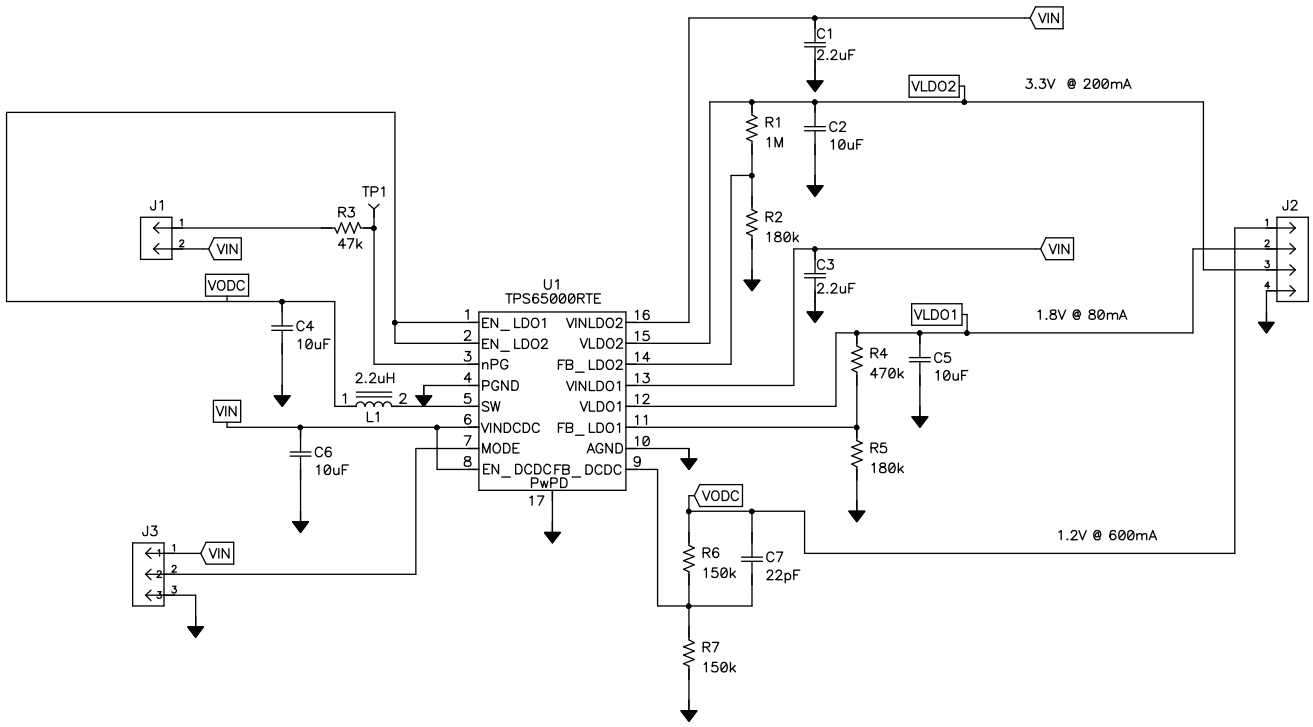

Figure 1. PMP5000 Reference Design Schematic

Proper sequencing is achieved in the design with the use of enable pins. The Core 1.2V at 1000mA (Step Down Converter in TPS65000) comes first, which in turn enables the LDOs of the device thus, following the required sequence.

4 List of Material

Table 2. PMP5000 List of Material

Count	RefDes	Value	Description	Size	Part Number	MFR	AREA
2	C1	2.2 µF	Capacitor, Ceramic, vvV, [temp], [tol]	0603	GRM39yyyxxxKvvvA	Murata	5650
4	C2	10 µF	Capacitor, Ceramic, 10 µF, 10V, X5R, 10%,	0805	GRM21BR61A106KE19L	Murata	10560
	C3	2.2 µF	Capacitor, Ceramic, vvV, [temp], [tol]	0603	GRM39yyyxxxKvvvA	Murata	5650
	C4	10 µF	Capacitor, Ceramic, 10 µF, 10V, X5R, 10%,	0805	GRM21BR61A106KE19L	Murata	10560
	C5	10 µF	Capacitor, Ceramic, 10 µF, 10V, X5R, 10%,	0805	GRM21BR61A106KE19L	Murata	10560
	C6	10 µF	Capacitor, Ceramic, 10 µF, 10V, X5R, 10%,	0805	GRM21BR61A106KE19L	Murata	10560
1	C7	22 pF	Capacitor, Ceramic, 22 µF, 6.3V, X5R, 20%,	0805	GRM21BR60J226ME39L	Murata	10560
1	J1	PTC36SAAN	Header, Male 2-pin, 100 mil spacing, (36-pin strip)	0.100 inch x 2	PTC36SAAN	Sullins	
1	J2	PTC36SAAN	Header, Male 4-pin, 100 mil spacing, (36-pin strip)	0.100 inch x 4	PTC36SAAN	Sullins	50000
1	J3	PTC36SAAN	Header, Male 3-pin, 100 mil spacing, (36-pin strip)	0.100 inch x 3	PTC36SAAN	Sullins	0.043 inch
1	L1	2.2 µH	Inductor, SMT Multi-layer, yyA, zzmilliohm	2520 mm	MIPS2520D2R2	FDK Corp.	20400
1	R1	1M	Resistor, Chip, 1/10W, 1%	0805	CRCW0805-xxxx-F	Vishay	15,300
2	R2	180k	Resistor, Chip, 1/10W, 1%	0805	CRCW0805-xxxx-F	Vishay	15,300
1	R3	47k	Resistor, Chip, 1/10W, 1%	0805	CRCW0805-xxxx-F	Vishay	15,300

Table 2. PMP5000 List of Material (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR	AREA
1	R4	470k	Resistor, Chip, 1/10W, 1%	0805	CRCW0805-xxxx-F	Vishay	15,300
	R5	180k	Resistor, Chip, 1/10W, 1%	0805	CRCW0805-xxxx-F	Vishay	15,300
2	R6	150k	Resistor, Chip, 1/10W, 1%	0805	CRCW0805-xxxx-F	Vishay	15,300
	R7	150k	Resistor, Chip, 1/10W, 1%	0805	CRCW0805-xxxx-F	Vishay	15,300
1	TP1	10000	Through Hole, O.040 Dia		STD	STD	0.100 x 0.100 inch
1	U1	TPS65000RTE	IC, 2.25MHz Step-Down Converter W/ dual LDO and SVS	QFN-16	TPS65000RTE	TI	83200

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

5 Test Results

The startup waveform, shown in Figure 2, demonstrates that the required sequencing order is followed.

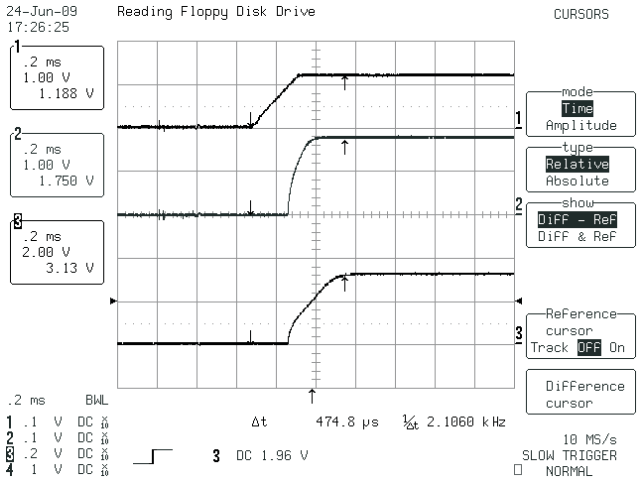

Figure 2. Shows Sequencing in Start up Waveform

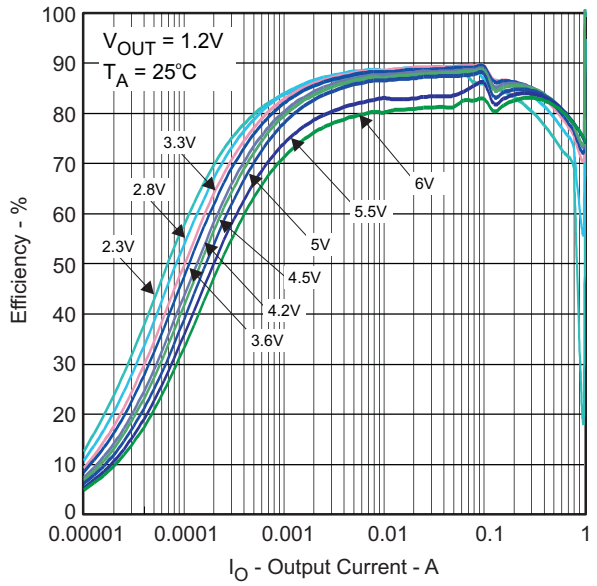

Figure 3. Efficiency vs Output Current (TPS65000)

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