

High Integration, High Efficiency Power Solution using DCDC Converters for TMS320DM365 Processor

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PMP - DC/DC Low Power Converters

ABSTRACT

This reference design is intended for users designing with the TMS320DM365 Processor. This design is ideal for achieving the requirement of a input voltage of 5V, and uses a multi-output DCDC Converter with integrated FETs for a simple and highly integrated configuration.

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1 Introduction

In multi-voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power up and power down operations.

Sequencing refers to the order, timing and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long term reliability of the dual voltage device, while the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter ICs.

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up. Bus contention may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

2 Power Requirements

The power specifications and sequencing requirements for TMS320DM365 Processor is shown in the table below.

Table 1. TMS320DM365 Power Specs

	Pin Name	Voltage (V)	I _{max} (mA)	Tolerance	Sequencing Order
Core	CVDD, VDD12_PRTCSS, VDDA12_DAC, VPP	1.2 *	650	±5%	1
I/O	VDDS18, VDD18_PRTCSS, VDDMXI, VDD18_SLDO, VDD18_DDR, VDDA18_PLL, VDDA18_USB, VDDA18_VC, VDDA18_ADC, VDDA18_DAC	1.8	95	±5%	2
I/O	VDDS33, VDDA33_USB, VDDA33_VC	3.3	51	±5%	3
I/O	VDD_AEMIF1_18_3 3, VDD_AEMIF2_18_3 3, VDD_ISIF18_33	1.8 / 3.3	65	±5%	Ramp with appropriate voltage
Note: <ul style="list-style-type: none"> • If running DM365 @ 300MHz, then CVDD, VDD12_PRTCSS, VDDA12_DAC and VPP = 1.35V and I_{max} = 800mA. • If using PRTCSS, power-up sequencing changes to: <ol style="list-style-type: none"> 1. Power on PRTCSS core (1.2-V) while RESET is low 2. Power on PRTCSS I/O (1.8-V) 3. Power on Main core (1.2-V) 4. Power on Main I/O (1.8-V) 5. Power on Main/Analog I/O (3.3-V) 					

3 Features

The design uses the following high-efficiency DCDC Converter with integrated FETs.

Devices:	TPS65053
Power supply specs:	
V _{in}	12 V ± 10%
V _{out1}	1.2 V ± 5% at 800 mA
V _{out2}	1.8 V ± 5% at 200 mA
V _{out3}	3.3 V ± 5% at 200 mA
Sequencing	1) V _{out1} 2) V _{out2} 3) V _{out3}

TPS65053

- Step-Down Converters
 - Up To 95% Efficiency
 - DCDC1 = 1 A; DCDC2 = 0.6 A
 - DC/DC Converters Externally Adjustable
- LDOs
 - Adjustable output voltage
 - Up to 400 mA Output Current (LDO1)
 - Separate power Input and Enable

More information on the Devices can be found from the datasheet.

TPS65053 – [SLVS754B](#)

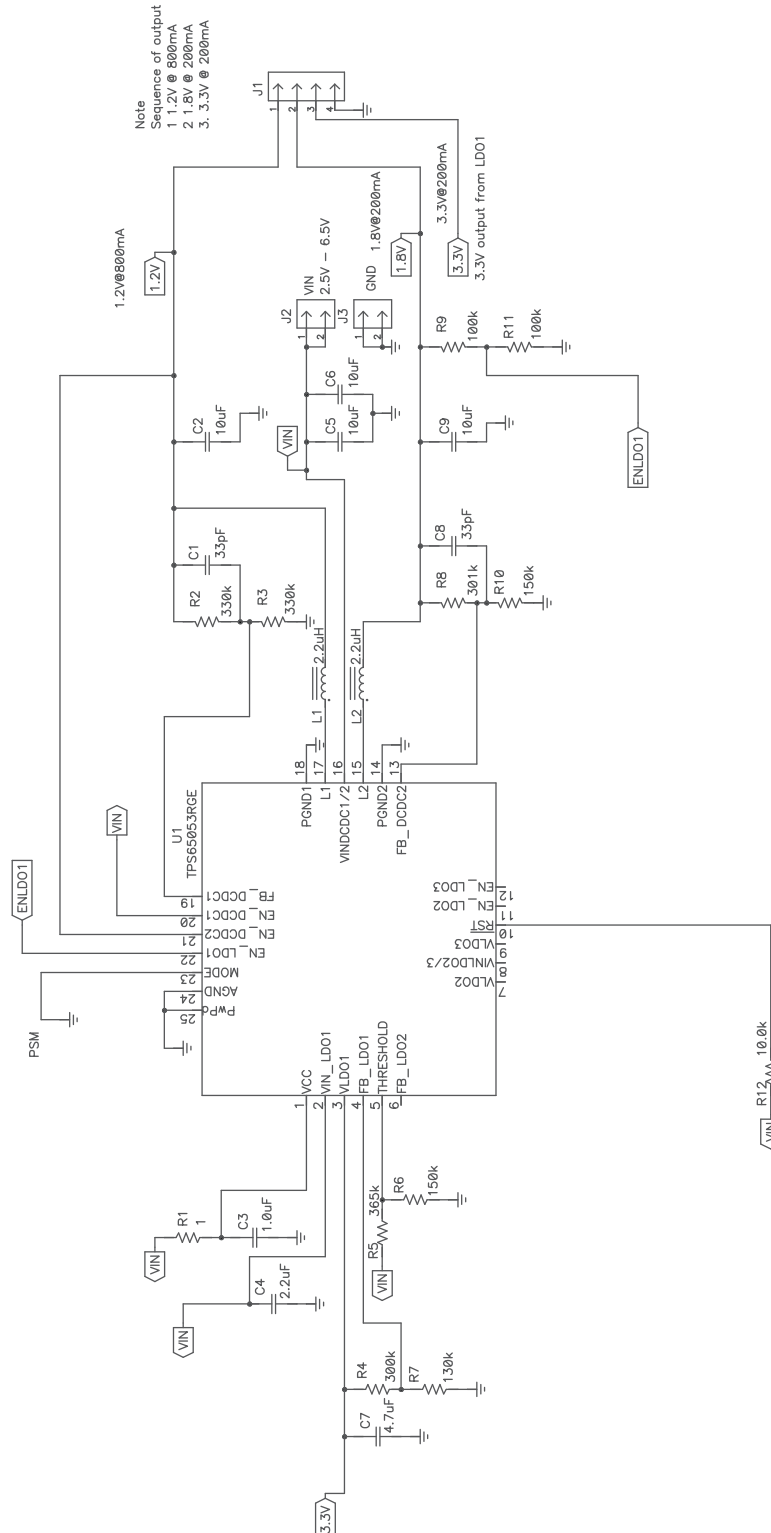


Figure 1. PMP5049 Reference Design Schematic

Proper sequencing is achieved in the design with the use of enable pins. The Core 1.2V at 800 mA (DCDC1 in TPS65053) comes first, which in turn enable the DCDC2. The output from DCDC2 is then used to enable the LDO1 of the device thus, following proper sequence.

4 List of Materials

Table 2. PMP5049 List of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
2	C1	33 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H330J	TDK	5650
4	C2	10 μ F	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata	10560
1	C3	1.0 μ F	Capacitor, Ceramic, 16V, X7R, 10%	0603	C1608X7R1C105K	TDK	5650
1	C4	2.2 μ F	Capacitor, Ceramic, 10V, X5R, 10%	0603	GRM188R61A225KE34D	Murata	5650
	C5	10 μ F	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata	10560
	C6	10 μ F	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata	10560
1	C7	4.7 μ F	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM219R61A475KE19D	Murata	10560
	C8	33 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H330J	TDK	5650
	C9	10 μ F	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	Murata	10560
1	J1	PEC36SAAN	Header, Male 4-pin, 100mil spacing, (36-pin strip)	0.100 inch x 4	PEC36SAAN	Sullins	50000
2	J2	PTC36SAAN	Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins	
	J3	PTC36SAAN	Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins	
2	L1	2.2 μ H	Inductor, SMT, 1.5A, 110m Ω	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft	26,560
	L2	2.2 μ H	Inductor, SMT, 1.5A, 110m Ω	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft	26,560
1	R1	1	Resistor, Chip, 1/16W, 5%	0603	Std	Std	9100
2	R2	330k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
	R3	330k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
1	R4	300k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
1	R5	365k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
2	R6	150k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
1	R7	130k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
1	R8	301k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
2	R9	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
	R10	150k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
	R11	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
1	R12	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5,650
1	U1	TPS65053RGE	IC, 2.25 MHz Dual Step-down Converter With 3 Low Input Voltage LDOs	QFN24	TPS65053RGE	TI	108800

- Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
 2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
 4. Ref designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.

5 Test Result

The startup waveform, shown in [Figure 2](#), demonstrates that the required sequencing order is followed

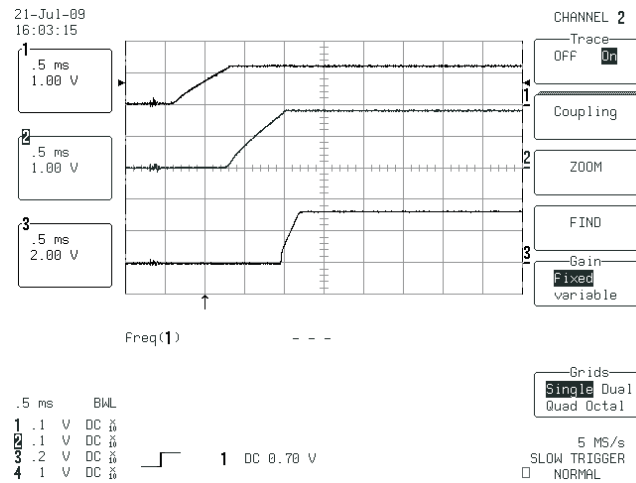


Figure 2. Shows Sequencing in Startup Waveform

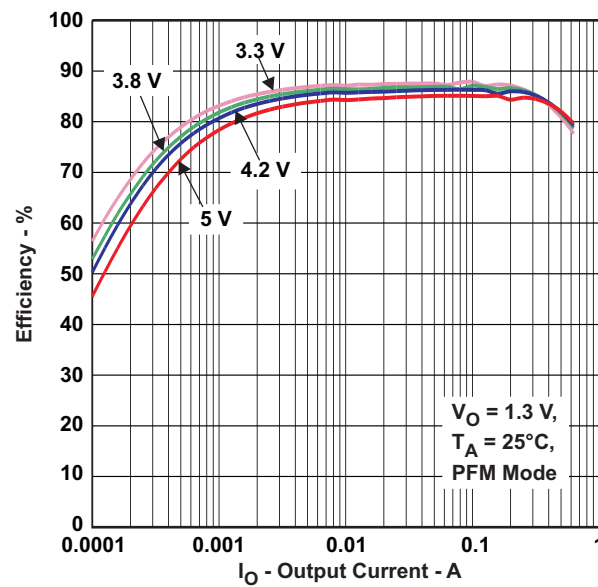


Figure 3. Efficiency vs Output Current (TPS65053)

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