Application Note

Using the TPS6215x in an Inverting Buck-Boost Topology

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Low Power DC-DC Applications

ABSTRACT

The TPS6215x family of synchronous buck dc-to-dc converters from Texas Instruments features a wide operating input voltage range from 3 V to 17 V and an adjustable output voltage of 0.9 V to 6 V. These devices are well-suited for many applications, such as standard 12-V rail supplies, embedded systems, and portable applications. Furthermore, the TPS6215x can be configured in an inverting buck-boost topology, where the output voltage is inverted or negative with respect to ground. This application report describes the inverting buck-boost topology in detail for the TPS6215x family. This topology can also be applied to the TPS6213x/4x/6x/7x converters.

Note

Precautions need to be taken when using these devices in an inverting buck-boost topology. Please review Section 2.1 to understand and robustly eliminate known risk.

Table of Contents

List of Figures

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1 Inverting Buck-Boost Topology

1.1 Concept

The inverting buck-boost topology is very similar to the buck topology. In a standard buck configuration, shown in Figure 1-1, the positive connection (V_{OUT}) is connected to the inductor and the return connection is connected to the device ground.

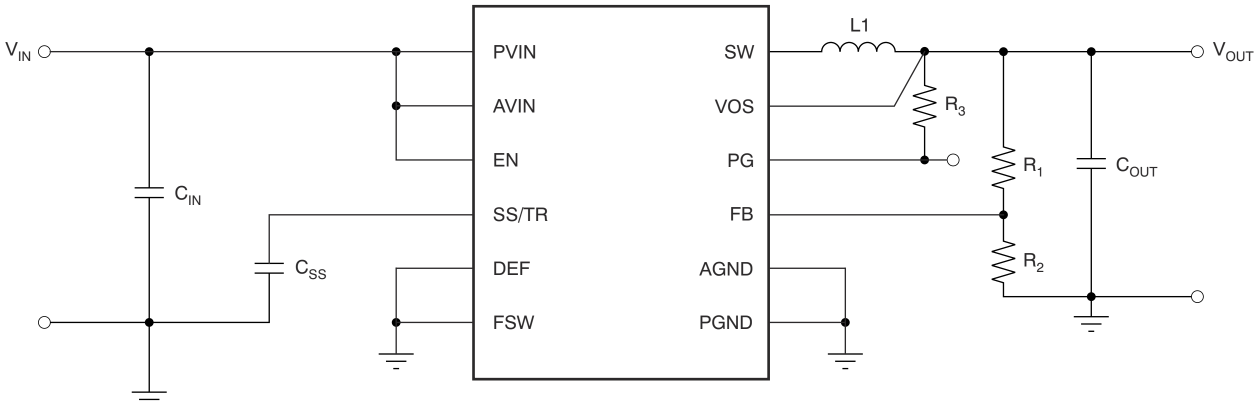


Figure 1-1. Buck Topology

However, in the inverting buck-boost configuration illustrated in Figure 1-2, the device ground is used as the negative output voltage pin (labeled as V_{OUT}). What was previously the positive output in the buck configuration is now used as the ground (GND). This shift in topology allows the output voltage to be inverted and always remain lower than the ground.

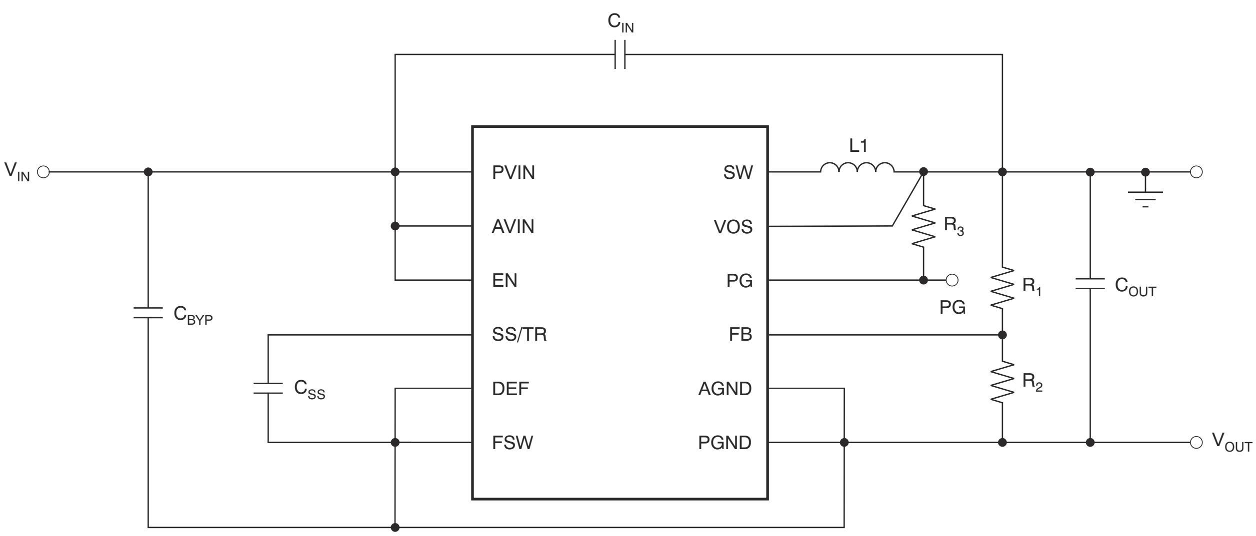


Figure 1-2. Inverting Buck-Boost Topology

The circuit operation in the inverting buck-boost topology differs from that in the buck topology. Though the components are connected the same as with a buck converter, the output voltage terminals are reversed, as Figure 1-3(a) shows. During the *on* time of the control MOSFET, shown in Figure 1-3(b), the inductor is charged with current, while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the *off* time of the control MOSFET and the *on* time of the synchronous MOSFET, shown in Figure 1-3(c), the inductor provides current to the load and the output capacitor. These changes affect many parameters, as discussed in the *Design Considerations* section.

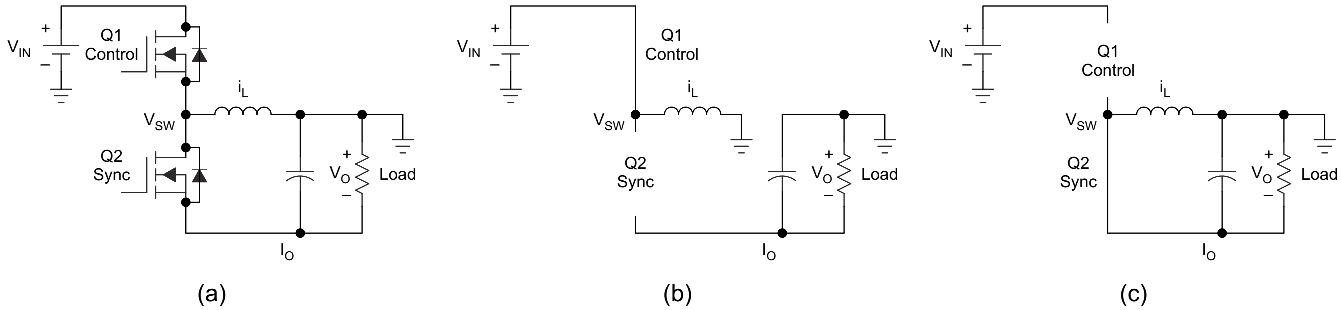


Figure 1-3. Buck-Boost Configuration

1.2 Output Current Calculations

The average inductor current is also affected in this topology. In the buck configuration, the average inductor current is equal to the average output current because the inductor always supplies current to the load during both the *on* and *off* times of the control MOSFET. However, in the inverting buck-boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the *on* time of the control MOSFET. During the *off* time, the inductor connects to both the output capacitor and the load (see Figure 1-3). Knowing that the *off* time is (1 – D) of the switching period, Equation 1 can be used to calculate the average inductor current:

$$I_{L(Avg)} = \frac{I_{OUT}}{(1 - D)} \tag{1}$$

The operating duty cycle for an inverting buck-boost converter can be found with Equation 2:

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} \times \frac{1}{\eta} \tag{2}$$

rather than V_{OUT}/V_{IN} for a buck converter. The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. The peak-to-peak inductor ripple current is given by Equation 3:

$$\Delta I_L = \frac{V_{IN} D}{f_S L} \tag{3}$$

where:

- ΔI_L (A): the peak-to-peak inductor ripple current
- D: duty cycle
- η: efficiency
- f_S (MHz): switching frequency
- L (μH): inductor value
- V_{IN} (V): the input voltage with respect to ground, not with respect to the device ground or V_{OUT}

Equation 4 calculates the maximum inductor current:

$$I_L = I_{L(avg)} + \frac{\Delta I_L}{2} \tag{4}$$

For example, for an output voltage of –3.3 V, 2.2-μH inductor, and input voltage of 12 V, the following calculations produce the maximum allowable output current that can be ensured based on the TPS62150 minimum current limit value of 1.4 A. The efficiency term is estimated at 85%.

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} \times \frac{1}{\eta} = \frac{-3.3}{-3.3 - 12} \times \frac{1}{0.85} = 0.254 \tag{5}$$

$$\Delta I_L = \frac{V_{IN} \times D}{f_s \times L} = \frac{12 \times (0.254)}{2.5\text{MHz} \times 2.2\mu\text{H}} = 554\text{mA} \tag{6}$$

Rearranging Equation 4 and setting $I_{L(max)}$ equal to the minimum value of I_{LIMF}, as specified in the datasheet, gives:

$$I_{L(avg)} = I_{L(max)} - \frac{\Delta I_L}{2} = 1.4 - \frac{0.554}{2} = 1123\text{mA} \tag{7}$$

This result is then used in Equation 1 to calculate the maximum achievable output current:

$$I_{OUT} = I_{L(avg)} \times (1 - D) = 1123\text{mA} \times (1 - 0.254) = 838\text{mA} \tag{8}$$

Table 1-1 provides several examples of the calculated maximum output currents for different output voltages (–1.8 V, –3.3 V and –5 V) based on an inductor value and switching frequency of 2.2 μH and 2.5 MHz, respectively. Increasing the inductance and/or input voltage allows higher output currents in the inverting buck-boost configuration, while using the low frequency setting decreases the available output current. The maximum output currents for the TPS62150 in the inverting buck-boost topology are frequently lower than 1000 mA due to the fact that the average inductor current is higher than that of a typical buck. The output current for the same three output voltages and different input voltages is displayed in Figure 1-4.

Table 1-1. Maximum Output Current Calculation for Different Values of V_{IN} and V_{OUT}

f_s (MHz)	2.5	2.5	2.5
V_{OUT} (V)	–5	–3.3	–1.8
L (μH)	2.2	2.2	2.2
V_{IN} (V)	12	12	12
$I_{L(max)}$ (A)	1.4	1.4	1.4
η	0.85	0.85	0.85
D	0.346	0.254	0.153
ΔI_L (mA)	755	554	335
$I_{L(avg)}$ (mA)	1023	1123	1233
I_{OUT} (mA)	669	838	1043

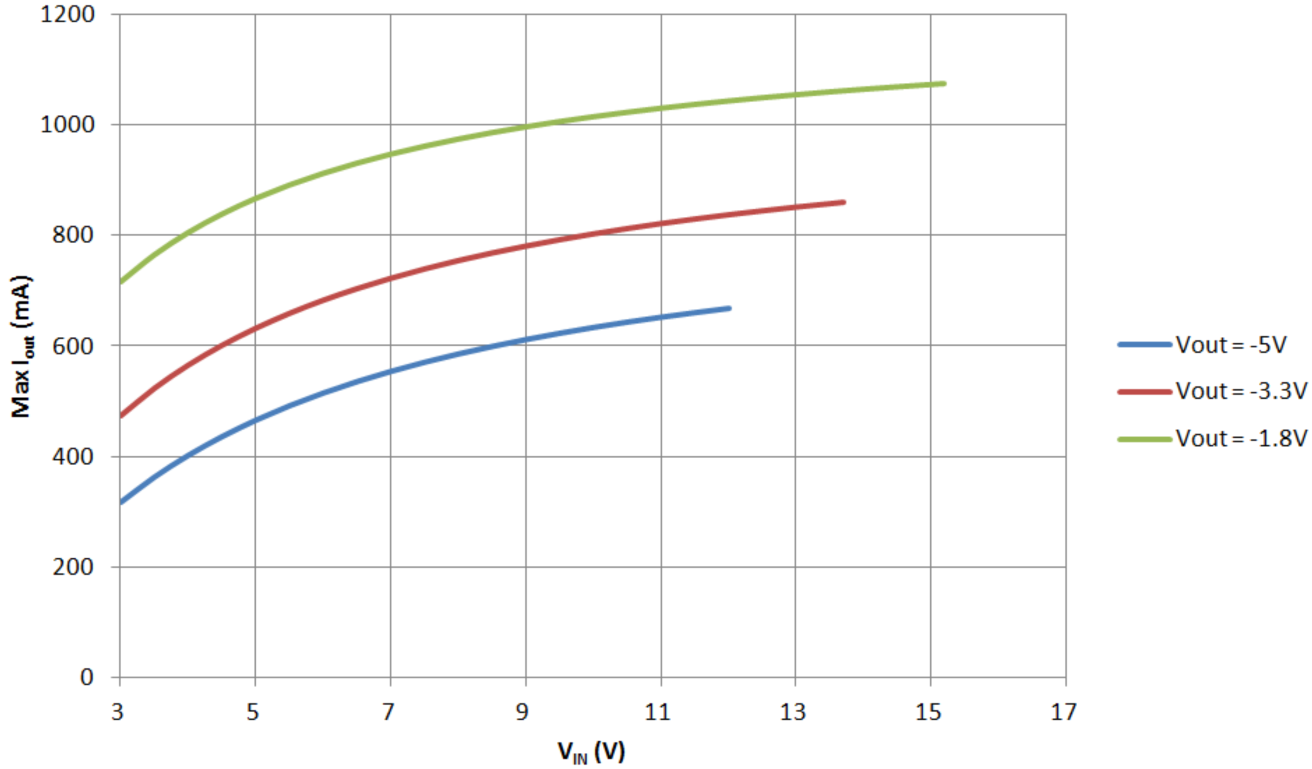


Figure 1-4. Maximum Output Current versus V_{IN}

1.3 V_{IN} and V_{OUT} Range

The input voltage that can be applied to an inverting buck-boost converter IC is less than the input voltage that can be applied to the same buck converter IC. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, not V_{IN} to ground. Thus, the input voltage range of the TPS6215x is 3V to 17 + V_{OUT}, where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but negative. The output voltage for the inverting buck-boost topology should be set between –0.9 V and –6 V. It is set the same way as in the buck configuration, with two resistors connected to the FB pin.

2 Design Considerations

2.1 Design Precautions

When using any of the TPS6213x/4x/5x/6x/7x converters for an inverting buck-boost application, there is a risk if the VIN and EN pins are connected together directly.

The inverting buck-boost is commonly used to power the negative side of a differential rail. If the positive rail is applied to this differential rail first, the downstream devices activate and their Iq charges a positive prebias voltage on the negative rail. Input brownout and quick power cycles are other scenarios that can prebias the negative rail and cause startup issues. With VIN/EN tied together and having a positive prebias on the output of inverting buck-boost, the device may enable before it has time to initialize internal circuitry which can cause unexpected startup behavior or cause the device to get stuck. Ensure that the EN pin is asserted after VIN is powered on would eliminate this issue robustly.

There are three proposed workarounds to avoid this issue:

The first suggestion is to adjust the system power up sequence to prevent the unintended voltage buildup on the negative rail. This means enabling the negative rail first so that it is able to start up correctly, then enabling the positive rail. Adjusting the power on sequence this way will ensure that the inverting buck-boost converter has a correct startup.

If the application relies on the device enabling with VIN, then an RC filter is required to add a delay between VIN and the EN pin. This ensures that the device has enough time to initialize the internal circuitry before the device is enabled to start regulating the output. The 100 kΩ and 1 µF RC filter provides the necessary delay between the VIN and EN pins for devices' initialization. An example of this schematic modification is shown in two different options, one using a series resistor to limit the current into the EN pin Figure 2-1 and another using a schottky diode to clamp the EN pin Figure 2-2. When using the Schottky diode option, the forward voltage drop should be selected less than 0.3 V so that the device doesn't exceed the absolute maximum rating on the EN pin.

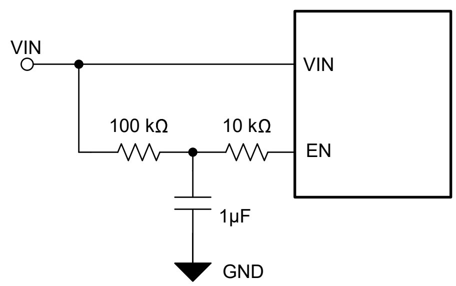


Figure 2-1. EN Pin Delay Using an RC Filter and Series Resistor

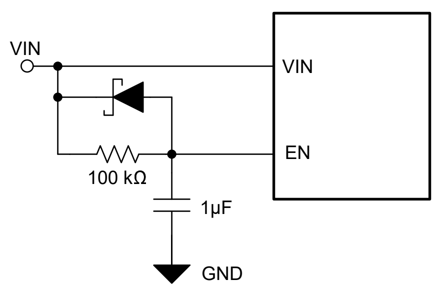


Figure 2-2. EN Pin Delay Using an RC Filter and Schottky Diode

Lastly, if the application requires enabling and disabling of the device from an external control signal, like a microcontroller or PG pin from an upstream device, then the order of power sequence is important. During power up, VIN must be applied before the EN signal and during power down, the EN pin should go low before VIN is removed. This ensures that the EN pin does not exceed the maximum rating of VIN + 0.3 V, which can damage the device. See Figure 2-4 for more information on level shifting the digital inputs.

2.2 Additional Input Capacitor

An additional input capacitor, C_{BYP}, is required for stability as a bypass capacitor for the device. This capacitor is in addition to the input capacitor, C_{IN}, from V_{IN} to ground (refer to Figure 1-2). The recommended minimum value for the bypass capacitor and the input capacitor is 10 µF.

As a side effect, the C_{BYP} capacitor provides an AC path from V_{IN} to V_{OUT}. When V_{IN} is applied to the circuit, this dV/dt across a capacitor from V_{IN} to V_{OUT} creates a current that must return to ground (the return of the input supply) to complete its loop. This current might flow through the internal low-side MOSFET's body diode and the inductor to return to ground. Flowing through the body diode pulls the SW pin and VOS pin more than 0.3 V below IC ground, violating their absolute maximum rating. Such a condition might damage the device and is not recommended. Therefore, a Schottky diode should be installed on the output, per Figure 2-3. Startup testing should be conducted to ensure that the VOS pin is not driven more than 0.3 V below IC ground when V_{IN} is applied.

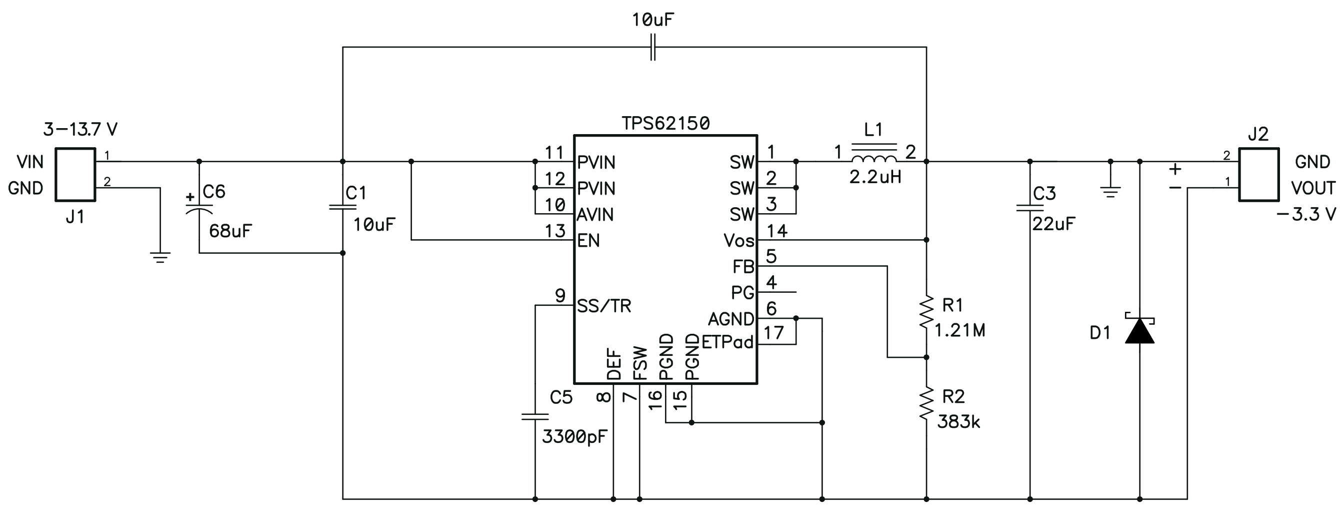


Figure 2-3. TPS62150 Inverting Buck-boost Schematic with Schottky D1

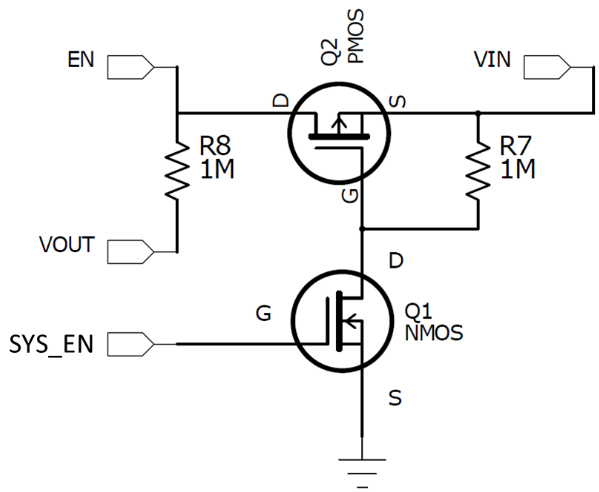
The AC path through C_{BYP} might also worsen the line transient response. If strong line transients are expected, the output capacitance should be increased to keep the output voltage within acceptable levels during the line transient.

2.3 Digital Pin Configurations

2.3.1 Digital Input Pins (EN, FSW, DEF)

Because V_{OUT} is the IC ground in this configuration, the EN pin must be referenced to V_{OUT} instead of the ground. In a buck configuration, the specified typical threshold voltage for the enable pin in the product data sheet is 0.9V to be considered high and 0.3V to be considered low (see the TPS62130, TPS62140, TPS62150, TPS62160, and TPS62170 product data sheets, Reference 2 through Reference 6). In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 0.9V + V_{OUT} and the low threshold is 0.3V + V_{OUT}. For example, if V_{OUT} = -3.3V, the V_{EN} is considered a high level for voltages above –2.4V and a low level for voltages below –3V. The same effect is true with the DEF and FSW pins.

This behavior can cause difficulties enabling or disabling the part, since in some applications, the IC providing the EN signal may not be able to produce negative voltages. The level shifter shown in Figure 2-4 alleviates any problems associated with the offset EN threshold voltages by eliminating the need for negative EN signals.



VOUT is the negative output voltage of the inverting buck-boost converter

Figure 2-4. EN Pin Level Shifter

The positive signal that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN grounded), Q2 sees 0V across its V_{GS}, and also remains off. In this state, the EN pin sees V_{OUT} which is below the low level threshold and disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (minimum V_{GS} as specified in the MOSFET's data sheet), the gate of Q2 is pulled low through Q1. This drives the V_{GS} of Q2 negative and turns Q2 on. As a consequence, V_{IN} ties to EN through Q2 and the pin is above the high level threshold, causing the device to turn on. Ensure that the V_{GD} of Q2 remains within the MOSFET's ratings during both enabled and disabled states. Failing to adhere to this constraint can result in damaged MOSFETs.

The enable and disable sequence is illustrated in Figure 2-5 and Figure 2-6. The SYS_EN signal activates the enable circuit, and the G/D NODE signal represents the shared node between Q1 and Q2. The EN signal is the output of the circuit and goes from VIN to –VOUT properly enabling and disabling the device. An active discharge circuit was implemented to accelerate –V_{OUT}'s return to 0V when the IC is disabled.

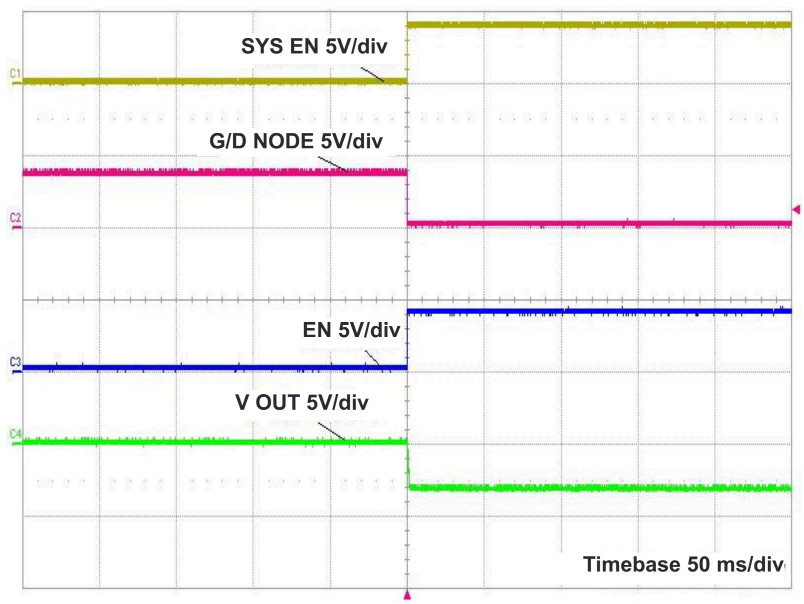


Figure 2-5. EN Pin Level Shifter on Startup

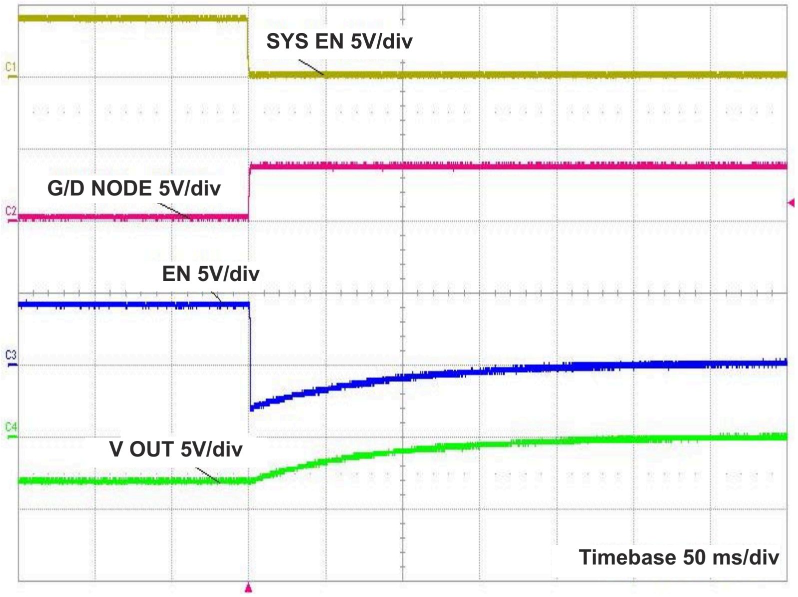


Figure 2-6. EN Pin Level Shifter on Shutdown

2.3.2 Power Good Pin

These devices have a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because V_{OUT} is the IC ground in this configuration, the PG pin is referenced to V_{OUT} instead of ground, which means that the device pulls PG to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin may not be able to withstand negative voltages. The level shifter circuit shown in Figure 2-7 alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it may be left floating or connected to V_{OUT} without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin should not be driven more than 7 V above the negative output voltage (IC ground).

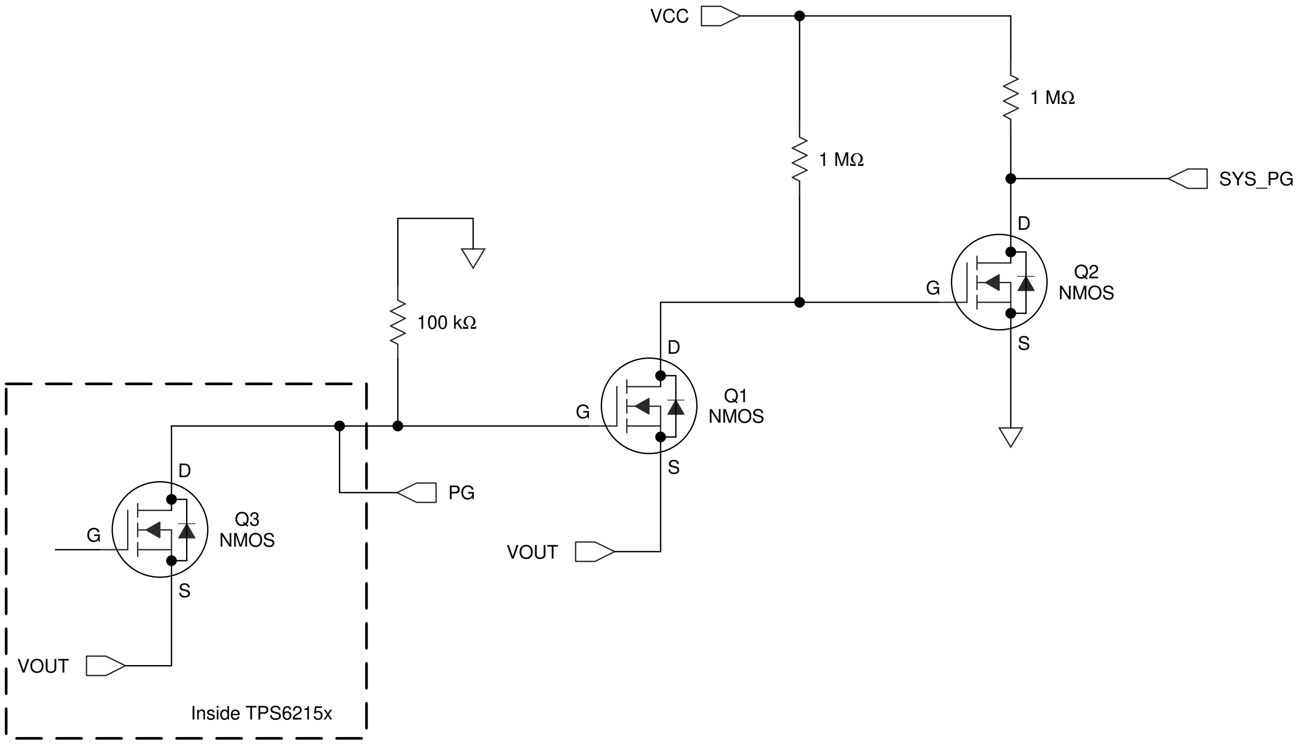


Figure 2-7. PG Pin Level Shifter

Inside these devices, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is off and Q2 is on because its V_{GS} sees V_{CC}. SYS_PG is then pulled to ground.

When Q3 turns off, the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PG is then pulled up to the V_{CC} voltage. Note that the V_{CC} voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG net.

This PG pin level shifter sequence is illustrated in Figure 2-8 and Figure 2-9. The PG signal activates the PG pin level shifter circuit, and the GD Node signal represents the shared node between Q1 and Q2. This circuit was tested with a V_{CC} of 1.8 V and dual NFET Si1902DL. The SYS_PG net is the output of the circuit and goes between ground and 1.8 V, and is easily read by a separate device.

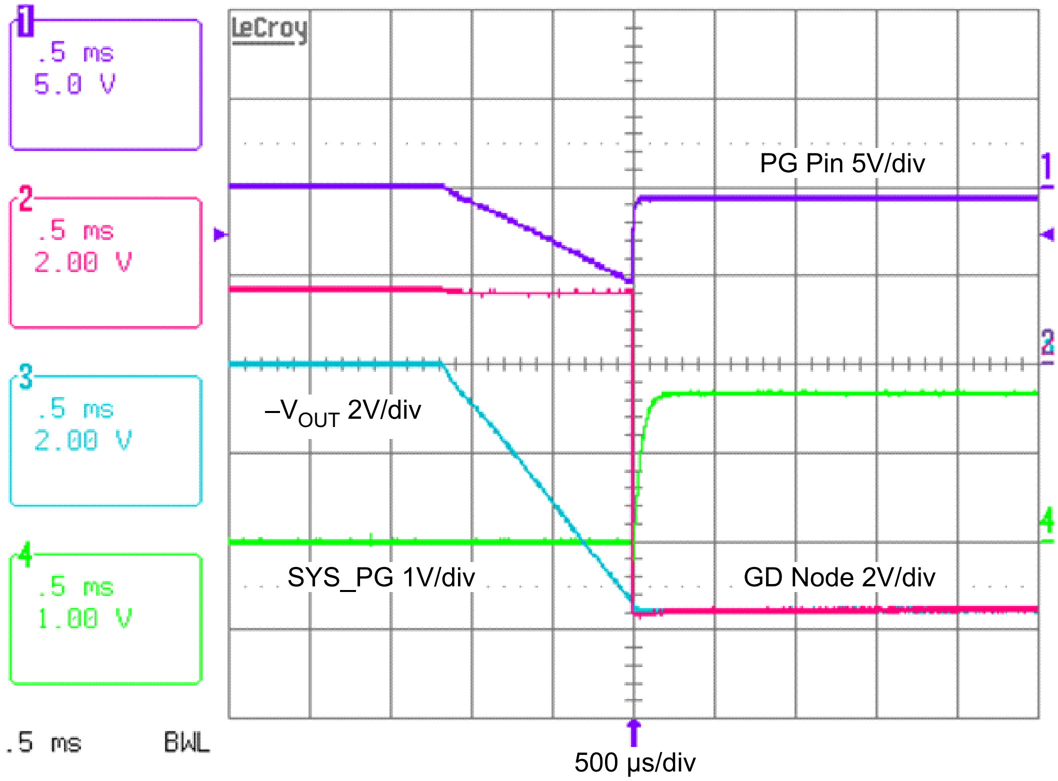


Figure 2-8. PG Pin Level Shifter on Startup

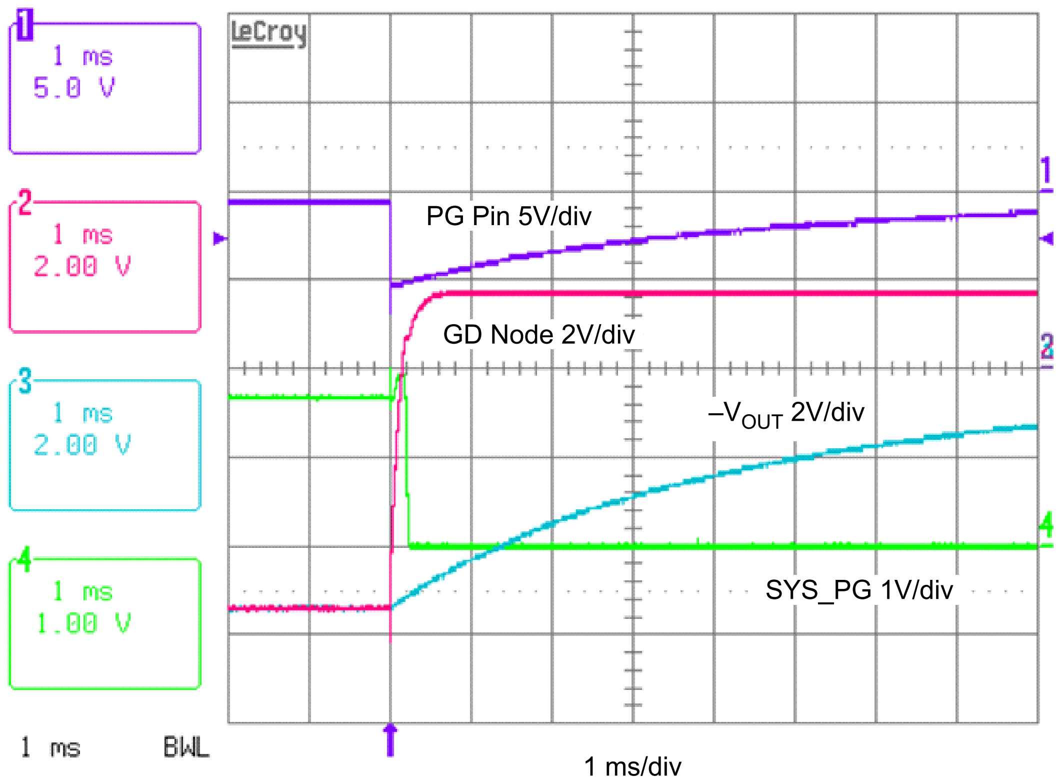


Figure 2-9. PG Pin Level Shifter on Shutdown

2.4 Startup Behavior and Switching Node Consideration

In the inverting buck-boost topology, the voltage on the SW pin switches from V_{IN} to V_{OUT}, instead of from V_{IN} to GND. As the high-side MOSFET turns on, the SW node sees the input voltage; as the low-side MOSFET turns on, the SW node sees the device ground, which is the output voltage. During startup, V_{IN} rises to achieve the desired input voltage. V_{OUT} starts ramping down after the EN pin voltage exceeds its threshold level and V_{IN} exceeds its UVLO threshold. As V_{OUT} continues to ramp down, the SW node low level follows it down. Figure 2-10 shows the resulting normal and smooth startup of the output voltage.

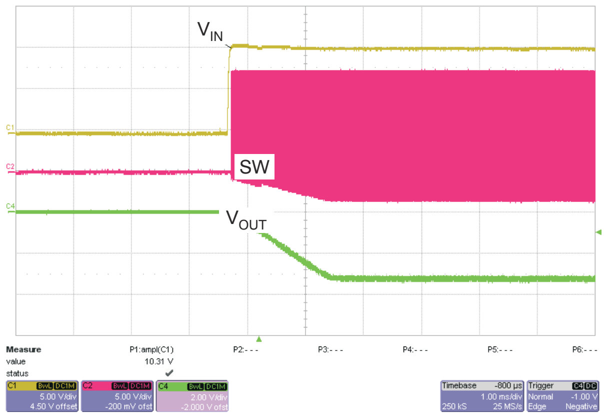


Figure 2-10. SW Node Voltage During Startup

3 External Component Selection

The inductor and output capacitor must both be selected based on the needs of the application and the stability criteria of the device, which are different from the traditional buck converter approach. A load transient test should be performed to evaluate stability. Figure 4-9 shows the results of such a test performed on the example circuit. The lack of ringing indicates stability.

3.1 Inductor Selection

To select the inductor value for the inverting buck-boost topology, use Equation 1 through Equation 4 instead of the equations provided in the TPS62150 data sheet. These formulas help to select the proper inductance by designing for a maximum inductor current ($I_{L(Max)}$) or finding the peak inductor current for a given inductance. $I_{L(Max)}$ should be kept below the device minimum current limit value for a reliable design. The worst-case $I_{L(Max)}$ occurs at the minimum V_{IN} for a given design.

Once $I_{L(Max)}$ is determined, it is recommended to choose an inductor with a saturation rating 20% to 30% higher than $I_{L(Max)}$ to allow for peak currents that may occur during startup or load transients. For the inverting buck-boost topology, the minimum recommended inductance is 2.2 µH. If more efficient, half-frequency operation is desired (FSW = high), then a 3.3-µH inductor is the recommended minimum value. The FSW pin should be connected to ground to set it to a logic high.

3.2 Capacitor Selection

Tiny ceramic capacitors with low equivalent series resistance (ESR) are desired to have low output voltage ripple. X5R- or X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics. A minimum 10-µF capacitor is recommended for both C_{BYP} and C_{IN}. These capacitance values can be increased without limit. For the output capacitor, a minimum of 22 µF is recommended. Making this capacitor value too great can cause instability. This situation can be evaluated through a Bode plot or load transient response. The voltage rating of C_{BYP} must be greater than (V_{IN} + V_{OUT}).

4 Typical Performance

The reference design shown in Figure 4-1 was used to generate the typical characteristic graphs presented in this section and illustrated in Figure 4-2 through Figure 4-10.

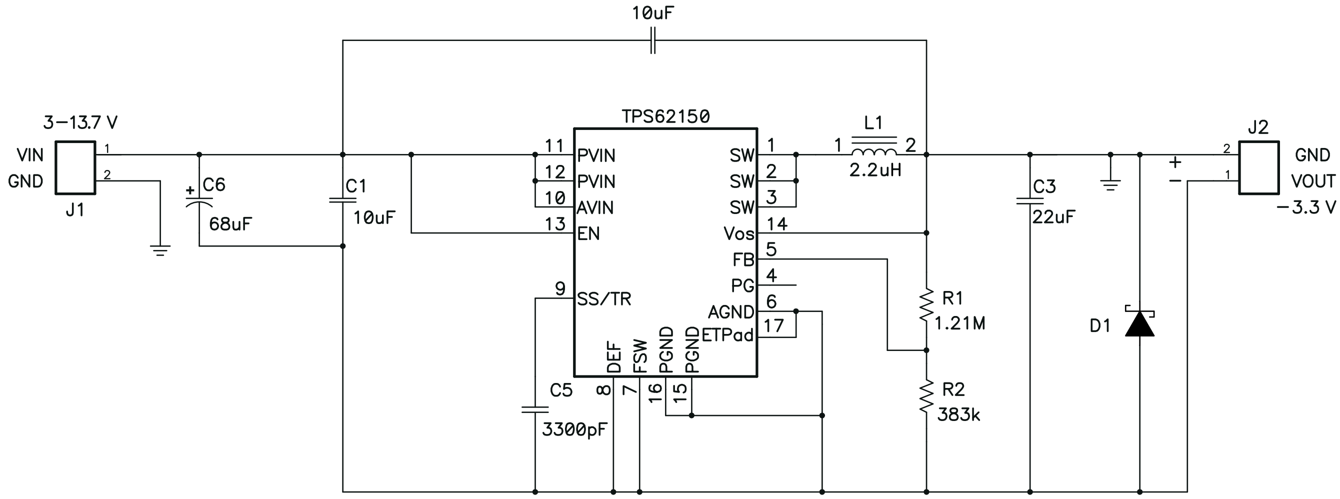


Figure 4-1. Schematic of the Tested Circuit

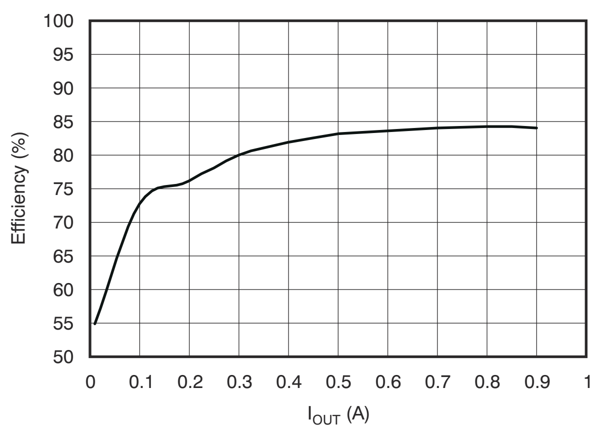


Figure 4-2. Efficiency vs Load Current with V_{IN} = 12 V

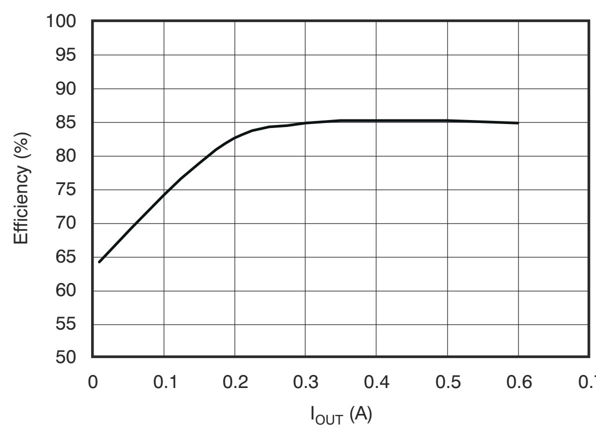


Figure 4-3. Efficiency vs Load Current with V_{IN} = 5 V

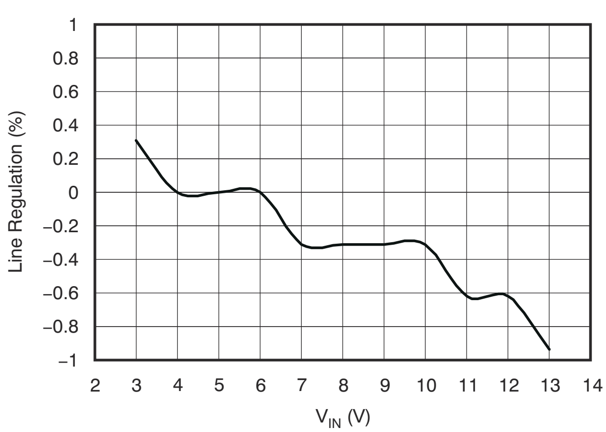


Figure 4-4. Line Regulation at 500-mA Load

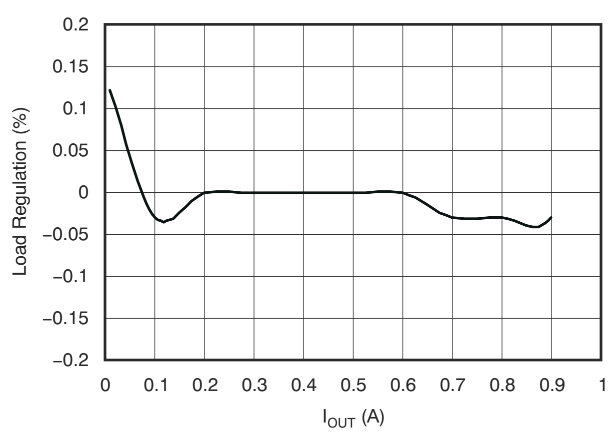


Figure 4-5. Load Regulation at V_{IN} = 12 V

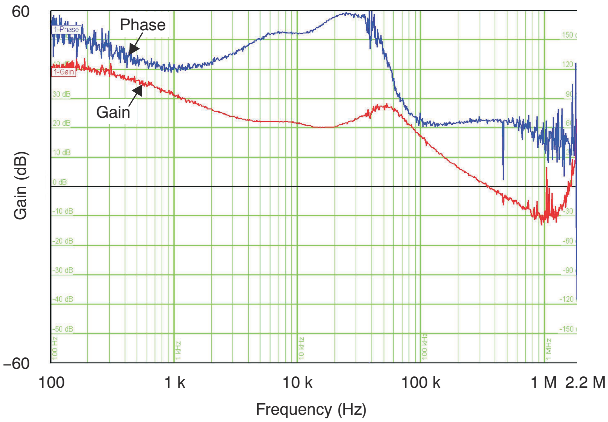


Figure 4-6. Bode Plot at V_{IN} = 12 V and 500-mA Load

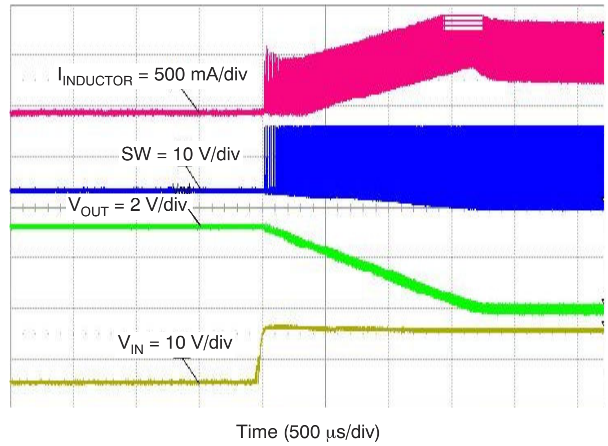


Figure 4-7. Startup on V_{IN} at 160-mA Load

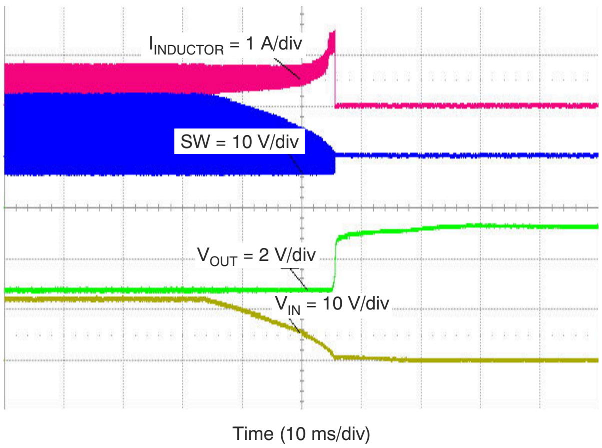


Figure 4-8. Shutdown on V_{IN} at 500-mA Load

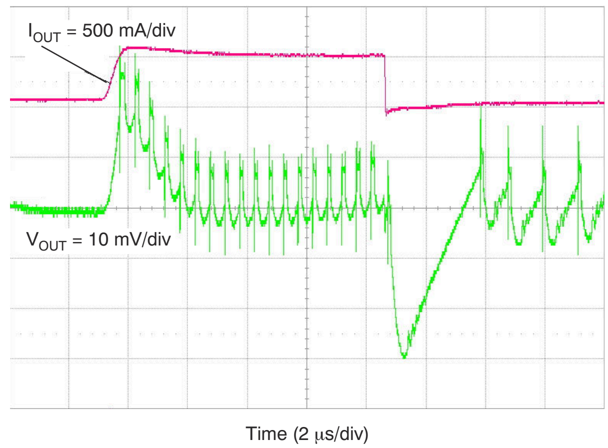


Figure 4-9. Load Transient Response, 0 mA to 500 mA with V_{IN} = 12V

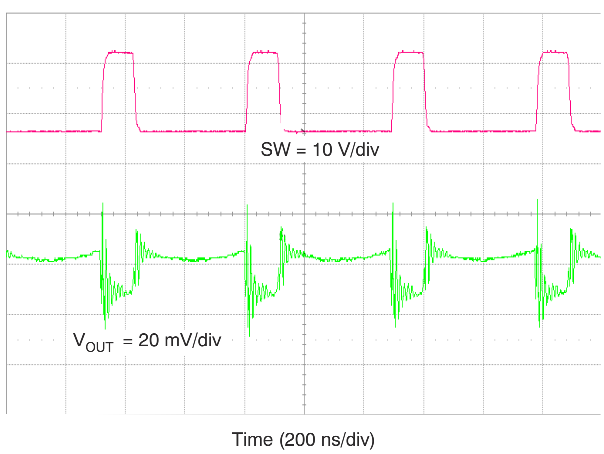


Figure 4-10. Output Voltage Ripple, V_{IN} = 12 V and I_{OUT} = 500 mA

5 Conclusion

The TPS6215x buck dc-to-dc converter can be configured as an inverting buck-boost converter to generate a negative output voltage. The inverting buck-boost topology changes some system characteristics, such as input voltage range and maximum output current. This application report explains the inverting buck-boost topology and how to select the proper values of external components with the changed system characteristics. It also gives design guidelines and precautions to ensure the robust operation of the converter. Measured data from the example design are provided. This application report also applies to any of the devices in the TPS6213x/4x/5x/6x/7x families.

6 References

The following documents are available for download from the TI web site:

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2. TPS62130 product data sheet. Literature number SLVSAG7.
3. TPS62140 product data sheet. Literature number SLVSAJ0.
4. TPS62150 product data sheet. Literature number SLVSAL5.
5. TPS62160 product data sheet. Literature number SLVSAM2.
6. TPS62170 product data sheet. Literature number SLVSAT8.
7. Tucker, J. (2007). *Using a buck converter in an inverting buck-boost topology*. Technical brief SLYT286.
8. Tucker, J. (2007). *Using the TPS5430 as an inverting buck-boost converter*. Application report SLVA257.
9. DCS-Control™ Landing Page: www.ti.com/dcs-control

7 Revision History

Changes from Revision C (June 2013) to Revision D (January 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *Design Precautions* section	7

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