Application Report
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TI ESD Protection Devices and the HDMI CTS

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ABSTRACT

HDMI compliance testing of the HDMI Transmitter port can be impacted by the addition of ESD protection devices. Texas Instrument's electrostatic discharge (ESD) protection devices for the HDMI transmitter port are designed to pass the HDMI Compliance Test Specifications (CTS) for HDMI1.4b or HDMI2.0. This application report outlines the impact these devices have on the CTS. The reader should note that in order to comply with the HDMI2.0 CTS, the design must also be in compliance with the HDMI1.4b CTS.

Contents

1 Introduction

When designing in transient voltage suppression (TVS) for an HDMI Transmitter port, the designer needs to consider which ESD protection requirements need to be met as well as the impact of the TVS on the performance of the HDMI transmitter. Texas instruments' ESD protection devices for the HDMI transmitter port have been designed to meet the highest protection level standards specified for ESD by IEC 61000-4-2 while minimizing, and in some cases improving, the impact on meeting the HDMI1.4b CTS and HDMI2.0 CTS. Texas Instruments is an HDMI Adopter, and as such strives to meet or exceed the specifications outlined in the most current HDMI specifications.

2 HDMI1.4b CTS

The HDMI1.4b CTS tests relevant to TI ESD protection devices are listed within this section. ESD protection for the TMDS lines impacts signal integrity. This impact has been characterized by the use of examples related to the specific Test ID. The impact on the DDC and CEC control lines and test procedures are also outlined.

2.1 Test ID 7-4: TMDS – TRISE, TFALL

The capacitance of ESD protection devices impacts propagation delay as well as rise times (t_r) and fall times (t_f). By increasing the time constant, *tau* (τ) = RC, both t_r and t_f increase. For example, in Figure 1, the 20%–80% rise and fall times of an HDMI output signal and the same signal loaded with 0.8 pF are 48.8 ps and 55.87 ps, respectively.

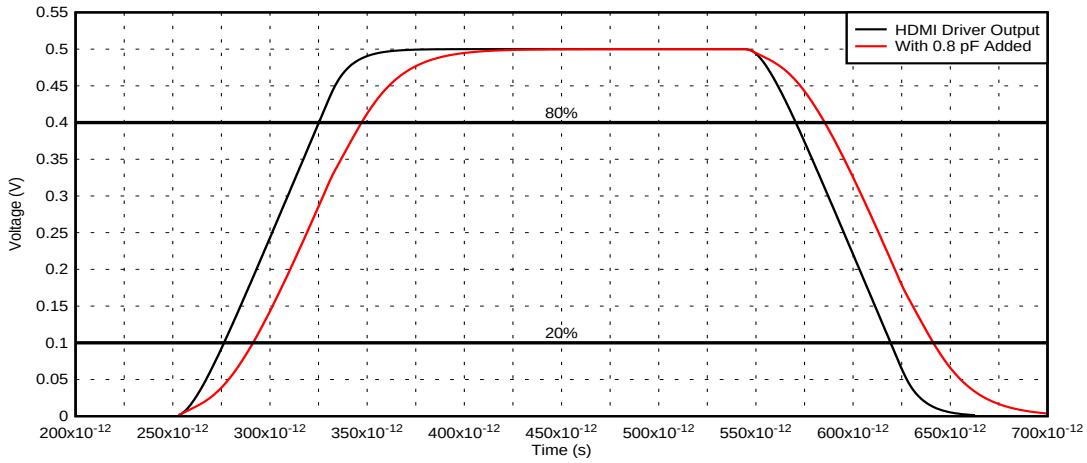

Figure 1. Change in t_r and t_f by a Capacitive Load

TI ESD protection devices are designed to add as little to the system's capacitance budget as possible, while still providing ESD protection levels that, in most cases, meet or exceed IEC 61000-4-2 Level 4 ESD protection levels of ±8-kV Contact and ±15-kV Air-Gap ratings.

2.2 Test ID 7-6: TMDS – Inter-Pair Skew

Inter-pair skew is the difference in time a differential signal propagates through any TMDS line, when compared to any of the remaining TMDS pairs; for both low to high and high to low transitions. ESD protection devices can effect this specification in two different ways: By having different lengths in the electrical path between any input to output pins and by having different phase delays between propagating signals due to a different RC constant. In Figure 2, TMDS pair 1 and TMDS pair 2 have a difference in propagation delay caused by a difference in electrical lengths of 15 ps, resulting in 15 ps of skew. Figure 3 shows the skew caused by different phase delays.

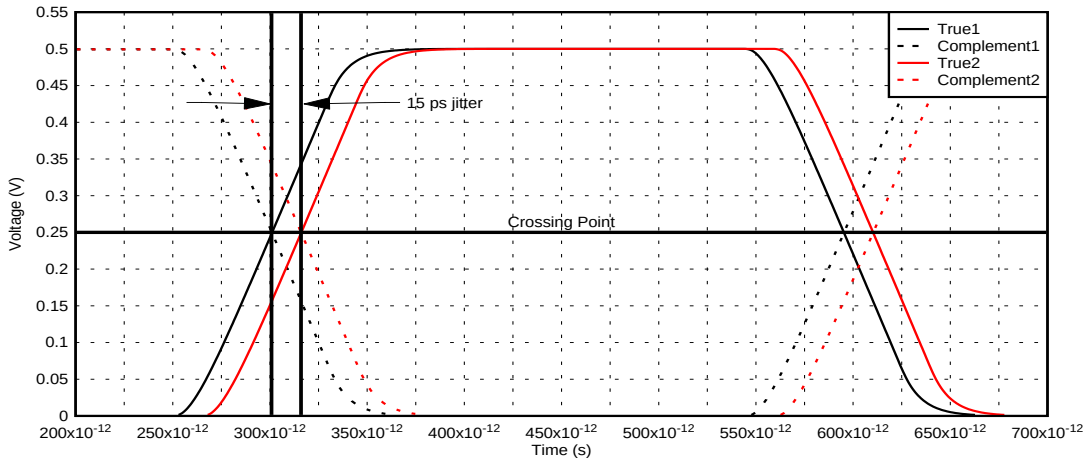

Figure 2. Inter-Pair Skew From Different Electrical Lengths

Differences in electrical lengths for any TI ESD protection device designed to protect the HDMI TMDS lines predominately do not need to be considered. This is due to the single protection pin approach for providing a parallel path to ground for ESD. Differences in phase delays (which, in turn, causes propagation delays) for any of TI's multi-channel ESD protection devices are tightly controlled by utilizing monolithic integrated circuit technology to ensure there is excellent capacitance matching between any two protection pins. For TI ESD protection devices with separate input and output pins for the TMDS lines, differences in electrical lengths are minimized by design, as well as specified in the data sheet.

2.3 Test ID 7-7: TMDS – Intra-Pair Skew

Intra-pair skew is the difference in time the true and complement signals propagate within any one of the four TMDS pairs, for both low to high and high to low transitions.

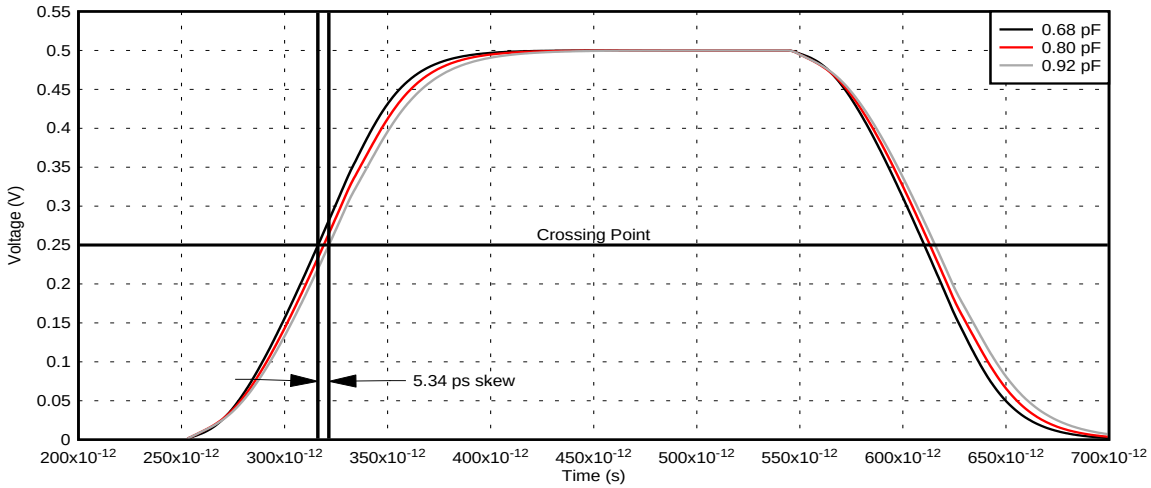

Figure 3. Skew Added by t_r and Phase Delay Change From a 15% Capacitance Variation

ESD protection devices effect this measurement identically to the inter-pair skew tested in Test ID 7-6 discussed previously, with the only difference being a smaller allowable skew. Figure 3 shows one signal in a TMDS pair with a 5.34 ps skew caused by varying the load capacitance ±15%. The change in capacitance effects the t_r, t_f, and propagation delay of the signal.

2.4 Test ID 7-9: TMDS – Clock Jitter

Clock jitter is defined as timing variations of the signal edges from their ideal values. The cause of these timing variations has many sources. Jitter can be caused by, to name a few, a varying frequency of the TMDS clock; signal skews based on differences in t_r, t_f; capacitance variations causing skews in propagation delays; noise coupling; reflections from impedance mismatches; crosstalk; or any mixture of these.

ESD protection devices primarily impact this test by causing differences in t_r, t_f, and inter and intra-pair skews as described in the preceding sections. The designer need only consider the impact TI ESD protection devices have on those tests in order to address their impact on clock jitter. The relationship between clock jitter and data jitter is specified only indirectly by the Test ID 7-10: TMDS –Data Eye Diagram tests discussed in Section 2.5.

Figure 4 shows the jitter caused by a 10 ps difference in propagation delay between the true and complementary signals within a TMDS pair.

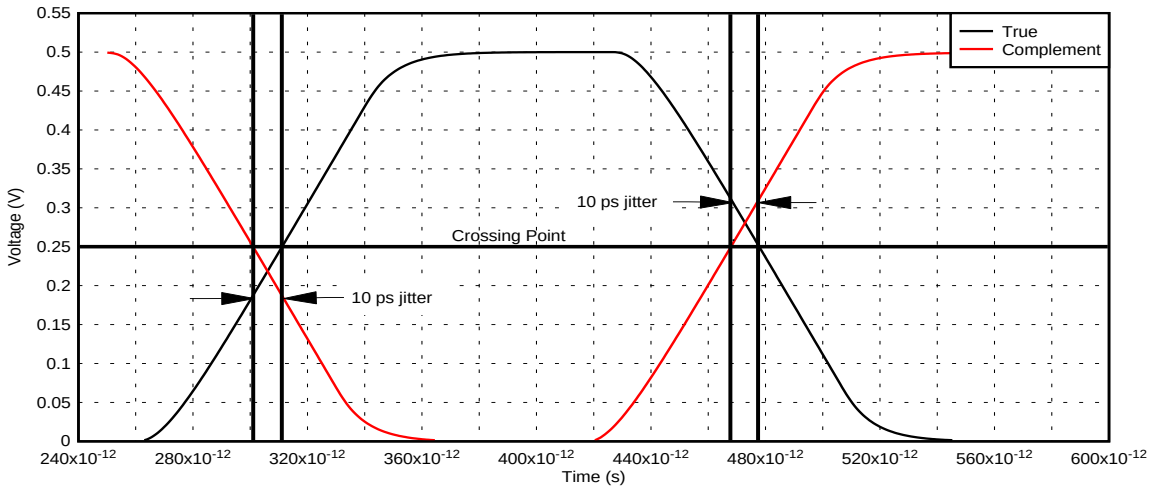

Figure 4. Jitter from Different Propagation Delays Within a TMDS Pair

2.5 Test ID 7-10: TMDS – Data Eye Diagram

Data Eye Diagrams conveniently display all of the t_r, t_f, and inter and intra-pair skews, all in one easy to discern test. Additional to the specifications impacted by an ESD protection device, the Data Eye Diagram displays minimum and maximum voltage level specifications as well. In the HDMI1.4b Specification, t_r and t_f are only specified for the minimum times. Maximum times for these specifications are not directly specified due to the Data Eye Diagram Mask's implied definition. If t_r and t_f are fast enough to avoid the minimum eye opening, then the t_r and t_f specifications are satisfied. Combining this consideration along with those for t_r, t_f, and inter and intra-pair skews, the designer can properly predict the impact an ESD protection device will have on the overall signal integrity of the system.

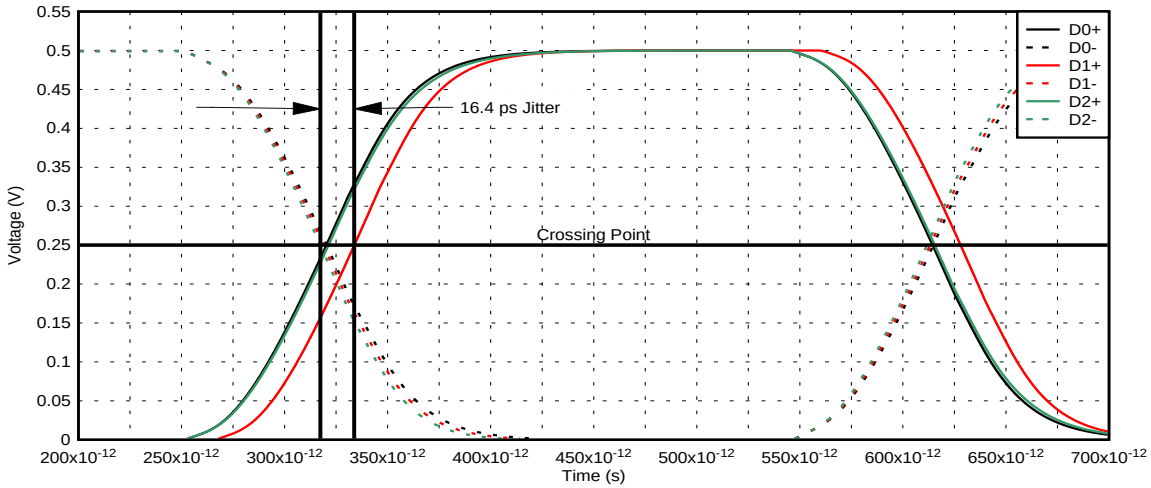

Figure 5. Data TMDS Signals with Previous Skews Combined

In Figure 5, one bit for each of the three TMDS data channels is graphed. Each of the three TMDS lines has some variation as shown in the previous sections. TMDS line D0 has a 0.85-pF load on both signal lines. TMDS line D1 has a 0.80-pF load on both lines, with the addition of D1+ also having a 10-ps propagation delay due to a longer electrical length. TMDS line D2 has 0.92-pF load on D2+ and 0.68-pF load on the D2- line. The total jitter caused is 16.4 ps.

In Figure 6 a Data Eye Diagram was simulated with the same variations used in Figure 5. Additionally, a 1% Gaussian pixel clock jitter has been added from the transmitter on a 9-bit pseudo-random bit sequence (PRBS) signal pattern. All three data TMDS line Eye Diagrams are over-layed onto the same graph. Blue is D2, green is D1. D0, purple, is hidden behind the two. In this case the total jitter is 33.3 ps.

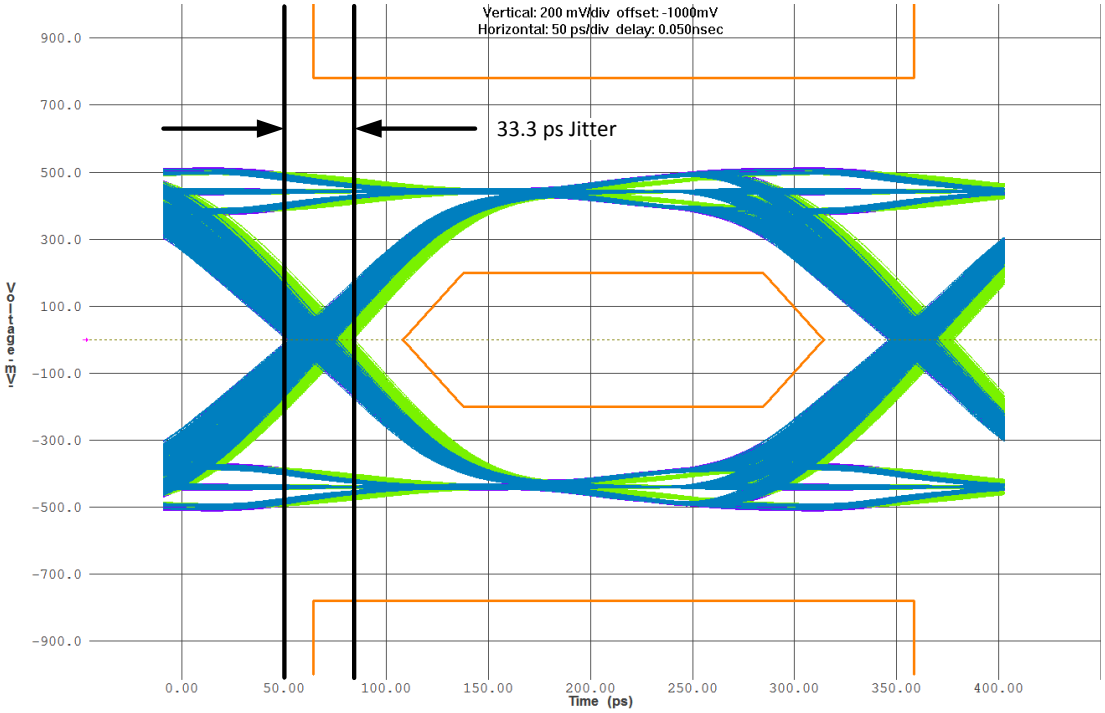

Figure 6. Three TMDS Data Eye Diagrams Combined

2.6 Test ID 7-13: TMDS – DDC/CEC Capacitance and Voltage

The Display Data Channel (DDC) and Consumer Electronics Control (CEC) capacitances are tested with the system powered-off and powered-on. In both cases, a capacitance requirement is specified for the capacitance which is parallel to ground (C_P). The voltage tests check for proper pull-up resistor values on DDC and CEC. For TI ESD protection devices that have an input pin and an output pin for DDC and CEC, the correct pull-up values are included in the design. For TI ESD protection devices with a single pin for each DDC and CEC line, the pull-up resistors for the HDMI transmitter source are tested.

When testing capacitance for TI ESD protection devices with a single pin for each DDC and CEC line, the added C_P is specified in the data sheet and is designed to be only a small part of the overall capacitance budget specified in this compliance test.

When testing capacitance using TI ESD protection devices that have both an input pin and an output pin for the DDC and CEC lines, during powered-on tests the device needs to be fully powered, with the connector side hot-plug detect (HPD) pin set to 0 V (grounded). The ESD protection device's level-shifter enable and load-switch enable pins (where applicable) should be set to 0 V as well, which is the typical control set for when no sink is attached. For powered-off tests, the device should have all power pins, level-shifter enable pins and load-switch enable pins (where applicable) set to 0 V.

2.7 Test ID 7-15: CEC Line Degradation

When the HDMI transmitter is powered off or on, the CEC line should not sink enough current to lower the voltage levels below specification on the CEC bus of any and all devices it is attached to.

TI ESD protection devices with a single protection pin for the CEC line are designed to have ultra-low leakage current, which is orders of magnitude below the maximum current allowed in this CEC test. Therefore, TI ESD protection devices with a single protection pin have a very minimal impact on this test.

TI ESD protection devices that have an input pin and output pin for CEC are either designed to buffer the HDMI core chip with high impedance while powered either off or on, or use an open-drain nFET for dual-supply level translation. In either case, passing the CEC Line Degradation test is designed into the TI ESD protection device.

3 HDMI2.0 CTS

The HDMI2.0 CTS tests related to TI ESD protection devices for the HDMI transmitter port also include all of the previous tests listed in the HDMI1.4b CTS section. Most of the following HDMI2.0 CTS tests listed are repetitions of the previous HDMI1.4b CTS tests with the exception of being ran at the faster data rate of 6 Gbps. They are listed here only to make the list complete, the effects of TI ESD protection devices are the same as the similar tests already described in the HDMI1.4b CTS section. The newly added test, HF1-9: Source Electrical – 6G – Differential impedance, will be discussed.

3.1 HF1-2: Source TMDS Electrical – 6G – TRISE, TFALL

This test is identical in scope to the HDMI1.4b Test ID 7-4, with faster rise and fall time specifications allowed. The designer needs to apply the same considerations here as in the previous test.

3.2 HF1-3: Source TMDS Electrical – 6G – Inter-Pair Skew

This test is identical in scope to the HDMI1.4b Test ID 7-6. The designer needs to apply the same considerations here as in the previous test.

3.3 HF1-4: Source TMDS Electrical – 6G – Intra-Pair Skew

This test is identical in scope to the HDMI1.4b Test ID 7-7. The designer needs to apply the same considerations here as in the previous test.

3.4 HF1-7: Source TMDS Electrical – 6G – Clock Jitter

This test is identical in scope to the HDMI1.4b Test ID 7-9. The designer needs to apply the same considerations here as in the previous test.

3.5 HF1-8: Source TMDS Electrical – 6G – Data Eye Diagram

This test is identical in scope to the HDMI1.4b Test ID 7-10. The designer needs to apply the same considerations here as in the previous test.

3.6 HF1-9: Source Electrical – 6G – Differential impedance

The HDMI1.4b CTS defines the maximum allowable variation in differential impedance for the sink-side TMDS lines. The HDMI2.0 CTS has been updated to include this test for the source-side TMDS lines as well. Differential impedance is measured with a time domain reflectometer (TDR). It maps the impedance of the signal path against time, or distance when considering the propagation velocity of the signal. In an impedance controlled environment, adding capacitance between a signal line and ground will cause the impedance value to become smaller in the vicinity of the added capacitance. Any additional series inductance will cause the impedance to increase in the vicinity of the inductance.

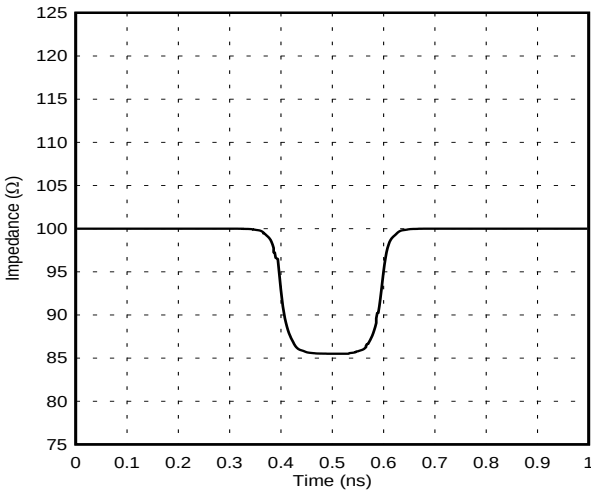

Figure 7. 192 ps t_r TDR of 0.6 pF Capacitance

Figure 7 shows a simulated TDR graph of a 100-Ω differential line loaded with 0.6 pF of capacitance. The rise time of the TDR used is 192 ps.

The effect of a change in impedance on a voltage-varying signal propagating down a line with an electrical length longer than 1/10th of the wavelength of the varying signal is to reflect back some voltage towards the source, of which some voltage can then reflect back again if there is another change in impedance. This back and forth reflection will continue through the line wherever there are any impedance mismatches. Depending on the distance between the impedance mismatches, the signal may be attenuated or amplified due to any part of the signal that has been reflected back and forth being added to the signal propagating down the line. If the impedance mismatches are big enough, then these reflections can change the voltage levels of the signal outside the receivers input logic levels, leading to a loss of data.

Typically, any ESD protection device will add a capacitive load to ground on the signal line being protected. TI ESD protection devices are designed to add as little to the system's capacitance budget as possible, while still affording ESD protection levels that, in most cases, meet or exceed IEC 61000-4-2 Level 4 ESD protection levels of ±8-kV Contact and ±15-kV Air-Gap ratings.

4 Conclusion

Designing ESD protection into a high-speed HDMI transmitter port can be successful with a proper TVS selected. TI ESD protection devices for the HDMI transmitter port are each designed to meet the HDMI 1.4b and/or the HDMI2.0 specifications. Any TI ESD protection device for the HDMI transmitter port lists which HDMI specification it meets in its respective data sheet. Texas Instrument's considerations for these compliance tests during the design process of an HDMI related ESD protection device will help ensure a designer's system is compliant with the targeted HDMI specification.

5 Related Documentation

The documents identified in this section are referenced within this document. Most references within the document use the text identified within the brackets [Document Tag], instead of the complete document title to simplify the text.

(a) [HDMI1.4b] High-Definition Multimedia Interface Specification Version 1.4b, October, 2011

(b) [HDMI2.0] High-Definition Multimedia Interface Specification Version 2.0a, March, 2015

(c) [HDMI1.4b CTS] High-definition Multimedia Interface CTS for Version 1.4b October, 2011

(d) [HDMI2.0 CTS] High-definition Multimedia Interface CTS for Version 2.0k June, 2015

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