

Adjusting the Output Voltage of a Fixed Output Voltage DC-DC Converter



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ABSTRACT

Fixed output voltage converters like TPS6287x generate an accurate output voltage with tight tolerance and temperature drift. This is hardly achievable with a DC-DC converter having an adjustable output voltage which is set by a resistor divider. The tolerance of the resistors of the feedback divider and the temperature drift of the resistors significantly affect the accuracy. At converters having a fixed output voltage the output voltage usually cannot be changed unless a digital interface is available and supports that. This is possible with devices of the TPS6287x family if the interface can be used to adjust the voltage if needed. If no interface is available at the time the change is needed there is a possible workaround which is described in this application note in detail.

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1 Introduction

At converters having a fixed output voltage, the output voltage usually cannot be configured in a simple way. Devices of the TPS6287x family support selecting a predefined output voltage using an appropriate configuration at the VSEL pin. If the desired output voltage cannot be selected using VSEL, the output voltage still can be programmed using the digital interface once the device is powered properly. This change can be done before the device is enabled. After enable, the device starts into the newly programmed output voltage. Additional details can be found in the [TPS6287x-Q1 2.7-V to 6-V Input, 6-A, 9-A, 12-A, 15-A, Automotive, Stackable, Synchronous Step-Down Converters with Fast Transient Response](#) data sheet.

If this process cannot be done, for example, if there is no interface communication possible since the host for the interface is not active before or during startup, other means of addressing that are required. This application note explains how this problem can be addressed using a resistor divider. This application note also explains the limitations of this approach.

2 Configuration

Figure 2-1 shows how this resistor divider must be connected. In the layout of the [TPS62873EVM-143](#) and [TPS62873EVM-144](#) footprints for those resistors are already provided.

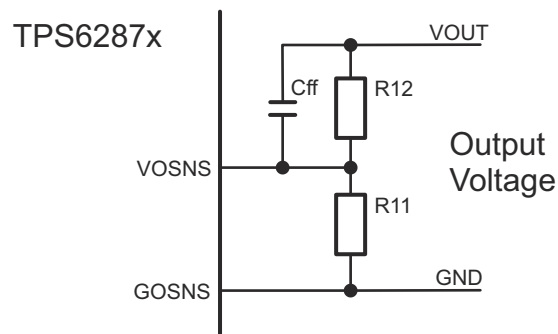


Figure 2-1. Resistor Divider

The output voltage then is defined by the fixed output voltage selected using VSEL and of course the values of the resistors used in this divider. Equation 1 shows how to calculate the output voltage.

$$V_{OUT} = V_{OUT_{fixed}} \cdot \left(\frac{R_{12} + R_{11}}{R_{11}} \right) \quad (1)$$

As Equation 1 shows, the fixed output voltage $V_{OUT_{fixed}}$ must be selected lower than the desired final output voltage.

The first obvious tradeoff of this approach is the loss of accuracy due to the tolerance of the resistor values and their temperature drift. This can be kept at a minimum by selecting a fixed output voltage version with an output voltage as close as possible to the desired final output voltage. The additional error for the minimum and the maximum output voltage of this configuration can be calculated using Equation 2 and Equation 3. An additional error is generated by the bias current flowing into the VOSNS pin. This bias current must flow through R12 which causes an increase of the output voltage. The resulting error can be kept negligible by using a low resistance value for R12. A resistor value in the range of 1 kΩ makes this error negligible for the TPS6287x devices.

$$V_{OUT_{min}} = V_{OUT_{fixed}} \cdot \left(1 - \Delta V_{OUT} \right) \cdot \left(\frac{R_{12} \cdot (1 - \Delta R_{12}) + R_{11} \cdot (1 + \Delta R_{11})}{R_{11} \cdot (1 + \Delta R_{11})} \right) \quad (2)$$

$$V_{OUT_{max}} = V_{OUT_{fixed}} \cdot \left(1 + \Delta V_{OUT} \right) \cdot \left(\frac{R_{12} \cdot (1 + \Delta R_{12}) + R_{11} \cdot (1 - \Delta R_{11})}{R_{11} \cdot (1 - \Delta R_{11})} \right) \quad (3)$$

Another important consideration is maintaining AC control performance. The resistors of the resistive divider, especially the upper resistor R12 in the VOSNS path, creates low pass filters together with parasitic capacitances at the VOSNS and GOSNS pins. To mitigate this effect a feed-forward capacitor Cff in parallel

to R12 can be added. Equation 4 shows how to estimate an appropriate value for this capacitor. f_{CO} in this equation is the expected crossover frequency of the control loop.

$$C_{ff} = \frac{2}{\pi \cdot f_{CO} \cdot R_{12}} \quad (4)$$

In case of the TPS6287x devices a total resistance in the range of 10 k Ω for the resistor divider and limiting the increase of the output voltage to a maximum of 20% is a good choice for getting negligible impact on the control performance.

If for example an output voltage of 1.2 V is needed, the TPS6287x-Q1 devices can be configured to a fixed output voltage of 1 V as described in the [TPS6287x-Q1 2.7-V to 6-V Input, 6-A, 9-A, 12-A, 15-A, Automotive, Stackable, Synchronous Step-Down Converters with Fast Transient Response](#) data sheet. With the recommendations and equations described above, an output voltage of 1.2 V can be configured with a resistive divider using 2 k Ω for R12 and 10 k Ω for R11. Assuming the resistor accuracy of both resistors is 1%, the accuracy of the output voltage changes from the initial +/- 1% specified for the 1 V fixed output voltage to +/- 1.3% which can be acceptable in most of the cases. Assuming a crossover frequency of 300 kHz, 1 nF is an appropriate value calculated for Cff for this configuration.

With the feedback divider, the voltages which can be set with the interface change as well. The default values defined in the registers scale with the gain of the feedback divider. Equation 5 shows how to calculate the new regulated output voltage for a dedicated voltage setting V_{OUT_Reg} in the VSET registers.

$$V_{OUT} = V_{OUT_Reg} \cdot \left(\frac{R_{12} + R_{11}}{R_{11}} \right) \quad (5)$$

If the feedback divider for example is designed to increase the output voltage by 20%, a programmed output voltage of 0.4 V in the VSET registers results in a regulated output voltage of 0.48 V.

3 Measurements

In the following, measurements are shown comparing the performance of an I2C programmed fixed output voltage converter with a configuration using a resistive divider to increase the output voltage. For the measurements, the [TPS62873 Buck Converter Evaluation Module User's Guide](#) was used. Both converters are configured for a default startup voltage of 1 V as described in the configuration example in the [Configuration](#) section. To implement this modification on the [TPS62873 Buck Converter Evaluation Module User's Guide](#), a 47 kΩ resistor is used for R5 and R6 is removed. The I2C version is reprogrammed to an output voltage of 1.2 V before startup, and the change of the output voltage in the adjustable version is done with a resistor divider using 10 kΩ for R11, 2 kΩ for R12 and 1 nF for Cff. For the higher output voltage, the components in the compensation network were changed to 1.5 kΩ for R1 and 3.9 nF for C1. All other components remained unchanged.

3.1 DC Regulation in PWM and Power Save Mode Operation

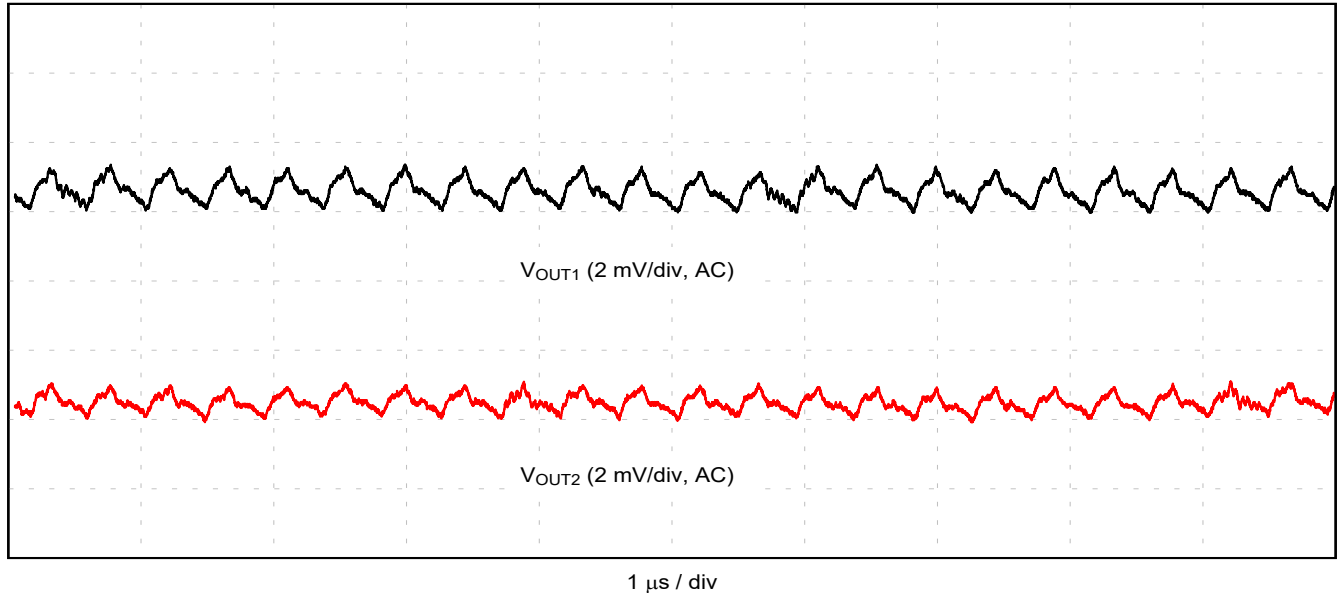


Figure 3-1. DC Regulation of the I2C and the Resistor Divider Version at 12 A Output Current

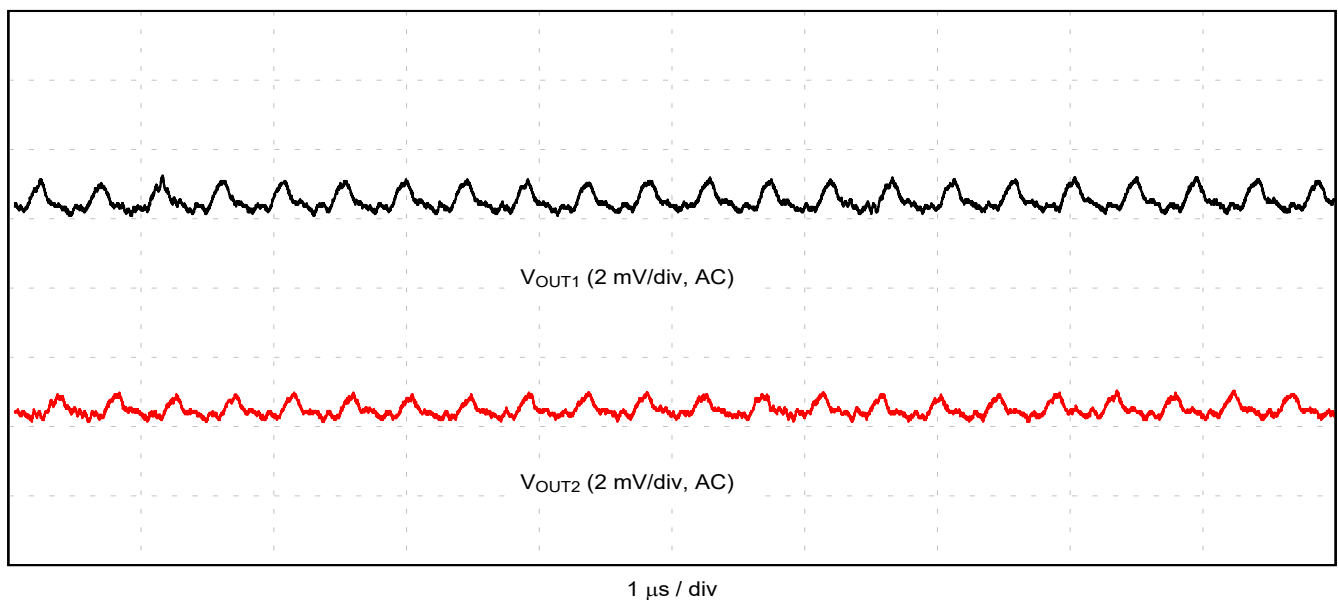


Figure 3-2. DC Regulation of the I2C and the Resistor Divider Version at 100 mA Output Current

Figure 3-1 and Figure 3-2 show output voltage ripple waveforms at different load conditions. Figure 3-1 shows the output voltage at 12 A load and Figure 3-2 shows the output voltage at 100 mA load. V_{OUT1} is the waveform of the I2C version and V_{OUT2} is the waveform of the resistor divider version. Both graphs show no significant difference in output voltage ripple at the different load conditions.

3.2 Transient Performance

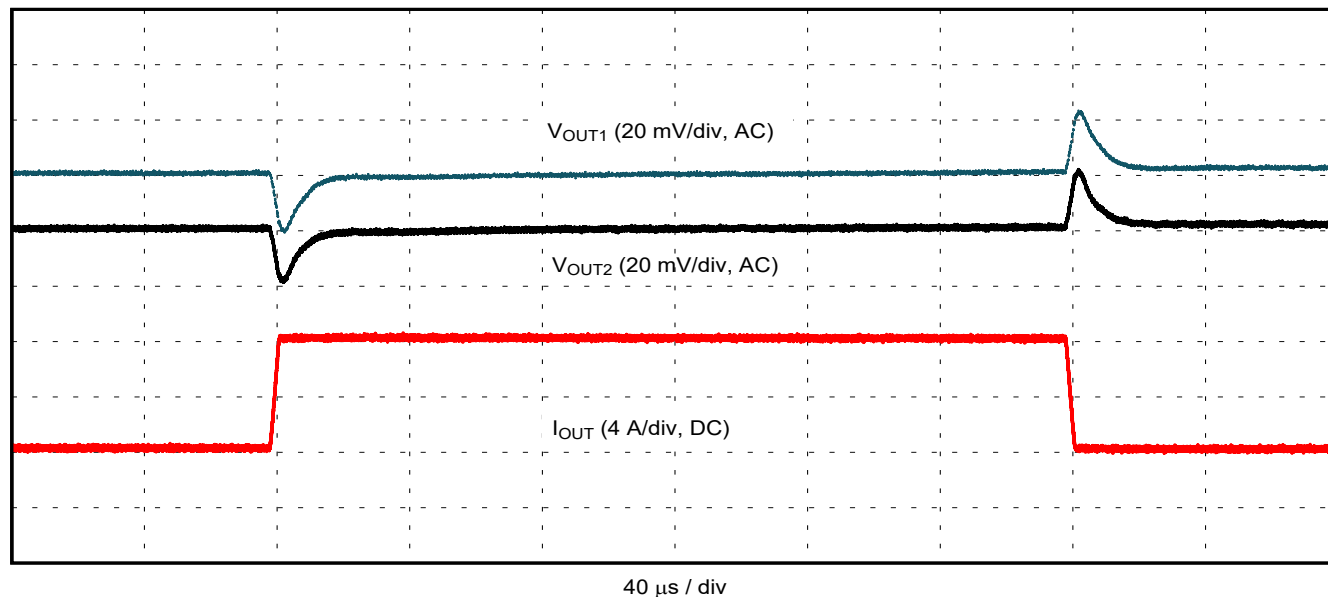


Figure 3-3. Load Transient of the I2C Version and Resistor Divider Version

Figure 3-3 shows the waveforms of a step response to a load increase from 4 A to 12 A and decrease to 4 A again. The current waveform is labeled I_{OUT} , the output voltage waveform of the I2C version is V_{OUT1} and the output voltage waveform of the resistor divider version is V_{OUT2} . Both output voltage waveforms show no difference.

3.3 Control Loop Gain

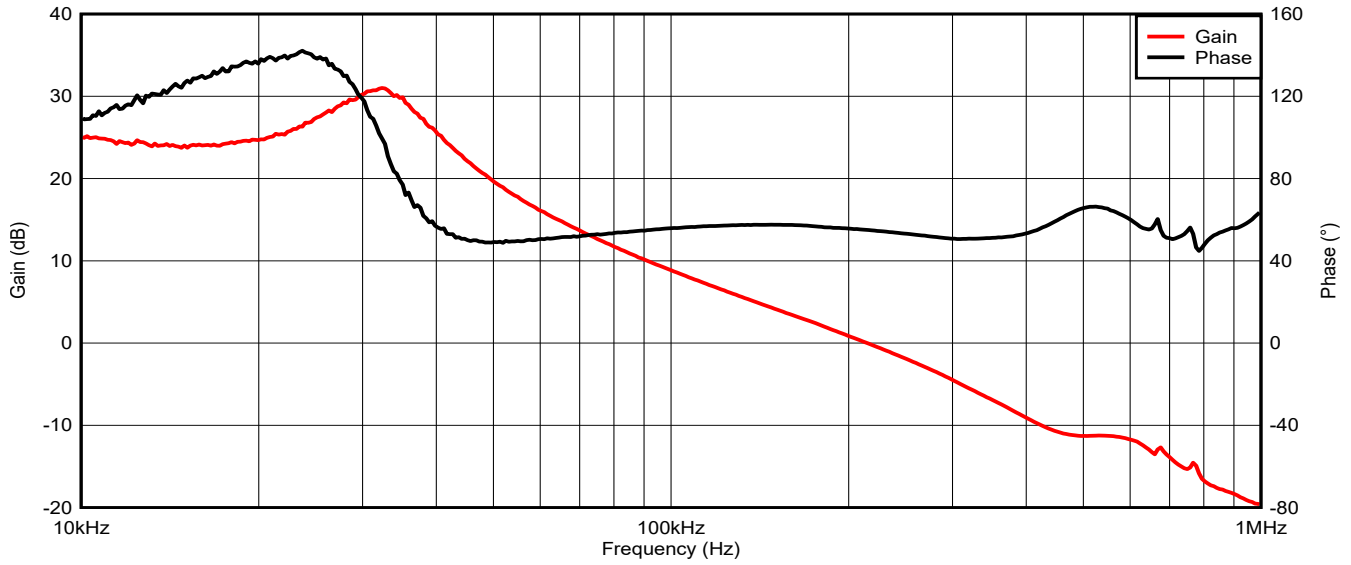


Figure 3-4. Bode Plot of the I2C Version

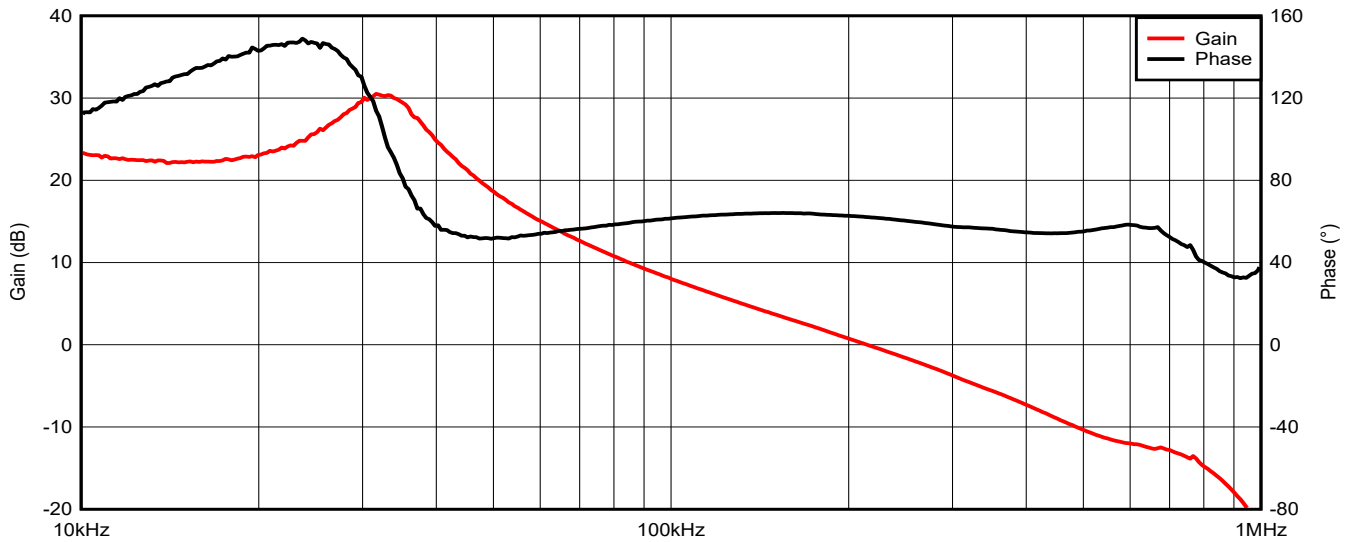


Figure 3-5. Bode Plot of the Resistor Divider Version

The gain and phase plots shown in [Figure 3-4](#) for the I2C version and [Figure 3-5](#) for the resistor divider version show no difference in their gain and phase characteristics.

4 Summary

Using a low impedance resistor divider within the limitations described in this application note can be a good approach for configuring a non-standard output voltage during startup and operation if the digital interface cannot be used for that for any reason. The impact on accuracy is low due to the limited gain of the resistive divider. The current flowing through the resistor divider impacts efficiency, but due to the low output voltages the TPS6287x devices are typically used for, this impact is negligible as well. The effort for this design modification is minimal, basically adding only three additional small passive components, similar to any other typical adjustable output voltage converter configuration.

5 References

- Texas Instruments, [TPS62873 Buck Converter Evaluation Module User's Guide](#).
- Texas Instruments [TPS62873 Dual Buck Converter Evaluation Module User's Guide](#).
- Texas Instruments, [TPS6287x-Q1 2.7-V to 6-V Input, 6-A, 9-A, 12-A, 15-A, Automotive, Stackable, Synchronous Step-Down Converters with Fast Transient Response](#) data sheet.

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