Application Note

Powering the AM625SIP With the TPS65219 PMIC

Power Management IC (PMIC)

ABSTRACT

This application note discusses the TPS65219 power management IC (PMIC) full feature-set powering the AM625SIP Sitara™ processor and principal peripherals. An orderable part number comparison table details the configurations of several factory programmed TPS65219 variants that can support different use cases. Example power maps are provided to assist the design process. For any questions or technical support, use the Power Management E2E design support forum.

Table of Contents

List of Figures

List of Tables

Trademarks

Sitara™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

The TPS65219 PMIC is a cost and space optimized solution developed to power the AM62x processor and its principal peripherals. This PMIC has flexible mapping and comes in several factory programmed orderable part numbers to support different use cases. The AM625SIP processor requires at minimum power for six main rails. These include the core supply (VDD_CORE), DDR PHY IO supply (VDDS_DDR), 1.8 V VDDA analog supply and the 1.8V/3.3 V IO supplies and analog IO rails (VDDSHV). Powering a processor such as the AM62x family demands requirements such as sufficient current headroom, tight transient requirements, and a number of rails that can be fully controlled for power up and power down sequencing. In the event of any inconsistency between any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

Note

This application note covers AM625SIP specifically. For AM625, AM625-Q1, AM623 and AM620-Q1, refer to SLVAFD0

2 TPS65219 Overview

The TPS65219 PMIC contains seven regulators; 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). The Buck converters are capable of supporting up to 3.5 A for Buck1, and 2 A each for the remaining buck regulators. LDO1 and LDO2 (2×400 mA) can be configured as load switch and bypass mode to support dynamic SD card voltages, while LDO3 and LDO4 (2×300 mA) can be configured as load switches. With a VIN range of 2.5 V to 5.5 V, the PMIC can support a common 3.3 V or 5 V system voltage. Table 2-1 shows a summary of the voltage and current capabilities for each of the analog resources. With an I2C interface, three GPIO pins, and three multi-function-pins, the TPS65219 PMIC provides the full power package to supply the AM62x SoC, as well as many other SoCs.

Table 2-1. TPS65219 Power Resources

	Input Voltage	Output Voltage	Current Capability	Comments
BUCK1	2.5 V - 5.5 V	0.6 V - 3.4 V	3.5 A	• 2.3 MHz switching frequency • Dynamic voltage scaling • Programmable power sequencing and default voltages. • Integrated voltage supervisor for undervoltage.
BUCK2	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
BUCK3	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
LDO1	1.5 V - 5.5 V (LDO, Load-Switch) 1.5 V - 3.4 V (Bypass)	0.6 V - 3.4 V (LDO) 1.5 V - 3.4 V (Bypass)	400 mA	• Programmable power sequencing and default voltages. • Configurable as load switch and bypass-mode. • Integrated voltage supervisor for undervoltage
LDO2	1.5 V - 5.5 V (LDO, Load-Switch) 1.5 V - 3.4 V (Bypass)	0.6 V - 3.4 V (LDO) 1.5 V - 3.4 V (Bypass)	400 mA	
LDO3	2.2 V - 5.5 V	1.2 V - 3.3 V	300 mA	• Programmable power sequencing and default voltages. • Configurable as load switch • Integrated voltage supervisor for undervoltage
LDO4	2.2 V - 5.5 V	1.2 V - 3.3 V	300 mA	

2.1 TPS65219 Functional Block Diagram

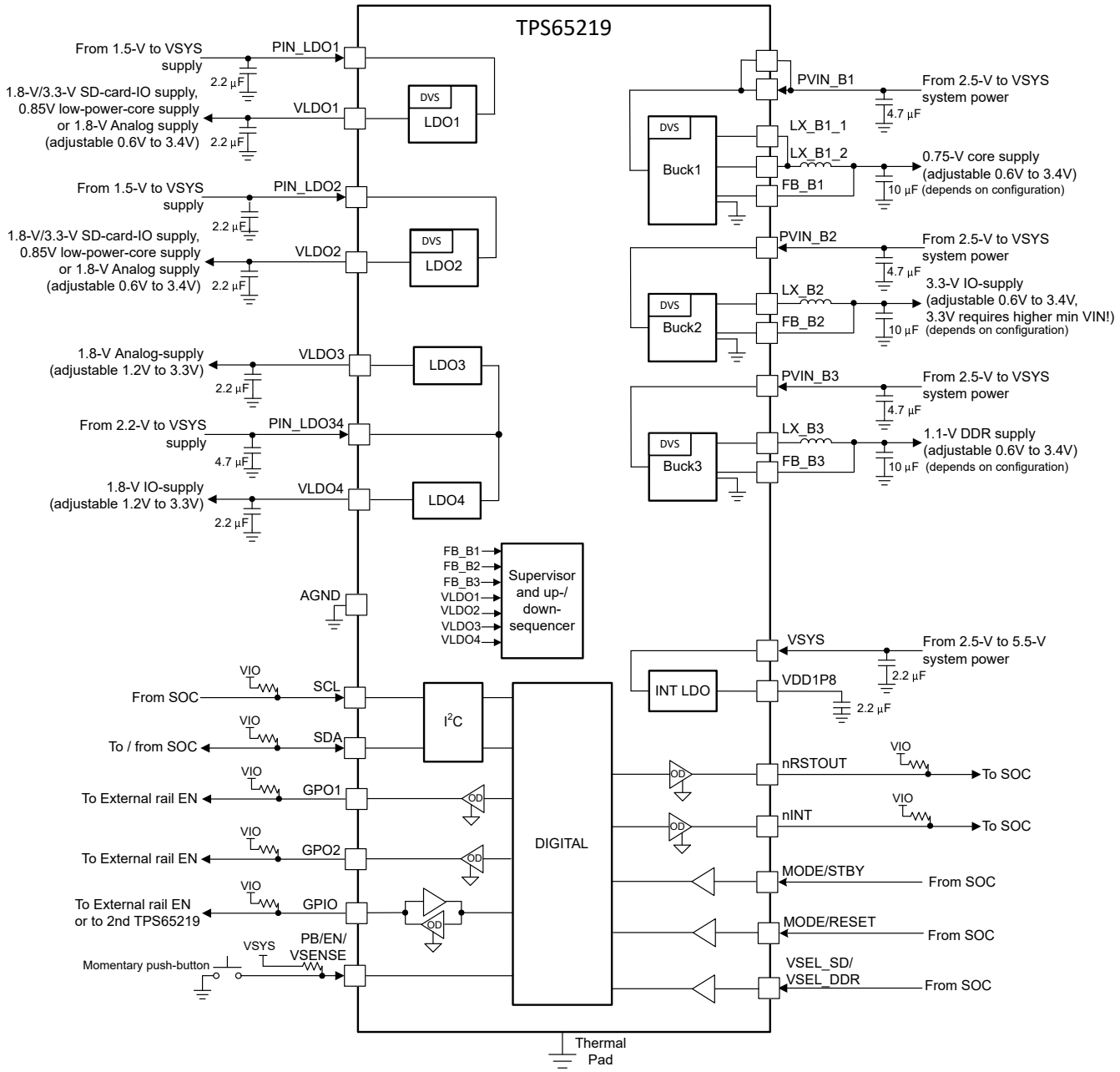


Figure 2-1. TPS65219 Functional Block Diagram

3 TPS65219 Variants

There are multiple variants of the TPS65219 PMIC that come factory programmed with unique register settings to power the AM62x processor and peripherals. Selecting the correct orderable part number (OPN) depends on the application use case, specially the input supply, memory type and CORE voltage. Section 3.1 compares the main NVM settings for the orderable part numbers that are currently available for industrial applications. This table also includes the resources that are available to support new designs. For additional detailed information, please refer to the device data sheet.

Note

Each orderable part number has a technical reference manual (TRMs) that shows the default register settings. The NVM register settings are identified with a "X" in the reset column of the register map in the data sheet. If none of the pre-programmed orderable part numbers (OPNs) meet the application requirements, refer to Section 4 for information about the options for a custom NVM.

3.1 TPS65219 NVMs to Power AM625SIP

Table 3-1. TPS65219 NVMs for AM62x Industrial Applications

		TPS6521902	TPS6521908
Use Case	**Vsys**	**3.3 V**	**3.3 V**
	VDD_CORE	**0.75 V**	**0.85 V**
	Integrated Memory	**LPDDR4**	**LPDDR4**
Technical Reference Manual (TRM)		SLVUCL0	SLVUCM0
BUCK1	**Vout**	0.75 V	0.85 V
	Bandwidth	High bandwidth	High bandwidth
BUCK2	**Vout**	1.8 V	1.8 V
	Bandwidth	High bandwidth	High bandwidth
BUCK3	**Vout**	1.1 V	1.1 V
	Bandwidth	High bandwidth	High bandwidth
LDO1	**Vout**	3.3 V/1.8 V (Bypass)	3.3 V/1.8 V (Bypass)
LDO2	**Vout**	0.85 V	1.2 V (Disabled)
LDO3	**Vout**	1.8 V	1.8 V
LDO4	**Vout**	2.5 V	2.5 V
GPIOs	**GPO1**	Disabled	Disabled
	GPO2	Enabled	Enabled
	GPIO	Disabled	Disabled
MODE/RESET	**Config**	Warm Reset	Warm Reset
	Polarity	High= Normal operation Low=Warm Reset	High= Normal operation Low=Warm Reset
MODE/SBY	**Config**	Mode and Standby	Mode and Standby
	Polarity	High=Active State & Forced-PWM Low=Stby State & Auto-PFM	High=Active State & Forced-PWM Low=Stby State & Auto-PFM
VSEL_SD/DDR	**Config**	SD	SD
	Rail	LDO1	LDO1
	Polarity	High = LDO1_VSET Low = 1.8 V	High = LDO1_VSET Low = 1.8 V
EN/PB/VSENSE pin config		Push-button	Enable
First Supply detection [1]		Enabled	Enabled

1. First Supply detection allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF_REQ status. FSD can be used in combination with any ON-request configuration, EN, PB or VSENSE. At first power-up the EN/PB/VSENSE pin is treated as if it had a valid ON request.

Note

See Section 5 for a comparison of the two VDD_CORE operating points.

4 TPS6521905 User-Programmable NVM

Figure 4-1 shows the supply options that are available. This Application note described the pre-configured NVMs that are available to power the AM62x for different use cases. If none of the orderable part numbers (OPNs) described in this document meet the application requirements or minor changes to the default settings are needed, a custom NVM is required. For high volume opportunities, TI creates a new orderable part number with custom NVM settings. For low volume opportunities, customers can use the resources listed in Table 4-1 to program the PMIC in a production line or through third party programming service.

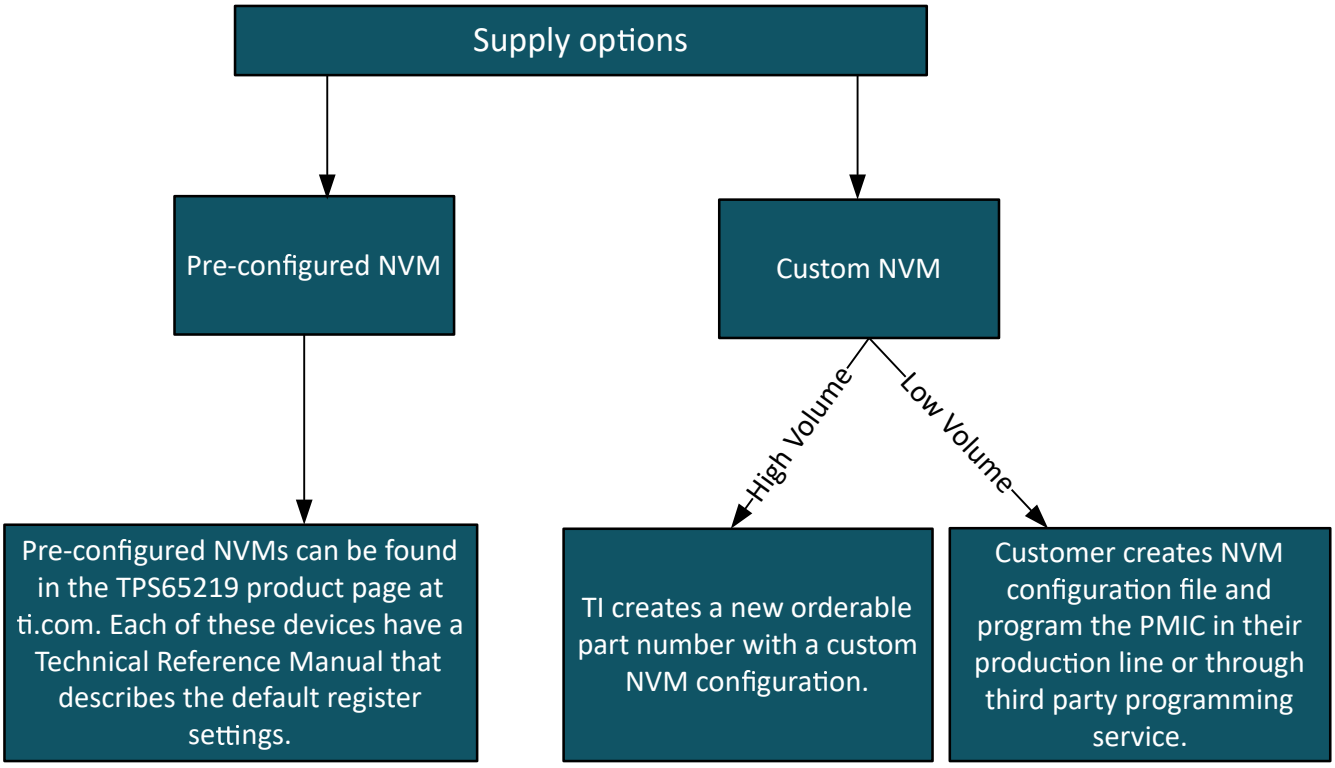


Figure 4-1. Supply Options

Table 4-1. TPS6521905 Programming Resources

Resource	Link
Programming Guide	TPS65219 Non-Volatile Memory (NVM) Programming Guide
Graphical User Interface (GUI)	TPS65219 graphical user interface
Socketed EVM	TPS65219 non-volatile memory (NVM) programming board
TPS6521905 data sheet	User-programmable power management IC (PMIC) with three step-down DC/DC converters and four LDOs

5 AM62x Core Voltage Selection

VDD_CORE is the Core supply of the AM62x processor. This domain has two operating points. Table 5-1 compares the 0.75V and 0.85V operating points in terms of frequency, power consumption, power mapping and sequencing requirements. Since AM62x does not support dynamic voltage scaling, different TPS65219 orderable part numbers are used to support the 0.75 V or 0.85 V operating points.

Table 5-1. CORE Voltage Selection

	VDD_CORE	
	0.75 V (Flexible Core)	**0.85 V (Lowest BOM option)**
Maximum operating frequency on A53SS (Cortex-A53x)	Up to 1.25 GHz	Up to 1.4 GHz
Power Consumption	lower power consumption VDD_CORE [1]	higher power consumption [1]
PMIC and Processor Power Mapping	Requires two PMIC rails; One to supply VDD_CORE at 0.75V and a second PMIC rail to supply VDD*R*_CORE at 0.85V. Buck1, when configured to output 0.75V, is used to supply VDD_CORE. LDO2, when configured to output 0.85V, is used to supply VDDR_CORE.	Lowest BOM option. Allows suppling VDD_CORE (Core supply) and VDDR_CORE (RAM supply) from the same PMIC rail. Buck1, when configured to output 0.85V, is used to supply both CORE rails.
Sequencing	Power-up and power-down sequence requirements. VDD_CORE needs to ramp up before VDDR_CORE. VDD_CORE needs to ramp down after VDDR_CORE.	No sequencing requirements for the CORE supplies as they are both supplied by the same PMIC rail.

(1) For information on the processor power consumption, see the AM62x Power Estimation Tool application note.

6 VSYS Voltage Ramp

The TPS65219 power-up sequence is gated by the following main steps: Voltage on VSYS goes above the POR_Rising threshold, PMIC loads the NVM content into the register map and then waits for an ON request before executing the power-up sequence. The first ON request can be bypassed by enabling the first supply detection feature (FSD) in the *PU_ON_FSD* register field. When *PU_ON_FSD*=0x1, PMIC starts executing the power-up sequence after the NVM settings are loaded to the register map, without waiting for an ON request. In this scenario, customers must ensure the pre-regulator supplying the VSYS reaches a stable output voltage before the PMIC starts executing the power-up sequence. The voltage on VSYS must reach the targeted Vout in approximately 2.3ms after VSYS goes above the POR_threshold.

Note

If FSD is enabled (*PU_ON_FSD*=0x1) and VSYS has a slow ramp, PMIC will try to enable the first rail without having the required input to output voltage headroom. This conditions create a fault on the PMIC.

Figure 6-1 shows an example where FSD is enabled and VSYS has a slow ramp.

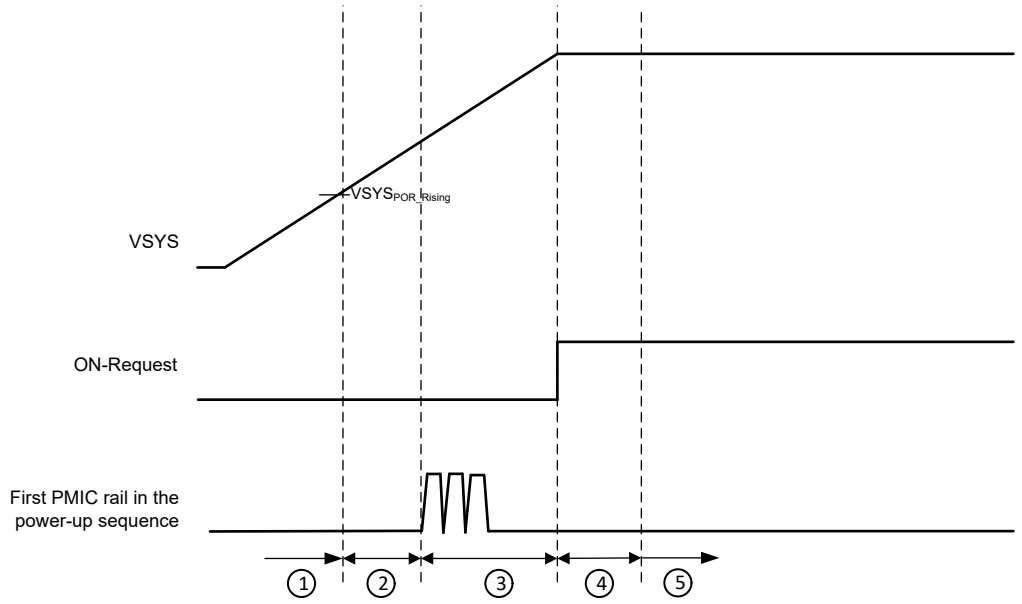
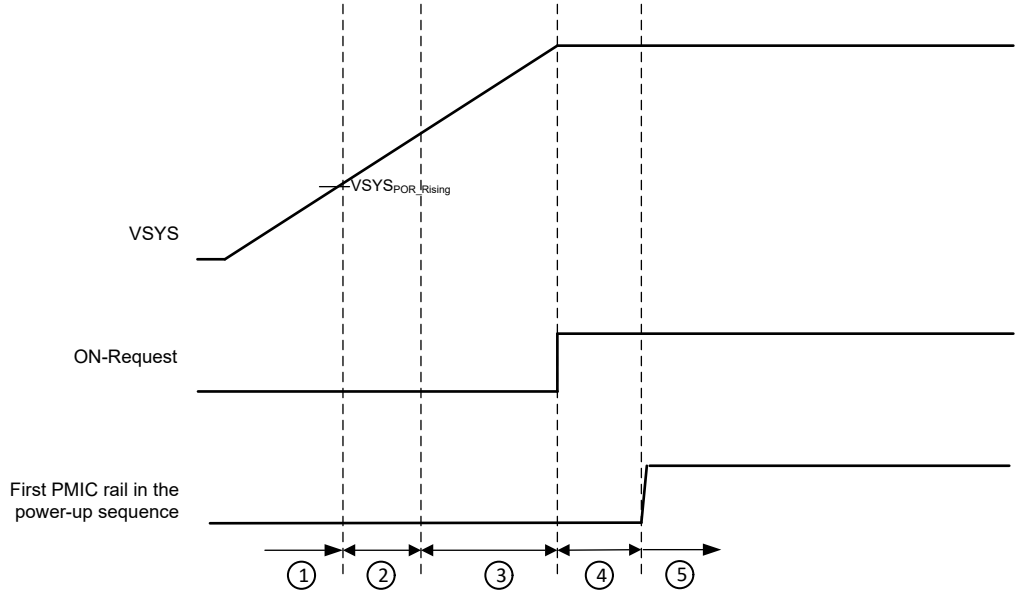


Figure 6-1. VSYS Slow Ramp with FSD Enabled

- **Step 1**: VSYS reaches the POR_Rising threshold.
- **Step 2**: NVM settings are loaded to the registers in approximately 2.3ms.
- **Step 3**: Since FSD is enabled, PMIC starts executing the power-up sequence but the voltage on VSYS is still too low and does not meet the input to output headroom. The first PMIC rail in the power-up sequence shows three voltage peaks which represent the first power-up and the two attempts configured in the retry counter (MASK_RETRY_COUNT).
- **Step 4**: the enable pin goes high and the pin deglitch takes effect.
- **Step 5**: the PMIC is not able to execute the power-up sequence because the device stayed in Initialize state after the power-up attempts in step#3. A power-cycle on VSYS with a faster ramp is required to get the PMIC out of the Initialize state.

Figure 6-2 shows an example where FSD is disabled and VSYS has a slow ramp.



- **Step 1**: VSYS reaches the POR_Rising threshold.
- **Step 2**: NVM settings are loaded to the registers in approximately 2.3ms.
- **Step 3**: Since FSD is disabled, PMIC waits for an ON request to execute the power-up sequence.
- **Step 4**: the enable pin goes high and the pin deglitch takes effect.
- **Step 5**: the PMIC starts executing the power-up sequence starting with the rails assigned to the first slot.

Figure 6-2. VSYS Slow Ramp with FSD Disabled

7 Power Block Diagrams

There are several considerations to take into account when designing the TPS65219 to power the AM62 processor and the peripherals.

- Will the application be using LPDDR4 or DDR4 memory?
- Does an SD card need to be supported?
- What will the system supply voltage be?
- Are there any external discrete ICs that will require fully controlled sequencing?
- Does system application prioritize highest integration or lowest power consumption?

Each of these questions impact the design, configuration, setup, among others, of the power block diagram and plays a role designing the most robust power solution. The sections below describe how the TPS65219 PMIC can supply the AM62x processor on different application requirements.

All the TPS65219 variants described in this application note have LDO1 configured as bypass to supply the SD card dual-voltage I/O (3.3 V and 1.8 V). A processor GPIO control signal with a logic high default value and an external pull-up is used to set SD IO to 3.3 V initially. After the power-up sequence, the processor can set GPIO signal low to select 1.8 V level as needed for high-speed card operation per SD specification. This bypass configuration allows control of the LDO1 voltage from 3.3 V to 1.8 V without the need to establish I2C communication during boot from SD card operations. The bypass configuration on LDO1 requires connecting its input supply pin (PVIN_LDO1) to 3.3 V.

7.1 TPS6521902 Powering AM62x

VSYS = 3.3 V or 5 V | Memory: LPDDR4 | VDD_CORE = 0.75 V

Figure 7-1 shows the TPS6521902 variant powering the AM62x processor on a system with 3.3 V input supply and LDDR4 memory. Buck1 is the PMIC rail with the highest current rating and it is used to supply VDD_CORE. LDO2 supplies VDD*R*_CORE. Buck2 and Buck3 supply the 1.8V IO domain and the 1.1V LPDDR respectively. LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO3 supplies the 1.8V analog domain. LDO4 are 2.5V free power resource that can be used to supply external peripherals like the Ethernet PHY. This NVM variant also has GPO2 pre-programmed to enable an external discrete IC. When using a 3.3V input supply, GPO2 can be used to enable an external power-switch that supplies the system 3.3V IO. This power switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration (before the PMIC start the next slot in the power-up sequence). GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed.

The TPS6521902 also supports 5V input supply. When using VSYS = 5 V, replace the external power-switch with a 3.3 V Buck converter. This external buck converter is enabled by the same PMIC GPO2.

Note

Refer to the TPS6521902 Technical Reference Manual for a description of the NVM settings and power-up/power-down sequence diagrams.

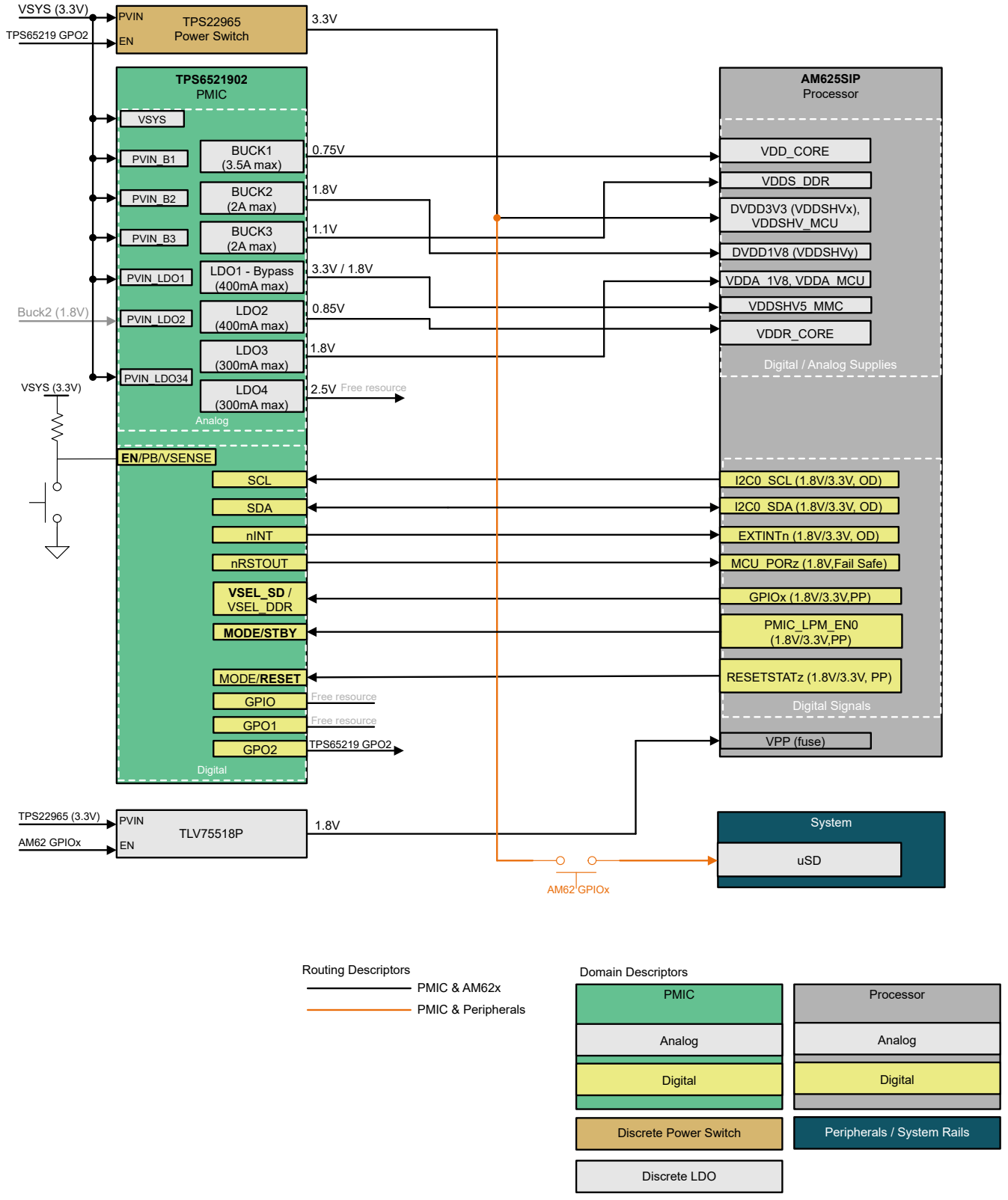


Figure 7-1. TPS6521908 Powering AM625SIP

7.2 TPS6521908 Powering AM62x

VSYS = 3.3 V or 5 V | Memory: LPDDR4 | VDD_CORE = 0.85 V

Figure 7-2 shows the TPS6521908 variant powering the AM62x processor on a system with 3.3 V input supply and LDDR4. In this configuration, Buck1 is configured with an output voltage of 0.85V to supply the CORE rails. As noted in the AM62x spec, "VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85 V". This requirement on the processor allows to have both, VDD_CORE and VDDR_CORE supplied by the same PMIC rail (Buck1). Buck2 and Buck3 supply the 1.8V IO domain and the LPDDR voltage respectively. LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO3 supplies the 1.8V analog domain. LDO2 and LDO4 are free power resource that can be used to supply external peripherals. This NVM variant also has GPO2 pre-programmed to enable an external discrete IC. When using a 3.3V input supply, GPO2 can be used to enable an external power-switch that supplies the system 3.3V IO. This power switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration (before the PMIC start the next slot in the power-up sequence). GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed.

The TPS6521908 also supports 5 V input supply. When using VSYS = 5 V, replace the external power-switch with a 3.3 V Buck converter. This external buck converter is enabled by the same PMIC GPO2.

Note

Refer to the TPS6521908 Technical Reference Manual for a description of the NVM settings and power-up/power-down sequence diagrams.

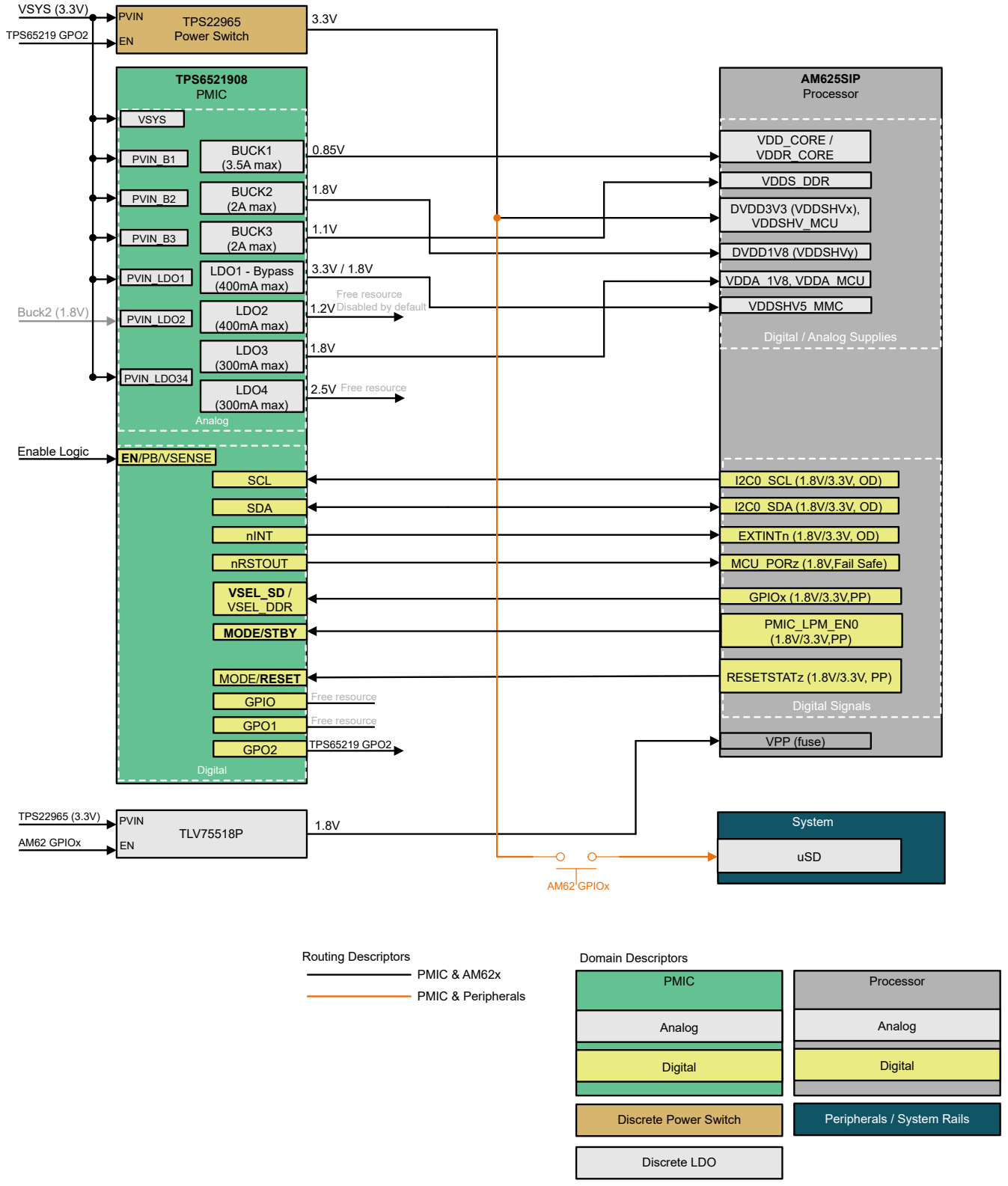


Figure 7-2. TPS6521908 Powering AM625SIP

8 TPS65219 VS Discrete

Table 8-1 shows a BOM size comparison between the PMIC and discrete. This BOM assumes all the PMIC power and digital rails are used in the application. The output capacitance of the PMIC Bucks depend on the selected NVM configuration (low bandwidth or high bandwidth). In this scenario, all Bucks are configured for high bandwidth which supports higher load transient but requires higher output capacitance.

Table 8-2 compares discrete with an optimized PMIC BOM where all the Bucks are configured as low bandwidth and two of the LDOs are unused.

Table 8-1. PMIC Option#1 VS Discrete

	Discrete			PMIC BOM Size		
AM62x-SIP	**Discrete IC**	**Example Part Number**	**Area (mm2)**	**PMIC rail**	**Example Part Number**	**Area (mm2)**
VDD_CORE	Buck	TPS62826DMQR	3.0625	BUCK1-L	SRP3020TA-R47M	4.1625
	Inductor	IHLP1212AEERR47M11	12.675	BUCK1-Cin	GRM21BR71A475KE51L	0.9375
	Cin	GRM188R6YA475ME15D	1.9425	BUCK1-Cout	GRM21BZ71A226ME15L	6.3825
	Cout	GRM188R61A226ME15D	1.9425			
	Rfb	RC0402FR-0741K2L	0.9375			
	Rfb	ERJ-2RKF1003X	0.9375			
	Csw_fb	GRM033R71E121KA01D	0.4675			
	Pull-up Res	ERJ-2RKF1003X	0.9375			
VDDS_DDR	Buck	TPS62A01DRLR	3.4225	BUCK3-L	TFM201208BLE-R47MTCF	4.1625
	Inductor	TFM252012ALMA1R0MTAA	6.1875	BUCK3-Cin	GRM21BR71A475KE51L	0.9375
	Cin	GRM188R6YA475ME15D	1.9425	BUCK3-Cout	GRM21BZ71A226ME15L	6.3825
	Cout	GRM188R61A226ME15D	1.9425			
	Rfb	RN73H1ETTP8352F25	0.9375			
	Rfb	ERJ-2RKF1003X	0.9375			
	Csw_fb	GRM033R71E121KA01D	0.4675			
	Pull-up Res	RC0402FR-07499KL	0.9375			
DVDDSHV5	LDO	TLV7103318QDSERQ1	3.0625	LDO1-Cin	GRM188C81C225KA12D	0.4675
	Cin	GRM188R6YA106MA73D	1.9425	LDO1-Cout	C1005X7S1A225K050BC	0.4675
	Cout	GRM155R61E225KE11D	0.9375			
	Rbleed	ERJ-2RKF1001X	0.9375			
	Pull-up Res	RC0201JR-0710KL	0.4675			
DVDD1V8	Buck	TPS62A01DRLR	3.4225	BUCK2-L	TFM201208BLE-R47MTCF	4.1625
	Inductor	TFM252012ALMA1R0MTAA	6.1875	BUCK2-Cin	GRM21BR71A475KE51L	0.9375
	Cin	GRM188R6YA475ME15D	1.9425	BUCK2-Cout	GRM21BZ71A226ME15L	6.3825
	Cout	GRM188R61A226ME15D	1.9425			
	Rfb	CRCW0402200KFKED	0.9375			
	Rfb	ERJ-2RKF1003X	0.9375			
	Csw_fb	GRM033R71E121KA01D	0.4675			
	Pull-up Res	RC0402FR-07499KL	0.9375			
VDDA	LDO	TLV74018PDQNR	1.5625	LDO3/LDO4-Cin	C1608X7S1A475K080AC	0.9375
	Cin	GRM033R61C105ME15D	0.4675	LDO3-Cout	C1005X7S1A225K050BC	0.4675
	Cout	GRM033R61C105ME15D	0.4675			
Additional analog resources				LDO2-Cin	GRM188C81C225KA12D	0.4675
				LDO2-Cout	C1005X7S1A225K050BC	0.4675
				LDO4-Cout	C1005X7S1A225K050BC	0.4675
PMIC package				PMIC IC package	TPS65219	18.0625
PMIC main supply				VSYS - Cin	GRM188C81C225KA12D	0.4675
PMIC internal LDO				VDD1P8 - Cout	C1005X7S1A225K050BC	0.4675
PMIC pull-up resistors				Various Resistors	RC0201JR-0710KL	3.74

Table 8-1. PMIC Option#1 VS Discrete (continued)

	Discrete			PMIC BOM Size		
AM62x-SIP	**Discrete IC**	**Example Part Number**	**Area (mm2)**	**PMIC rail**	**Example Part Number**	**Area (mm2)**
		Total Discrete Size	**66.2975**		**Total PMIC size**	**60.9275**

Table 8-2. PMIC Option#2 VS Discrete

	Discrete			PMIC Size - Optimized		
AM62x-SIP	**Discrete IC**	**Example Part Number**	**Area (mm2)**	**PMIC rail**	**Example Part Number**	**Area (mm2)**
VDD_CORE	Buck	TPS62826DMQR	3.0625	BUCK1-L	SRP3020TA-R47M	4.1625
	Inductor	IHLP1212AEERR47M11	12.675	BUCK1-Cin	GRM21BR71A475KE51L	0.9375
	Cin	GRM188R6YA475ME15D	1.9425	BUCK1-Cout	GRM21BZ71A226ME15L	3.375
	Cout	GRM188R61A226ME15D	1.9425			
	Rfb	RC0402FR-0741K2L	0.9375			
	Rfb	ERJ-2RKF1003X	0.9375			
	Csw_fb	GRM033R71E121KA01D	0.4675			
	Pull-up Res	ERJ-2RKF1003X	0.9375			
VDDS_DDR	Buck	TPS62A01DRLR	3.4225	BUCK3-L	TFM201208BLE-R47MTCF	4.1625
	Inductor	TFM252012ALMA1R0MTAA	6.1875	BUCK3-Cin	GRM21BR71A475KE51L	0.9375
	Cin	GRM188R6YA475ME15D	1.9425	BUCK3-Cout	GRM21BZ71A226ME15L	3.375
	Cout	GRM188R61A226ME15D	1.9425			
	Rfb	RN73H1ETTP8352F25	0.9375			
	Rfb	ERJ-2RKF1003X	0.9375			
	Csw_fb	GRM033R71E121KA01D	0.4675			
	Pull-up Res	RC0402FR-07499KL	0.9375			
DVDDSHV5	LDO	TLV7103318QDSERQ1	3.0625	LDO1-Cin	GRM188C81C225KA12D	0.4675
	Cin	GRM188R6YA106MA73D	1.9425	LDO1-Cout	C1005X7S1A225K050BC	0.4675
	Cout	GRM155R61E225KE11D	0.9375			
	Rbleed	ERJ-2RKF1001X	0.9375			
	Pull-up Res	RC0201JR-0710KL	0.4675			
DVDD1V8	Buck	TPS62A01DRLR	3.4225	BUCK2-L	TFM201208BLE-R47MTCF	4.1625
	Inductor	TFM252012ALMA1R0MTAA	6.1875	BUCK2-Cin	GRM21BR71A475KE51L	0.9375
	Cin	GRM188R6YA475ME15D	1.9425	BUCK2-Cout	GRM21BZ71A226ME15L	3.375
	Cout	GRM188R61A226ME15D	1.9425			
	Rfb	CRCW0402200KFKED	0.9375			
	Rfb	ERJ-2RKF1003X	0.9375			
	Csw_fb	GRM033R71E121KA01D	0.4675			
	Pull-up Res	RC0402FR-07499KL	0.9375			
VDDA	LDO	TLV74018PDQNR	1.5625	LDO3/LDO4-Cin	C1608X7S1A475K080AC	0.9375
	Cin	GRM033R61C105ME15D	0.4675	LDO3-Cout	C1005X7S1A225K050BC	0.4675
	Cout	GRM033R61C105ME15D	0.4675			
PMIC package				PMIC IC	TPS65219	18.0625
PMIC main supply				VSYS - Cin	GRM188C81C225KA12D	0.4675
PMIC internal LDO				VDD1P8 - Cout	C1005X7S1A225K050BC	0.4675
PMIC pull-up resistors				Various Resistors	RC0201JR-0710KL	3.74
		Total Discrete Size	66.2975		**Total PMIC size**	50.5025

9 Summary

The power delivery network (PDN) described in this document can be used as a guide for integrating the TPS65219 Power Management IC (PMIC) into industrial applications powering the Texas Instruments AM625SIP Sitara™ processor.

10 References

1. Texas Instruments, *TPS65219 Integrated Power Management IC for ARM Cortex—A53 Processors and FPGAs* data sheet.
2. Texas Instruments, *AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM* data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265