TEXAS INSTRUMENTS

# ADSL Full Rate and G.Lite,

## Central Office Modem, Analog Front End, Using TLV320AD12

Application Note

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# *ADSL and G.Lite Central Office Modem Analog Front End Using TLV320AD12*

**ABSTRACT**

This application note defines the system-level hardware for the asymmetrical digital-subscriber line (ADSL) central office analog front end (AFE) incorporating the Texas Instruments TLV320AD12 (AD12). The AFE design is intended to demonstrate the data-handling capabilities of the AD12 in a real system environment. This application note uses a simple line-coupling network; the end user should consider enhancements for actual implementation.

## 1 Purpose

The purpose of this application note is twofold: 1) to demonstrate the system hardware support and interface to the AD12, and 2) to provide a near product-ready reference design for ADSL central office modem AFEs.

The TLV320AD12 device and this application report are applicable to both full rate ADSL and G.Lite. The only difference is in the allocation of tones used for data transfer. G.Lite uses a subset of the frequencies used for Full Rate ADSL. This allows a single Central Office modem design to operate as either a full rate ADSL, or as a G.Lite ADSL modem.

If G.Lite ADSL mode only is desired, the modem DSP code may be simplified, resulting in savings in the DSP computing power required for proper operation. This may result in overall power savings for the modem.

## 2 Key Components

Figure 1 shows the system-level block diagram of the AFE.

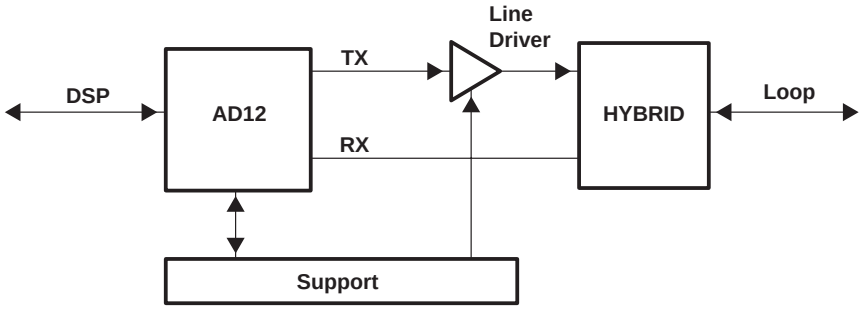


**Figure 1. AFE Block Diagram**

### 2.1 AD12

The AD12 is the target CODEC. The CODEC has four types of interfaces: 1) digital data to and from the DSP, 2) analog-transmit data to the 2-to-4 wire hybrid, 3) analog receive data from the 2-to-4 wire hybrid, and 4) power, clock, and compensation from the support hardware.

There are also eight general-purpose outputs GPO[0:7], not shown above, which may be used for status indicators or system level control functions. These are not essential to data transfer in the AFE.

## 2.2 Line Driver

The line driver amplifies the low-level signal from the AD12 TX port and provides the power necessary to drive the 100-Ω loop transmission line. This application note shows the use of the Texas Instruments THS6022 250-mA dual differential line driver for this function.

## 2.3 Hybrid

The hybrid is a three-port network intended to pass the signal from the line driver to the loop, from the loop to the AD12 RX port, and to isolate the AD12 RX port from the line driver power. The best coupling from the line driver to the loop is –3 dB; half of the transmitted signal power from the line driver is lost in the hybrid. The line driver-to-RX port isolation in most practical circuits is about –24 dB. The hybrid includes the loop line-coupling components, the line transformer, and the DC-line blocking capacitors. This hybrid design is very basic; actual product performance may require a more sophisticated hybrid design. This design is provided to show the basic operation of the hybrid. See Appendix A for the *Hybrid Design Primer*.

### *2.3.1 Support Hardware*

The support hardware consists of the loop timing oscillator, the power supply bypassing, and the compensation components required for proper operation of the AD12 and the line driver.

### *2.3.2 Loop Timing Oscillator*

For TI-centric ADSL modem designs, the loop timing is fixed at the central office; therefore, the oscillator is a fixed-frequency clock oscillator. This is due to the ability of the TI DSPs to process multiple ADSL lines, provided that the CO-end of each line is synchronous. Other manufacturers set loop-timing at the RT side of the modem. Typically, the loop timing oscillator must be stable to ±50 ppm.

In the schematic of Figure 2, the output of the clock oscillator shown on sheet 1 goes off board through pin 46 of connector T50–S1. This signal should be routed back to the board through pin 48. This allows one oscillator to run several AD12 boards. Hardware-address coding allows for up to four AD12s on the same serial bus. With this off-board jumper, the master slot can provide the clock for all slots without the need to populate/depopulate the oscillators when swapping slot cards around. In a single board system, only one oscillator is required.

### *2.3.3 Power*

The AD12 is a 3.3-V part only. The AD12 has separate supply (VDD) and ground (VSS) pins used on various sections of both digital and analog internal functions. It is necessary to connect all VDD and VSS pins for proper operation.

The digital sections of the AD12 are relatively quiet with respect to other digital devices and therefore may be connected to the analog VDD plane. The combined analog and digital VDD should be connected to a *clean* analog power bus. Do not connect these pins to the VDD bus used by the DSP or other high-speed digital devices.

### 2.3.4 Grounding

It is strongly recommended to use a single ground plane in the PWB properly channeled to minimize the flow of digital current from under the analog portions of the circuit. Channeling consists of cutting a single, short, narrow slot in the ground plane to prevent current from flowing in a specific area.

### 2.3.5 GPO Port

The GPO port is not required for AD12 operation; it is supplied as a convenience for modem status indicators, or operational control bits for other functions of the modem product. These bits are set via a serial-port register.

### 2.3.6 Power Supply Bypassing and Compensation

Due to the high-frequency and low-noise nature of ADSL, power supply bypassing and compensation capacitors should be selected carefully with respect to the type of dielectric used in the capacitor.

COG/NPO dielectrics are superior to all other dielectrics in both ESR and self-resonant frequency. Package sizes for capacitors over 1000 pF are difficult to find.

X7R and X5R dielectrics are recommended for larger capacitance values. These dielectrics are still effective at ADSL frequencies.

Solid tantalum dielectrics are effective at ADSL frequencies, but the ESR is greater than that of the other dielectrics previously mentioned. Tantalum capacitors may be used, but the capacitance should at least be doubled in most cases.

### 2.3.7 Loop

The loop is a standard telephone-subscriber loop interface.

### 2.3.8 DSP

The DSP interface consists of a bidirectional parallel-data sample bus, and a bidirectional serial-control bus. These busses are interfaced to a DSP for modulation data processing.

#### 2.3.8.1 Parallel Bus

The parallel bus may be a direct interface to the DSP, depending on the DSP used. Care must be taken to observe *quiet times* as defined in the AD12 data sheet. AD12 read activity (OE active) during *quiet times* may raise the noise floor of the CODEC RX channel. Refer to the AD12 data sheet for details on *quiet time* requirements.

#### 2.3.8.2 Serial Bus

The serial bus is a direct interface to the DSP serial port. Serial port activity is independent of the *quiet times* previously described. Serial accesses can be made at any time. The AD12 generates a free-running SCLK signal for serial-control transfer. The DSP initiates serial transfers by issuing the frame-sync signal FS.

# Appendix A Hybrid Design Primer

## A.1 HYBRIDs

The term *hybrid circuit* is used in telecommunications to identify a three-port network used to separate transmit and receive signals from a bidirectional line port. Such a circuit allows full-duplex operation on a single wire for analog-signal communications service. This is a fairly simple concept not often understood due to the complexity of practical hybrid circuits.

In its simplest form, the hybrid can be represented by the signal flow diagram illustrated in Figure A–1.

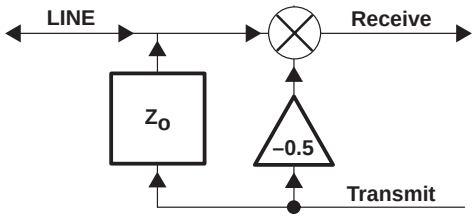


**Figure A–1. Basic Hybrid Signal Flow**

Any signal injected into the Transmit port is routed to the LINE port multiplied by 0.5 as a result of dividing the transmitted signal between the internal $Z_0$ line terminator and the external line impedance. Any signal injected into the LINE port is routed through the summing node and sent out the Receive port. Since the Transmit signal appears to be injected into the LINE port but is not desired on the Receive port, the Transmit signal in inverted, multiplied by –0.5, and summed with the LINE signal, thus canceling the Transmit image from the LINE signal. This leaves the actual signal injected into the LINE port to be sent off the Receive port.

### *A.1.1 Scope*

The remainder of this paper addresses approaches to implementation of hybrid design solutions using some realistic approximations. Designs derived from these approximations should be fine-tuned either by simulation or by empirical methods. The purpose of this paper is to convey the essence and concepts of hybrid design, and not necessarily provide a cookbook solution to the problem.

The circuit examples in this paper assume the characteristic impedance of the LINE is $Z_0$, a high-impedance receiver, and a transmitter is a very low impedance (~0 Ω) driver capable of driving 2 X $Z_0$. The first few examples assume a single-sided line in order to simplify the appearance of the circuitry and better convey the concepts. In actual practice, most communications lines are balanced, differential lines. After the basic concepts have been developed assuming a single sided line, conversion from single-sided examples to balanced-differential examples are addressed and demonstrated.

### A.1.2 Single-Service Line

The solution is simple assuming this communications service has access to the entire line bandwidth. Figure A–2 illustrates this solution:

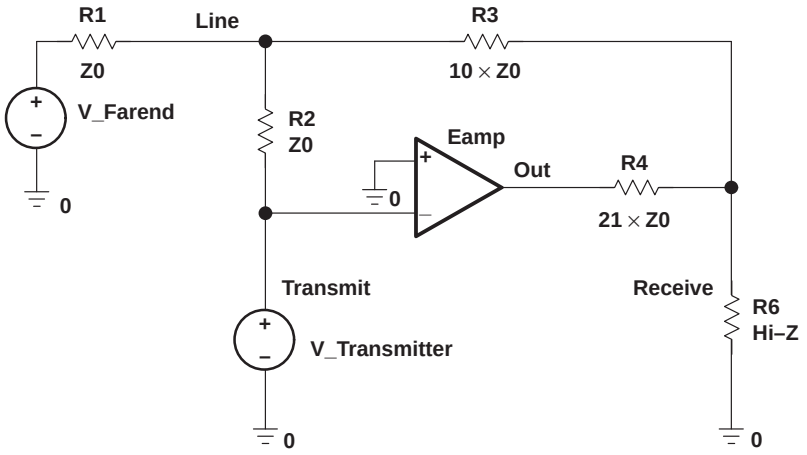


**Figure A–2. Single-Service Line Solution**

By setting R3 to 10 x $Z_0$, the termination of the hybrid LINE input is approximately 94% of $Z_0$. To size R4, assume V_Farend is zero, V_Transmit is nonzero, and the voltage at Receive is zero. The current contributed to the Receive port through R4 must be equal and opposite to the current contributed through R3. The voltage at LINE is slightly less than one-half of V_Transmit because of the voltage division due to R1 and R2; so the value of R4 must be slightly greater than two times the value of R3. Network analysis reveals that R4 must be exactly 21 x Z0 for this ratio of R3 to $Z_0$. The value of the Receive-port load does not affect the value of R4 because the desired voltage at Receive is zero.

Now that the hybrid Transmit to Receive rejection has been established, the LINE to Receive insertion loss can be calculated. Assume that V_Transmit is zero. R1 and R2 divide V_Farend by approximately two. There is a small error due to the path through R3. Assuming that the Receive port load is high-impedance, the voltage at the LINE port is again divided by the combination of R3 and R4. Approximately two thirds of the voltage in the line appears at the Receive port. Thus, the Receive insertion loss is approximately –3.5 dB. This is very near the theoretical insertion loss limit for a hybrid.

Fine-tuning of values can achieve ideal line termination conditions, but does little to reduce Receive insertion loss.

### A.1.3 Multiple-Services LIne

In a complex communications system, several services usually share the frequency spectrum of the same line, such as DC Power, an annunciator (ring) frequency, audio, and modulated data. This forces the use of filters to guard one service from the other. These filters appear in series with the LINE port of the hybrid. These filters are relatively innocuous to the signal in the LINE to Receive port path, but they severely complicate the Transmit to Receive cancellation task.

In a single service line, it may not be obvious that the Transmit signal reflects off of the LINE port, but in fact it does. In this case, where the LINE port is connected to a complex impedance, the Transmit to Receive cancellation path must now cancel a complex reflection.

For example, consider a single pole, high-pass filter in the LINE port path. The circuit in Figure A–3 demonstrates this situation:

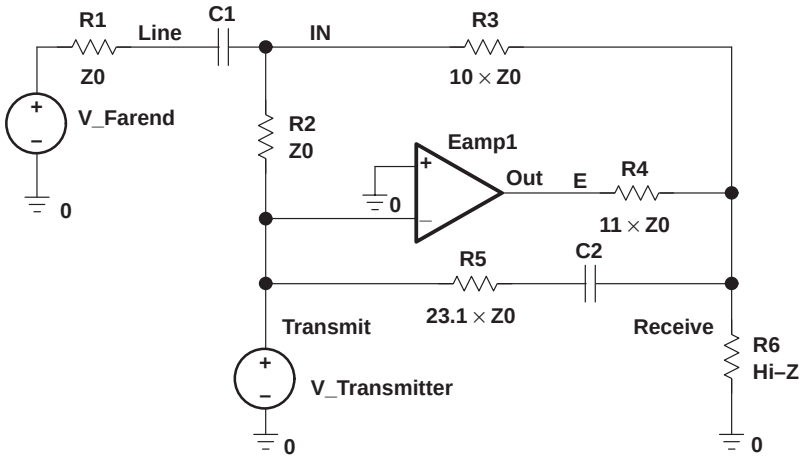


**Figure A–3. Multiple-Services Line Solution**

The dc cancellation network, formed by EAMP1 and R4, no longer has to cancel the effect of the dc-line current. It only has to cancel the effect of R2 and R3, and the value of R4 becomes R2 plus R3.

As the frequency of the transmitter rises above dc, current is drawn away from R3 by the line. This current must be replaced into the Receive port to keep the voltage at zero. Adding a single-pole high-pass network between Transmit and Receive (R5 and C2) can supply the required current. Assume now very high-frequency operation, where C1 and C2 are virtual short circuits. The current summation through R4 and R5 must equal the current through R4 alone for the single service line example where R4 was equal to 21 X $Z_0$.

$$-(11xZ_0) + V\_Transmit/R5 = -1/(21xZ_0)$$

$$R5 = 21x11xZ_0/10 = 23.1xZ_0$$

The cutoff frequency of the cancellation pole must be the same as the line-filter pole. Ignoring the minimal effect of the R3 path, the filter pole is determined by C1, R1, and R2. The cancellation pole is determined by R5 and C2 alone, because the transmitter has a zero-Ω output and the Receive port is forced to zero. Therefore,

$$f_{cl} = 1/(2xPIxC1x2xZ_0) = 1/(2xPIxC2x23.1xZ_0)$$

$$C2=C1x2/23.1$$

$$C2 = C1/11.55$$

As with the previous case, the errors due to the approximations are small, and component values should be fine–tuned for optimal performance.

When the INPUT filter is composed of many poles and zeros, an equivalent pole and/or zero in the cancellation network between Transmit and Receive should be implemented to cancel every pole and/or zero in the INPUT port filter network. This means that the simple network of R5 and C2 would be replaced by a more complex network, which may include connection to the inverted image of Transmit provided by EAMP1.

### *A.1.4 Single-Side to Balanced-Differential Translation*

By mirroring the single sided solution, dividing all impedances by two, and replacing the EAMPs with a connection to the opposite side of the transmitter voltage, the hybrid now becomes balanced and differential as shown in Figure A–4.

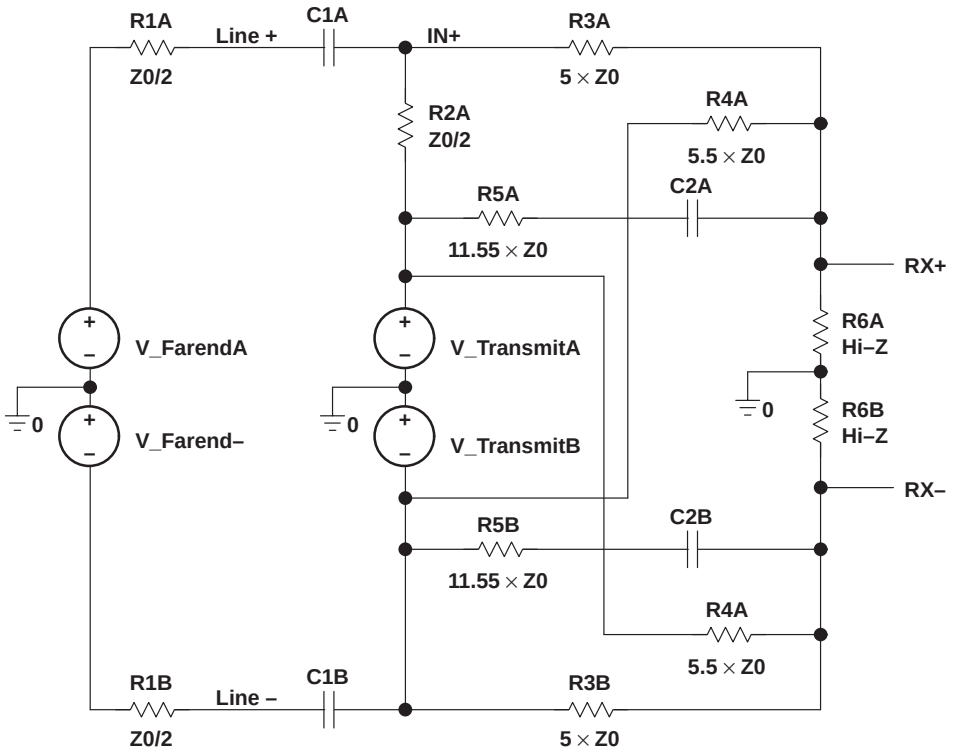


**Figure A–4. Single-Side to Balanced-Differential Translation**

Since most communications lines are transformer-coupled at least at one end, the effect of the transformer must be included in the LINE filter response. If the line is floating, the need to represent the ground nodes is only a convenience and may be omitted from the analysis.

## A.2 Schematics

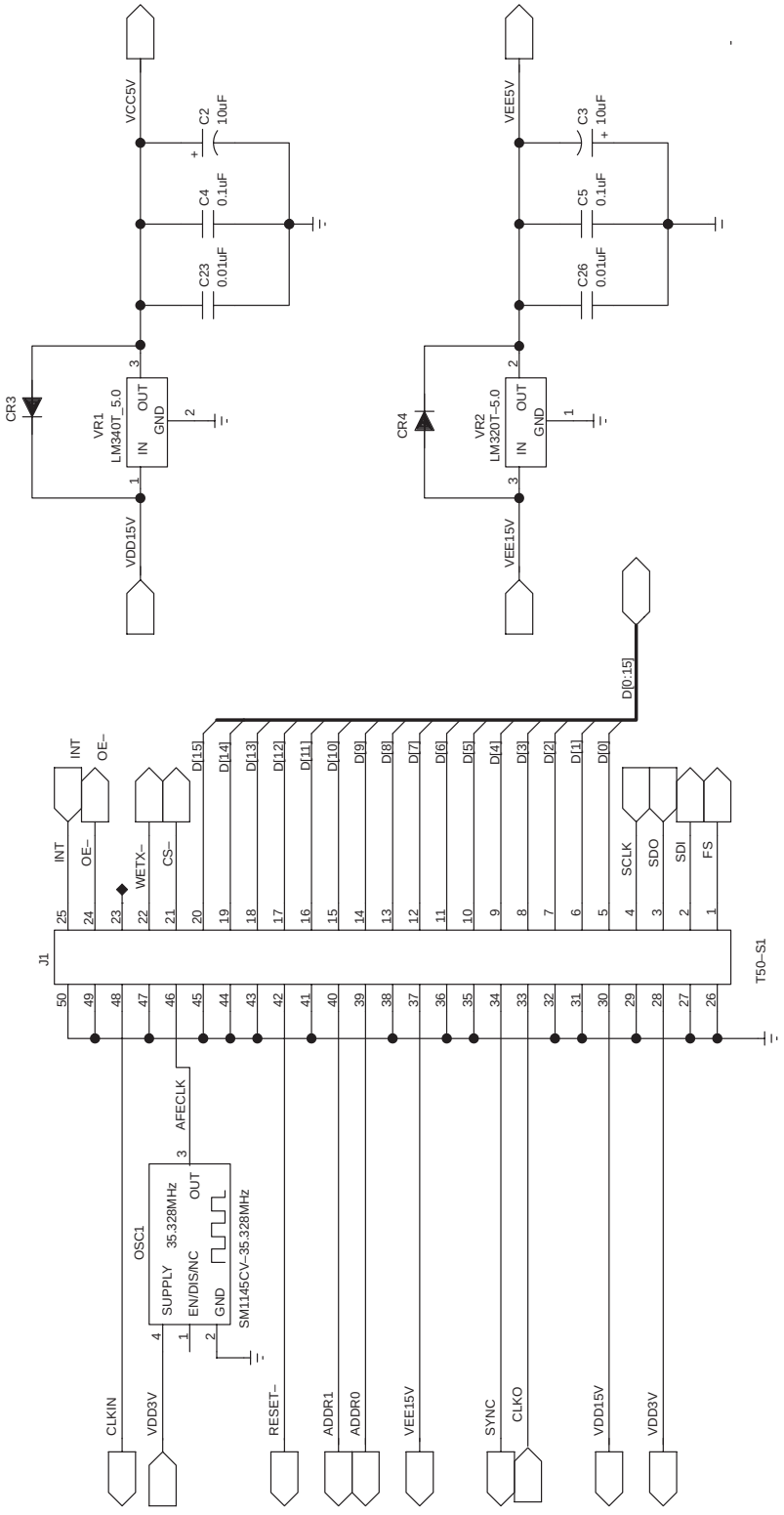


**Figure A–5. Schematic, Sheet 1 of 5**

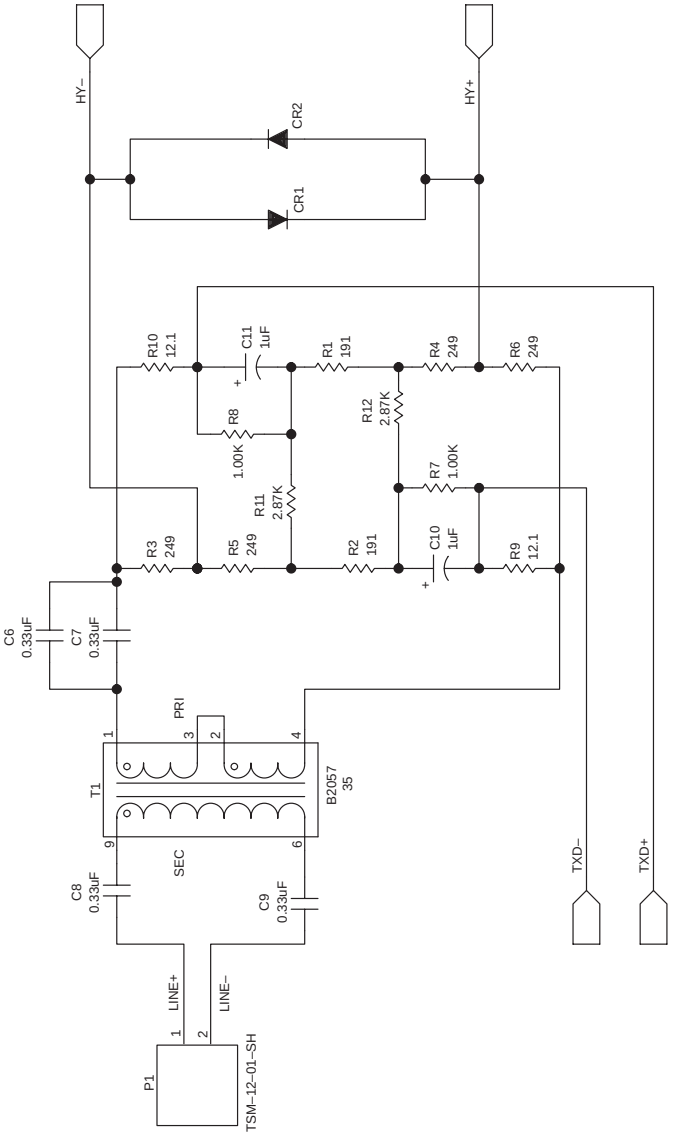


**Figure A–6. Schematic, Sheet 2 of 5**

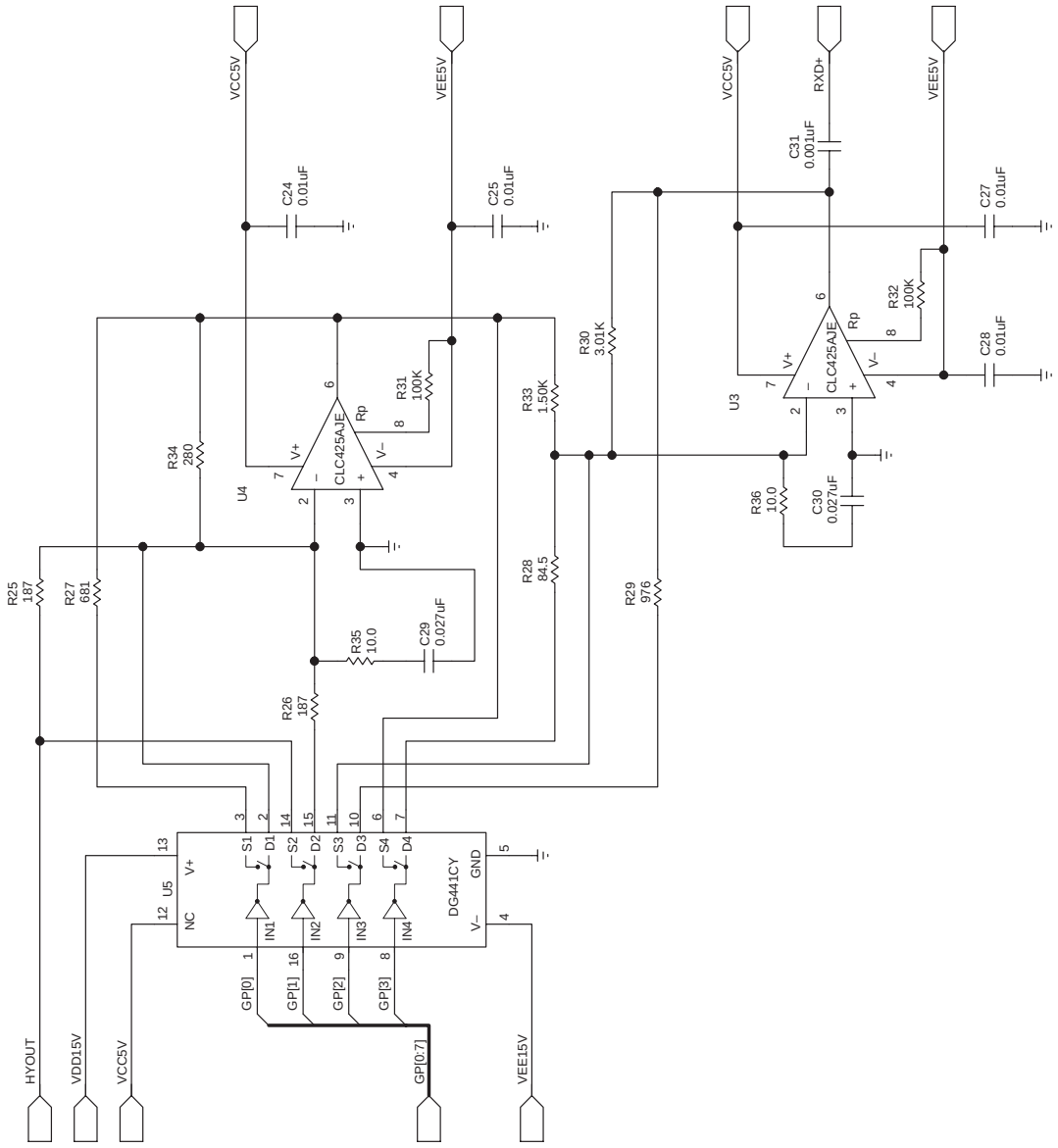


**Figure A–7. Schematic, Sheet 3 of 5**

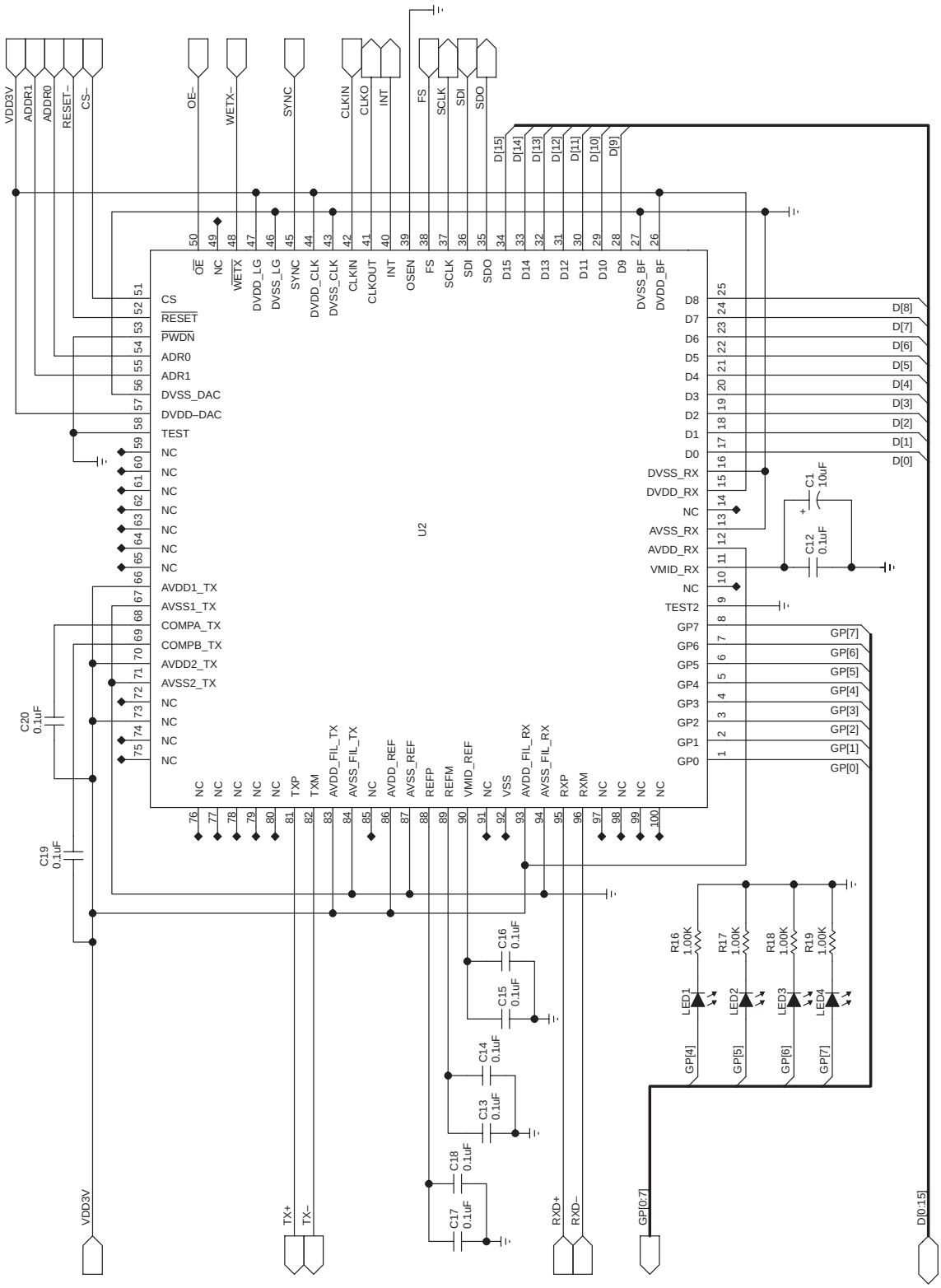


**Figure A–8. Schematic, Sheet 4 of 5**

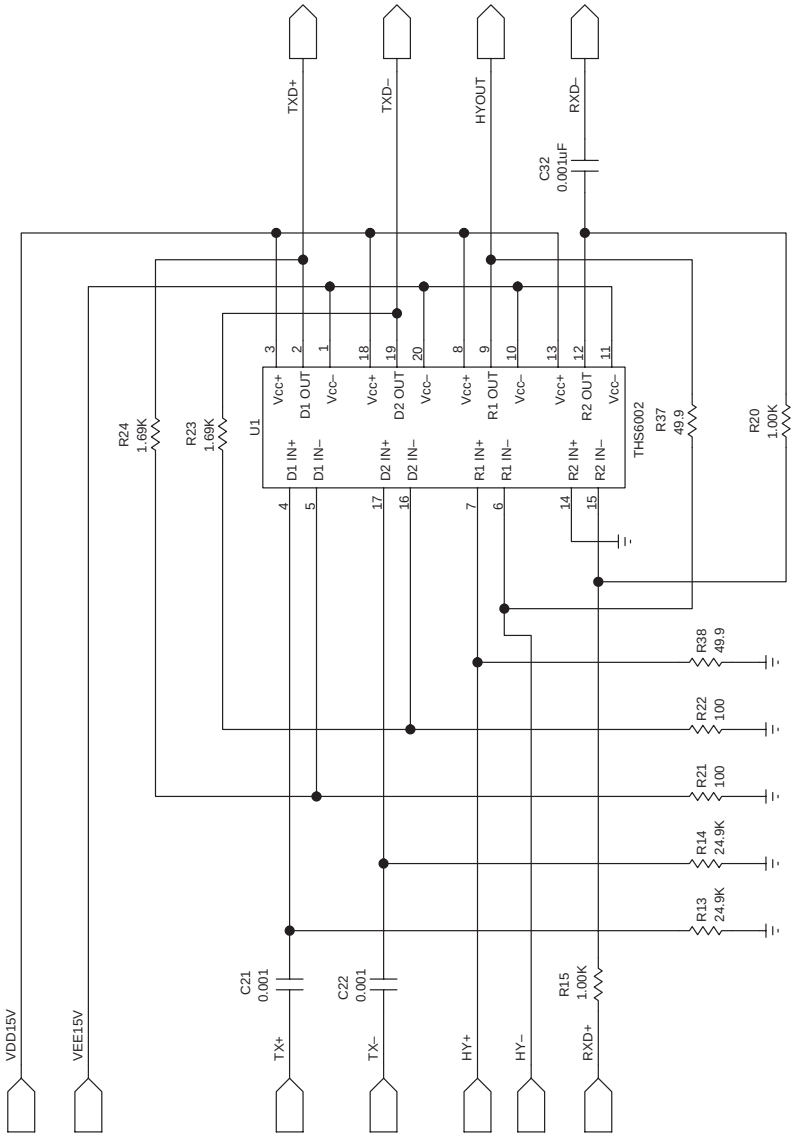


**Figure A–9. Schematic, Sheet 5 of 5**

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