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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Two-channel, 500-kSPS operation of the ADS8361

By Tom Hendrick (Email: t-hendrick@ti.com)
Data Acquisition Applications

Introduction

The ADS8361 is a member of the Texas Instruments (TI) motor control products family of serial analog-to-digital converters (ADCs). The ADS8361 is a 2+2-channel, 16-bit upgrade for the 2+2-channel, 12-bit ADS7861. Its 3.3- to 5-V digital interface is ideally suited for use with the entire TMS320 series of digital signal processors from TI.

The device features two independent 500-kSPS ADC channels, each with its own sample-and-hold circuits and serial data output pin. A user-controllable multiplexer (MUX) allows simultaneous sampling of two 2-channel pairs (4 total channels) at 250 kSPS.

Hardware pins

The ADS8361 features three hardware pins (M0, M1, and A0) that select various operating modes (see Table 1).

Mode I allows for 2-channel operation at speeds of up to 500 kSPS by utilizing both conversion channels. Mode II reduces the maximum throughput to 250 kSPS by using a single serial output pin (OUTA) to present the simultaneously sampled data from channel pairs Ax and Bx. Toggling the address pin A0 controls the selection of channel pair 0 or 1.

Modes III and IV allow the sequential output of both simultaneously sampled channel pairs A0 and B0, followed by A1 and B1. Since Mode III uses both serial outputs A and B, the maximum throughput can be maintained at 250 kSPS. Mode IV presents all 4 converted channels at the OUTA pins, with a maximum throughput of 125 kSPS.

Single McBSP operation

With the interface method presented in Reference 1, applications that do not require simultaneous sampling but do need two fast, independent ADCs can benefit from the ADS8361's 2-µs conversion time. An external MUX or bus switch between the serial outputs would allow 1- to 4-channel operation of channel A or B through a single multichannel buffered serial port (McBSP). Each channel can be independently operated at 500 kSPS. This method would require some sort of control over the state of one or more of the hardware pins M0, M1, and A0, adding additional logic to the design.

Applications with 2 channels and simultaneous-sampling rates of 250 kSPS or less also can use a single McBSP. Hardware pins M0 and M1 can be fixed at ground and V_{CC}, with A0 controlling the channel pairs to be converted (Mode II). This method uses the internal MUX to switch the conversion results from the A and B channels through OUTA. Tying both M0 and M1 to V_{CC} permits 4-channel, simultaneous-sampling applications to be realized. It also allows sequential presentation of two simultaneously sampled channel pairs, 4 channels in all (Mode IV), for applications needing sampling rates of 125 kSPS or less.

If a second McBSP is available, 2- and 4-channel, simultaneous-sampling operation can be realized with no additional "glue logic" required, at 500-kSPS throughput per channel for 2 channels and 250-kSPS for 4 channels.

Dual McBSP operation

The simultaneous conversion properties of the ADS8361 allow conversion data from channels Ax and Bx to be presented to the OUTA and OUTB pins at the same time. Both channels use the same conversion start (CONVST) signal and the same conversion clock so that data skew between A and B outputs is minimized.

To achieve full-speed, 2- and 4-channel operation, the transmitter portion (CLKX, FSX and DX lines) of one McBSP can be used to control the conversion speed, timing, and channel selection of the ADS8361. The ADS8361's serial data outputs, along with clock and frame sync

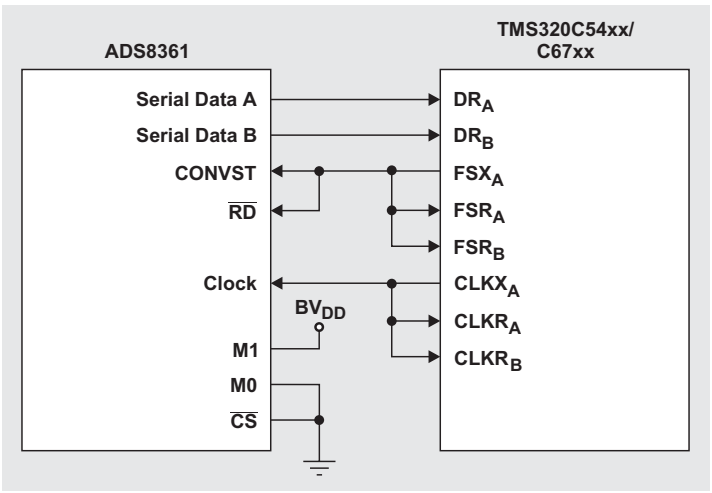
Table 1. Operating modes of ADS8361 hardware pins

MODE	HARDWARE PINS			2-CHANNEL/ 4-CHANNEL OPERATION	DATA ON SERIAL OUTPUTS	CHANNELS CONVERTED	TOTAL THROUGHPUT (kSPS)
	M0	M1	A0				
I	0	0	0	2-channel	A and B	A0 and B0	500
	0	0	1	2-channel	A and B	A1 and B1	500
II	0	1	0	2-channel	A only	A0 and B0	250
	0	1	1	2-channel	A only	A1 and B1	250
III	1	0	X	4-channel	A and B	Sequential	250
IV	1	1	X	4-channel	A only	Sequential	125

return, are then fed to the receiver portions of two McBSPs as shown in Figure 1.

To enhance the control of the ADS8361 further, the unused transmitter section of the second McBSP can be configured as GPIO and connected to the control pins M0, M1, and A0 of the ADS8361. For simultaneous, 2-channel operation at a 500-kSPS-per-channel conversion rate, all that is required is a single GPIO line to toggle A0.

Figure 1. Hardware interface example



Software interface

A project database for this article was developed and compiled with Code Composer Studio™ version 2.20. The most involved portion of writing the code for this simple interface was programming the McBSP. If you wish to receive the project file used in this example, please feel free to send an email to datconvapps@list.ti.com with the title of this article as the subject.

Since the two converters in the ADS8361 share a common interrupt, conversion clock, and conversion start mechanism, the software requirements for the DSP are quite simple. The first McBSP is configured to transmit a frame sync pulse to act as the conversion start signal. FSR_A, DX_A (Serial Data A), and $CLKR_A$ are returned to the first McBSP. The ADS8361's BUSY pin acts as an interrupt to the DSP, which in turn reads the serial data. When the second serial output of the ADS8361 is used, FSR, CLKR, and Serial OUTB are returned to the receiver of the second McBSP. This enables the user to configure the transmitter portion as GPIO to control channel 0 or channel 1 selection of the ADS8361 without the use of additional decode circuits.

Create a .CDB file

Code Composer Studio's graphical user interface for the DSP/BIOS™ configuration (.CDB file) and Chip Support Libraries (CSL) have made it easier than ever to write programs and set up the McBSP.

The first step in creating a project that accommodates the ADS8361 with two McBSPs is to create a .CDB file, then add it to the project. This process creates a .CMD file for the linker, which also needs to be added to the project. Additional DSP/BIOS files are created too, which are added to the project automatically when the .CDB file is loaded. All necessary files and libraries are loaded automatically, based on the DSP/BIOS configuration options set.

By expanding the CSL tab in the .CDB file, the user gains access to the McBSP Configuration Manager. A McBSP configuration is added, and the desired values for clock speed, etc., are set. Once the first configuration is done, it is simply highlighted, copied, and pasted. This creates two copies of the same configuration, each with its own name.

```
MCBSP_Config mcbspCfg0 = {
     0x0000,         /*  Serial Port Control Register 1   */
     0x0220,         /*  Serial Port Control Register 2   */
     0x0060,         /*  Receive Control Register 1   */
     0x0000,         /*  Receive Control Register 2   */
     0x0060,         /*  Transmit Control Register 1   */
     0x0005,         /*  Transmit Control Register 2   */
     0x0109,         /*  Sample Rate Generator Register 1   */
     0x3014,         /*  Sample Rate Generator Register 2   */
     0x0000,         /*  Multichannel Control Register 1   */
     0x0000,         /*  Multichannel Control Register 2   */
     0x2a00,         /*  Pin Control Register   */
};
MCBSP_Config mcbspCfg1 = {
     0x0000,         /*  Serial Port Control Register 1   */
     0x0200,         /*  Serial Port Control Register 2   */
     0x0060,         /*  Receive Control Register 1   */
     0x0000,         /*  Receive Control Register 2   */
     0x0000,         /*  Transmit Control Register 1   */
     0x0000,         /*  Transmit Control Register 2   */
     0x010e,         /*  Sample Rate Generator Register 1   */
     0x3013,         /*  Sample Rate Generator Register 2   */
     0x0000,         /*  Multichannel Control Register 1   */
     0x0000,         /*  Multichannel Control Register 2   */
     0x0a00,         /*  Pin Control Register   */
};
```

McBSP settings

The McBSPs are configured as shown in the sidebar at left.

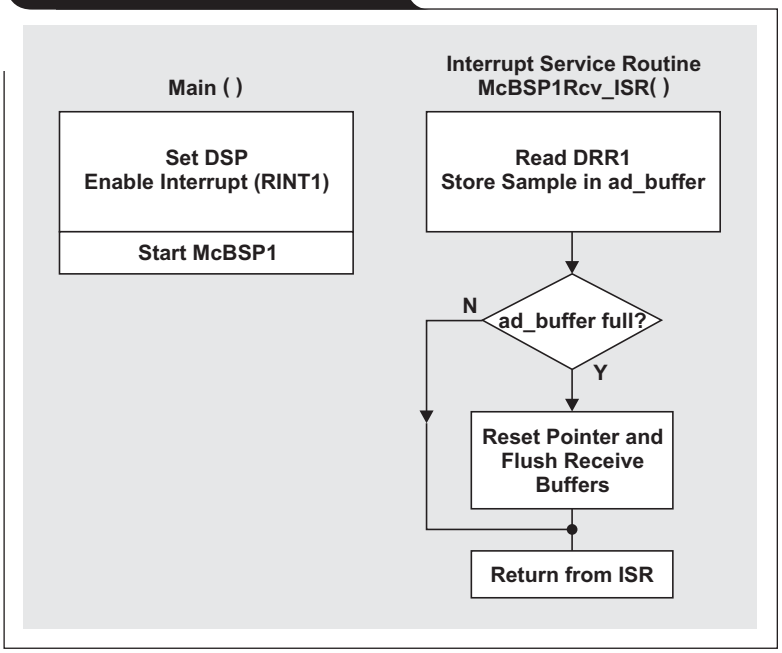
The McBSP is programmed as a serial port in nonstop clock mode (or DSP mode). Frame sync and serial clock signals are output pins. The receiver is set for 16-bit transfers with a 2-bit delay on data receive. The frame sync (FSX1) is generated by the sample-rate generator and is used for both the $\overline{RD}$ and CONVST signals on the ADS8361 by jumper W2 on the evaluation module (EVM).

In the sample code (see sidebar), the ADS8361 is running at 469 kSPS with a serial clock of 9.375 MHz. The C6711 DSP Starter Kit clocks the C6711 DSP at 150 MHz. The sample-rate generator clock source is half the CPU clock, or 75 MHz. The 9.4-MHz clock on CLKX is achieved by setting the CLKGDV bit field in the sample-rate generator register to 8. The formula for calculating the serial clock is

$$\text{CLOCK} = \frac{\frac{\text{CPUCLOCK}}{2}}{\text{CLKDIV} + 1}.$$

By this equation, each clock's cycle is approximately 106.6 ns, triggering a frame-sync pulse every 20 serial clock cycles, which gives a sample rate of 468 kHz. The frame period (FPER) field, in the sample-rate generator register, is where the 20-cycle period is set.

Figure 2. Software flow chart



Software flow

The software presented in this article reads 1024 samples at 469 kHz continuously. As selected in the configuration tool, all the register and peripheral programming is done during initialization. DSP/BIOS pre-initializes all the McBSP registers and other DSP registers before arriving in the main function. As a result, the main function simply enables the interrupt service routine and McBSP1; from then on, the DSP/BIOS and McBSP receive ISR do all the work. When a McBSP1 receive interrupt occurs, `McBSP1Rcv_ISR` reads the port and stores the data in `ad_buffer`. When the buffer is full, it resets the index, `i`, to the beginning and flushes the receive buffer (see Figure 2).

Conclusion

An EVM is available that provides a platform to demonstrate the functionality of the ADS8361 ADC with various TI DSPs and microcontrollers, while allowing easy access to all analog and digital signals for customized end-user applications. For more information on the EVM, visit **www**.ti.com/sc/device/ADS8361 and select Development Tools.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Tom Hendrick, "Interfacing the ADS8361 to the TMS320C6711 DSP," Application Report	slaa164
2. "Dual, 500kSPS, 16-Bit, 2 + 2 Channel, Simultaneous Sampling Analog-to-Digital Converter," ADS8361 Data Sheet	sbas230
3. "TMS320C6711, TMS320C6711B, TMS320C6711C Floating-Point Digital Signal Processing," Data Sheet	sprs088
4. "TMS320C6000 DSP/BIOS User's Guide"	spru303
5. "TMS320 Cross-Platform Daughtercard Specification, Revision 1.0," Application Report	spra711

Related Web sites

analog.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with ADS7861, ADS8361 or TMS320C6711

ADS809 analog-to-digital converter with large input pulse signal

By Hui-Qing Liu (Email: liu_hui-qing@ti.com)
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Introduction

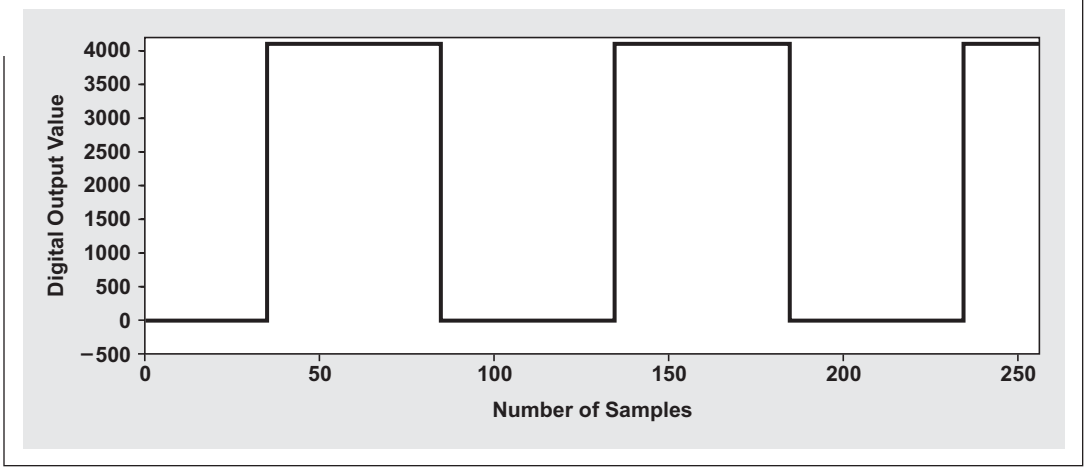
The Texas Instruments (TI) ADS809 is a 12-bit, 80-MHz pipeline analog-to-digital converter (ADC). It has high speed, high resolution, high-input bandwidth, and a high signal dynamic range. Its many other good features include good signal-to-noise-ratio (SNR), good linearity, low jitter, flexible clocking, an over-range indicator (OVR), "data valid" output, three-state output, an internal or external reference, and a single-ended or differential input configuration. It can be used for broadband communications, test equipment, medical instrumentation, CCD imaging, and other fast-ADC applications.

In these applications the input analog signal applied to the ADS809 varies and may be a DC, AC, narrow band, wide band, or pulse signal with a large amplitude. The sampling clock used for these applications can be up to 80 MHz with a uniform or non-uniform clock phase. Different applications require different critical features of the ADS809. In some conventional sampling applications, the ADC input analog signal is smooth with a large amplitude, and the SNR and spurious-free dynamic range (SFDR) are critical; while in some small-signal sampling applications, the SFDR and full-scale (FS) step-acquisition time are not as critical. However, the FS step-acquisition time is critical in large-signal sampling applications, especially when the sampling clock has to be high-frequency with a non-uniform phase and the analog input pulse signal is large (for example, 2 V). In this case the input signal has a sharp edge with a large voltage amplitude, and the pulse edge could be very close to the sampling clock edge due to sampling clock phase variations. If the ADC does not have fast step response for the signal settling, the next ADC sample after the pulse edge will be unstable, which is undesirable. Therefore it is critical for the ADC to have a fast settling time when a large input pulse signal is sampled. Similarly, when the input pulse is over full-scale range (FSR), it is important for the ADC to have a fast over-range recovery time. This is tough for any ADC in applications where the input pulse signal is large and sampling speed is very high with a non-uniform clock phase. However, the ADS809 works well with this type of application. This article presents the results of recent lab tests that further prove the ADS809's fast step response with a large, FS input pulse. The test data also covers the ADS809's response to over-range conditions.

Over-FSR performance of the ADS809

The ADS809's over-voltage condition is defined as the input voltage in excess of its maximum linear conversion range. The voltage FSR of the ADS809 can be set as 2 V_{p-p}, 1.5 V_{p-p}, 1 V_{p-p}, or another range based on the internal or external voltage reference configuration. For single-ended input, the maximum voltage at the ADS809 input pin is +FS (½ FSR above 2.5-V common-mode voltage), and the minimum voltage at input is –FS (½ FSR below 2.5-V common-mode voltage). For differential input, +FS is ¼ FSR above 2.5-V common-mode voltage, and –FS is ¼ FSR below 2.5-V common-mode voltage. For the input voltage over FSR, the ADS809 has control features that include 12-bit data-code control and an OVR.

Figure 1. Output of ADS809 with input pulse over FSR at 66-MHz sampling clock



The digital output code of the ADS809 is straight offset binary or binary two's complement. In straight offset binary format, when the input voltage is maximum, the ADS809 outputs all 12 data bits as 1s (digital value = 4095); and when the input voltage is minimum, the ADS809 outputs all 0s. When the input voltage is 0 (at the middle of the FSR) or only the common-mode voltage, the ADS809 outputs 100000000000 (digital value = 2048). The ADS809 will output data from 0 to 4095 when the input voltage is from –FS to +FS – LSB. The ADS809 will output 4095 when the input voltage is above +FS, and will output 0 when the input voltage is below –FS.

The ADS809 output-code control was tested with the ADC sampling clock at 66 MHz and the input differential pulse amplitude at 2.8 V (0.8 V over FSR). The test result shows that the ADS809 has stable output-code control and quick over-range recovery from the input pulse signal. This is shown in Figure 1. The ADS809 samples 255 digital output samples at 66 MSPS from an over-FS input pulse. The data shows that all the bits are stable at 1 when the input pulse signal is over +FS, and stable at 0 when the input pulse signal is under –FS. The data also shows that when the input pulse signal goes from over FS to under FS or vice versa, the output of the ADS809 tracks the input step change and stays at 4095 or 0 without any miss code or bit flip.

Another over-FSR control feature of the ADS809 is an OVR output pin, which indicates over-range conditions. The OVR output is a function of the reference voltage and the output data bits, so it has the same pipeline delay as the output data bits. The OVR is logical low if the input signal is within the FSR, and logical high if the input signal is over +FS or under –FS. The OVR changes from logical low to high, or logical high to low, immediately following the change of the output data. When this happens, the input voltage changes from inside the FSR to outside the FSR or vice versa. When the input signal continues under or over FS, the OVR always remains high. When the input signal changes from under FS to over FS or vice versa, the OVR changes from high to low for ½ CLK period, then changes to high again. In other words, the OVR outputs a negative pulse at the transition of the input voltage from over FS to under FS or vice versa (see Figure 2). The output's most significant bit (MSB) pin is flipped based on the over-FS input pulse. It is high when the input pulse is over FS and low when the input pulse is under FS. The OVR pin outputs a negative pulse that appears half of the sampling clock period earlier than the transition at the MSB pin.

FS step response of ADS809 and measurement method

The FS step response or step-acquisition time of the ADS809 is defined as the time for the input signal to settle or for the internal sample-and-hold (S/H) circuit to track the input signal with a certain accuracy (for example, 0.1% FS) after the FS step signal is applied to the ADS809. The ADS809 settling time of a FS step signal is 5 ns, which is typically within 0.1% FS and is the minimum required interval between the input step edge and the next sampling clock edge.

The fast step response of the ADC is important in applications with a non-uniform sampling clock, because the variation of the sampling clock phase can cause a phase change between the input pulse and the sampling clock. This is shown in Figure 3, where the rising edge of the clock samples the input pulse signal; and the time, t_S, between the input step edge and the next rising edge of the sampling clock changes with the sampling clock phase change. When t_S is less than the ADC's minimum value, the ADC will take an unstable sample from the unsettled input signal, which is undesirable.

Figure 2. OVR of ADS809 with input pulse over FS

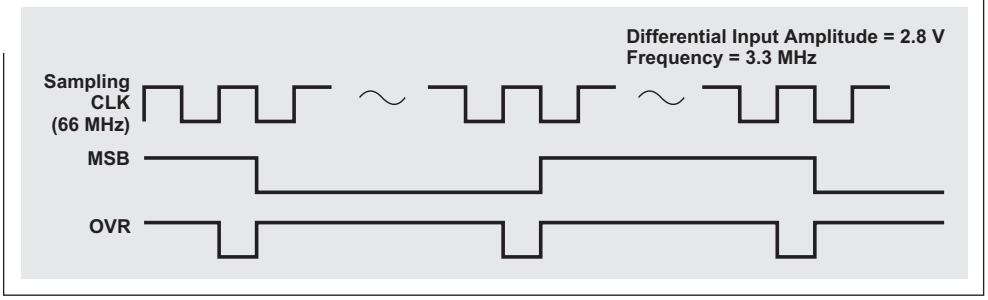
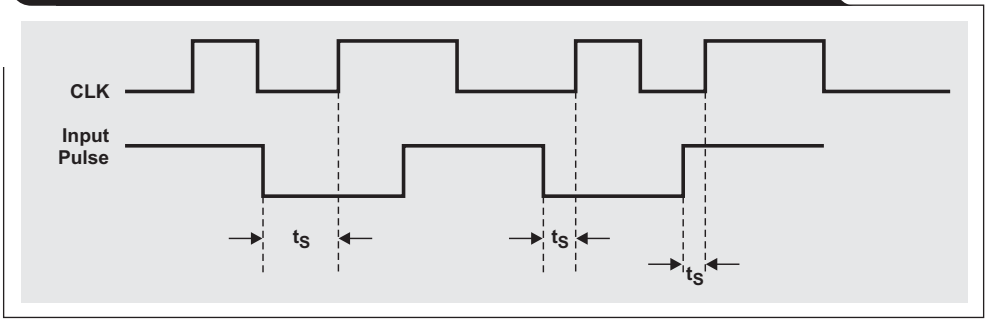
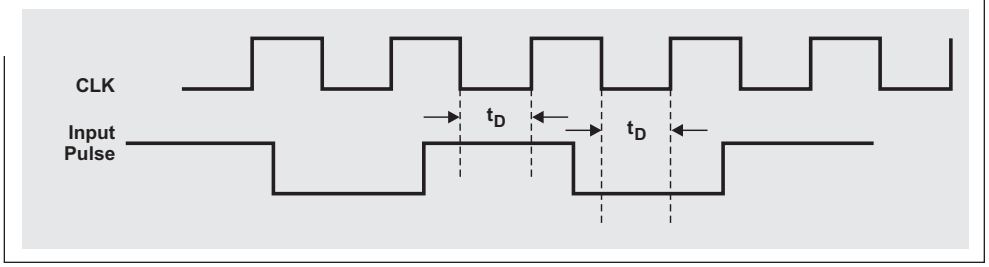


Figure 3. The input step appears during the clock's tracking time because of clock phase variation



There are two ways to evaluate the step response. One is measuring the time, t_S, shown in Figure 3. Another is measuring the relative tracking time, t_D, of the sampling clock shown in Figure 4.

Figure 4. The input step does not appear during the clock's tracking time



In the first method, the step signal (pulse edge in this case) is applied to the input of the S/H circuit directly during the tracking phase. By delaying the input pulse or sampling clock, we can find the minimum t_S, the first stable sample location after the pulse edge, where the pulse signal level has been recovered with the accuracy specified in the data sheet. This minimum t_S is the step response of the ADC. In this method, highly accurate measurement is needed. The signal input path of the ADC should be clean. Large external input capacitance from the board can cause signal step edge distortion, and poor board layout with source impedance mismatch may cause energy reflection or ringing. The probe capacitance of the oscilloscope is also a concern. The shape of the step edge and the detailed timing between the step signal and the ADS809 sampling clock should be carefully measured, including the ADS809 aperture time.

The second and simpler method of step-response evaluation is to measure the clock's tracking time, t_D, shown in Figure 4. In this method the clock's tracking edge appears after the input signal step edge. The clock's tracking edge triggers the ADS809 S/H circuit, changing the previous voltage at the sampling capacitor to the current voltage of the input pulse. The step-response time of the ADS809 S/H circuit should be the same as in the first method (measuring t_S) due to the same RC constant. If the tracking time during t_D measurement is too short, the first sample after the step signal will be unstable. The minimum tracking time of the ADC should be less than or close to half of the sampling clock cycle at the maximum speed specified.

Bench test of ADS809 step response

A real bench test was performed to determine the ADS809 step response with the method shown in Figure 3 (measuring t_S). The basic test block diagram of the ADS809 is shown in Figure 5. The ADS809 was configured with an internal reference, a differential analog input with 2-V FSR, a differential clock input, and an external 2.5-V common-mode voltage for the analog input, with no added load on the common-mode (CM) pin except normal bypass capacitance.

The differential analog input of the ADS809 was a pulse from the pulse generator with a frequency of 3.3 MHz and an amplitude of 2.92 to 2.08 V (high to low) at each analog input, near FSR. This input produced the digital output values of 3770 and 300 (high and low), including a small amount of DC offset. The input pulse's transition from high to low was used as the step signal in the bench test. The single-ended, 66-MHz sampling clock from the pulse generator was converted differentially through a differential translator. A Tektronix logic analyzer (TLA) was used to collect the digital output of the ADS809 to determine whether the sample was stable. After the input step signal, the digital value of the first sample should be 300, within an accuracy

Figure 5. Basic test block diagram for ADS809 step response

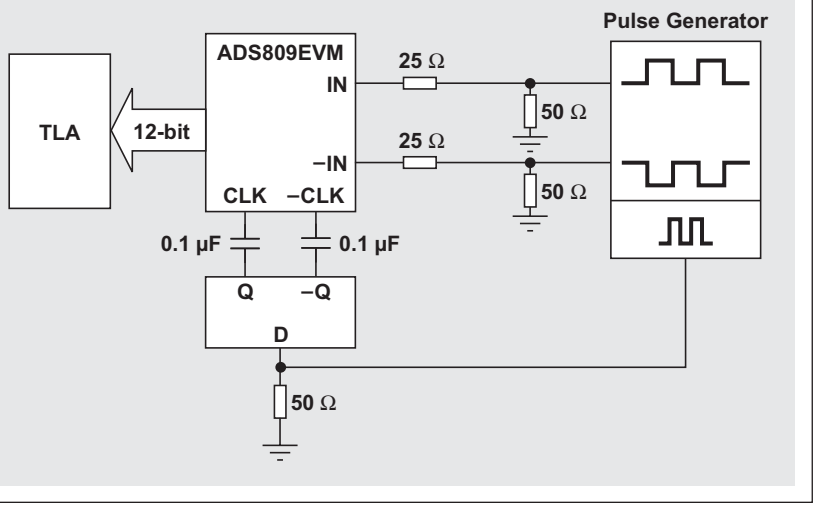
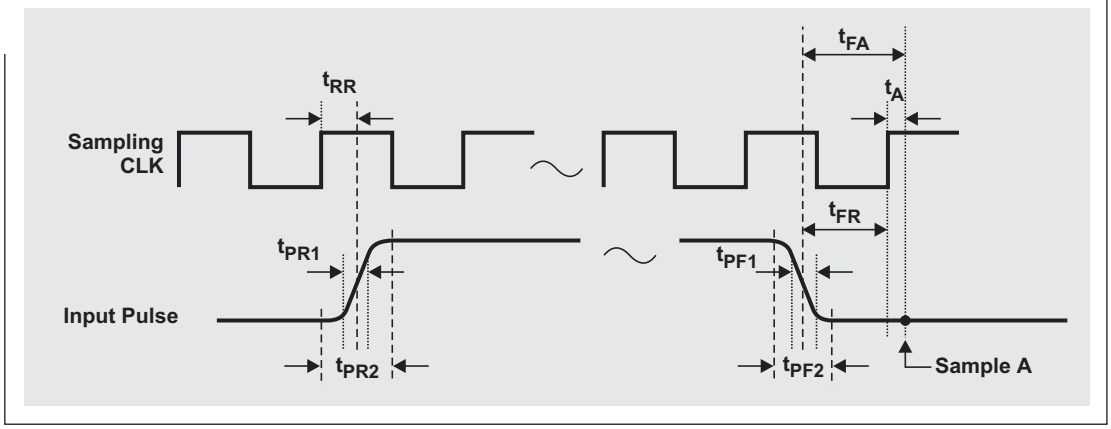


Figure 6. Timing measurement of sampling clock and input pulse at zero delay



of 0.1% FS, if the time interval between the step signal and the clock sampling edge is 5 ns or more as specified.

Three measurements were necessary in this bench test: aperture delay; input signal timing between the sampling clock and the input pulse; and the digital output of the ADS809 with input pulse delay.

The aperture delay, t_A, is the time from the rising edge of the sampling clock to the time when the sampling actually happens (see Figure 6). The data sheet provides only a typical value for t_A (3 ns). In the bench test the aperture delay was found by measuring the MSB and the time from the rising edge of the sampling clock to the falling edge of the pulse.

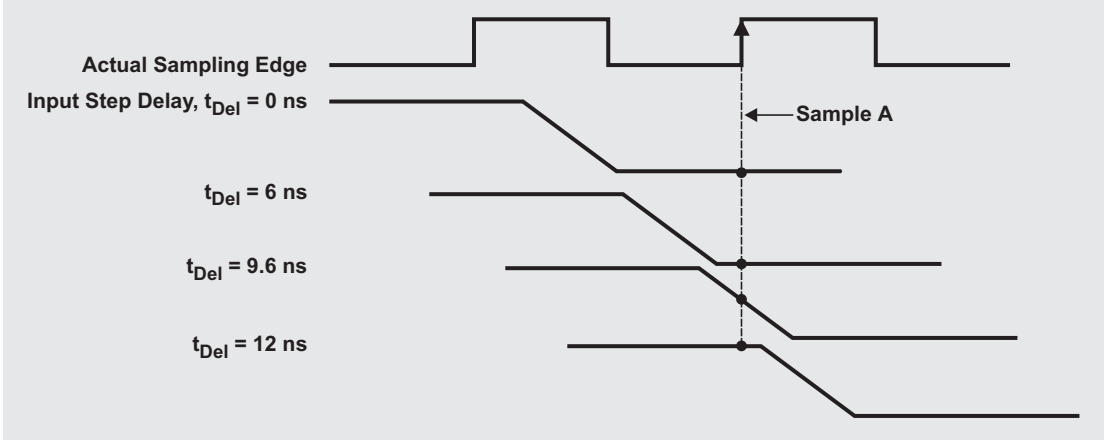
Figure 6 shows the measurement of the input signal timing between the sampling clock and the input pulse at zero delay. This measurement provides pulse edge information and a time reference for the input signal delay. The measurement was taken by Tektronix scope at the ADS809 input and clock input pins. The measurement data is shown in Table 1.

Table 1. Bench test measurement data

PARAMETER	MEASURED VALUE
Input pulse rising time (10% to 10%), t_{PR1}	1.1 ns at analog input pin IN
Input pulse falling time (10% to 10%), t_{PF1}	0.8 ns at analog input pin IN
Input pulse rising time (0.01% to 0.01%), t_{PR2}	2.7 ns at analog input pin IN
Input pulse falling time (0.01% to 0.01%), t_{PF2}	2.8 ns at analog input pin IN
Clock rising edge to pulse rising edge (50% to 50%), t_{RR}	8.5 ns at pins CLK and IN
Pulse falling edge to clock rising edge (50% to 50%), t_{FR}	6.59 ns at pins CLK and IN

After the input timing was measured, the input pulse delay, t_{Del}, was up to 12 ns in steps of 1 ns or less. When t_{Del} was 0, the time from the input pulse falling edge to the next rising edge of the sampling clock, t_{FR}, was 6.59 ns; and Sample A, the first sample after the high-to-low transition of the input pulse, was located at 9.59 ns ($t_{FR} + t_A = t_{FA}$) from the pulse falling edge (see Figure 6). With the increase of the input pulse delay, t_{FR} decreased and Sample A moved close to the falling edge of the input pulse. When the pulse delay was more than 9.5 ns, Sample A moved to the left side of the falling edge of the input pulse (see Figure 7).

Figure 7. Sample A moves with step signal delay



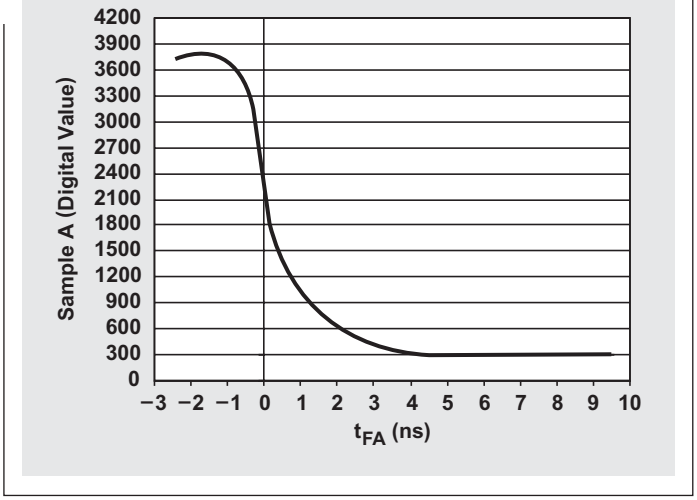
Sample A was collected by TLA, and its digital data is shown in Table 2. The Sample A output value of the ADS809 should be 300 (within an accuracy of ±0.1% FS) if t_{FR} is 2 ns or longer. In other words, Sample A is settled if the time t_{FA} (t_{FR} + t_A), from the falling edge of the input pulse to the actual sampling time of Sample A, is 5 ns or longer. For example, the digital value of Sample A is 299 when t_{FA} is 5.59 ns, and 300 when t_{FA} is about 9.59 ns, due to the input signal tracked by the ADS809 at these times. Sample A is unstable (the digital value is out of the range of 300 ± 0.1% FS) if t_{FA} is shorter than 5 ns. This is shown in Table 2 and Figure 8. For example, when t_{FA} is 3.59 ns, the digital value of Sample A is 358, which is significantly higher than 300, because the input signal has not recovered its low level after the high-to-low step of the input pulse. When t_{FA} is between 0.09 and –0.01 ns (see Table 2), Sample A hits the center of the falling edge or the middle scale of the ADS809. At this point t_{FR} reflects the aperture time of the ADS809. Continually delaying the input pulse eventually moves Sample A into the high level of the input pulse. When t_{FA} is less than –1.41 ns, the digital value of Sample A is about 3770 (see Figure 8). By this measurement, the step-acquisition time of the ADS809 is evaluated as 5 ns, within an accuracy of 0.1% FS, which matches the data sheet.

The test data introduced here includes a small error from the input timing measurement by the scope. There are actually many factors that can affect this type of measurement. The main one to point out here is that different input signal path conditions will have different digital values of Sample A at the same time space, t_{FA}. This could lead to a misinterpretation of the step-response time measurement. During the measurement, three different input signal path conditions were tested. In Condition 1, a 100-pF capacitor was added at the input of the ADS809 on the EVM board. In Condition 2, this 100-pF capacitor was taken off the board. In Condition 3, the 100-pF capacitance was taken off the board and a 25-Ω damping resistor was added on the input path of the board. All three conditions ran with the sampling clock at 66 MHz, the input pulse at 3.3 MHz, the differential pulse amplitude at 1.68 V, and a zero delay to all input signals. The test data shows significant variation of the digital value of Sample A. Condition 1 produced the largest variation, mainly caused by edge distortion of the input pulse due to the external capacitor. Condition 3 produced the smallest variation, mainly caused by board layout and mismatch of the signal source impedance.

Table 2. Digital value of Sample A versus input signal delay

t_{Del} (ns)	t_{FR} (ns)	t_{FA} (ns)	A (digital value)
0	6.59	9.59	300
1	5.59	8.59	299
2	4.59	7.59	301
3	3.59	6.59	296
4	2.59	5.59	299
5	1.59	4.59	315
6	0.59	3.59	358
7	–0.41	2.59	480
8	–1.41	1.59	739
9	–2.41	0.59	1277
9.5	–2.91	0.09	1902
9.6	–3.01	–0.01	2195
10	–3.41	–0.41	3334
11	–4.41	–1.41	3768
12	–5.41	–2.41	3767

Figure 8. Step-response measurement data



Conclusion

The ADS809, with 12-bit resolution and an 80-MSPS sampling speed, is used not only for conventional but also for nonconventional ADC sampling applications. An example of the latter is an ADC with a high-speed sampling clock with a non-uniform sampling phase that converts a large-amplitude input pulse signal. Such an application requires fast ADC settling time. This article has provided some test data based on the conditions of this type of application, including an over-FS control function and FS step-response measurement. The test data shows that the ADS809 has stable output-code control and stable OVR output when the input pulse signal is over 2-V FS. The ADS809 can convert a 2-V FS input pulse signal at an 80-MHz sampling rate and produce a stable output code. An actual bench test of the ADS809's FS step response was conducted; and the test method, procedure, and test results have been presented. The test data shows that the ADS809 has a FS step-acquisition time of 5 ns. It also indicates that the ADS809 has a large input dynamic range, a high-input bandwidth, and a fast, FS step response, making it suitable for large-signal sampling applications.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "12-Bit, 80MHz Sampling Analog-to-Digital Converter," ADS809 Data Sheet	sbas170
2. Mikael Gustavsson, J.J. Wikner, and N.N. Tan, *CMOS Data Converters for Communications* (Kluwer Academic Publishers, 2000).	—

Acknowledgments

Special thanks go to Bryan McKay for his work on the test board and to Wallace Burney for his article review.

Related Web sites

analog.ti.com
www.ti.com/sc/device/ADS809

LED-driver considerations

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Many of today's portable electronics require backlight LED-driver solutions with the following features: direct control of current, high efficiency, PWM dimming, over-voltage protection, load disconnect, small size, and ease of use. This article discusses each of these features and how they are achieved, and concludes with a typical circuit that implements each of these features.

Direct control of current

LEDs are current-driven devices whose brightness is proportional to their forward current. Forward current can be controlled in two ways. The first method is to use the LED V-I curve to determine what voltage needs to be applied to the LED to generate the desired forward current. This is typically accomplished by applying a voltage source and using a ballast resistor as shown in Figure 1. However, this method has several drawbacks. Any change in LED forward voltage creates a change in LED current. With a nominal forward voltage of 3.6 V, the LED in Figure 1 has 20 mA of current. If this voltage changes to 4.0 V, which is within the specified voltage tolerance due to temperature or manufacturing changes, the forward current drops to 14 mA. This 11% change in forward voltage causes a much larger 30% change in forward current. Also, depending upon the available input voltage, the voltage drop and power dissipation across the ballast resistor waste power and reduce battery life.

The second, preferred method of regulating LED current is to drive the LED with a constant-current source. The constant-current source eliminates changes in current due to variations in forward voltage, which translates into a constant LED brightness. Generating a constant-current source is fairly simple. Rather than regulating the output voltage, the input power supply regulates the voltage across a current-sense resistor. Figure 2 shows this implementation. The power-supply reference voltage and the value of the current-sense resistor determine the LED current. Multiple LEDs should be connected in a series configuration to keep an identical current flowing in each LED. Driving LEDs in parallel requires a ballast resistor in each LED string, which leads to lower efficiency and uneven current matching.

Figure 1. Voltage source with ballast resistor

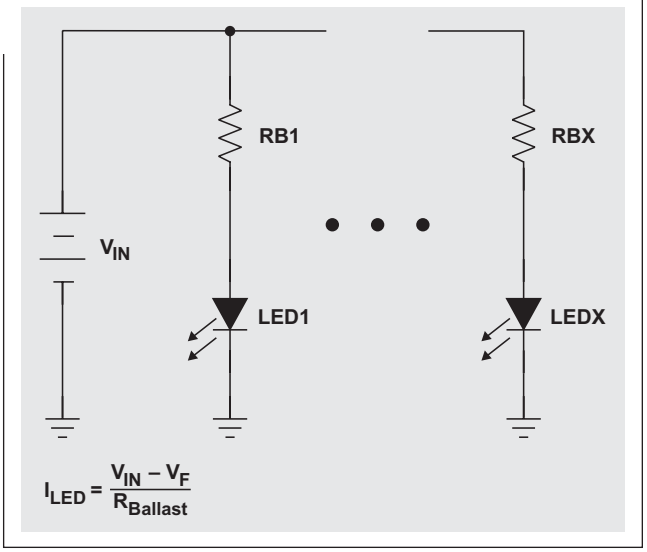
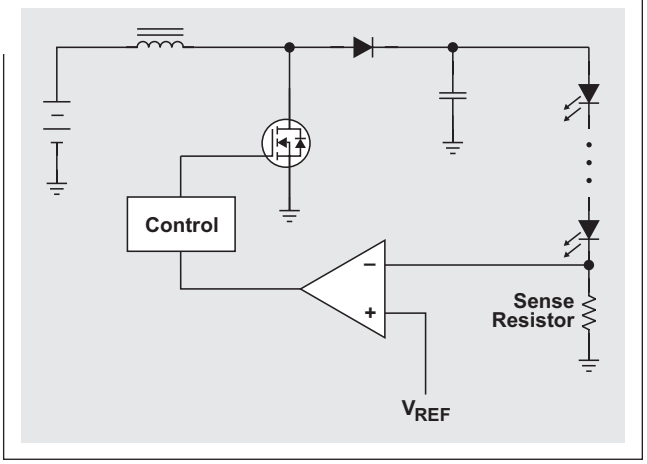


Figure 2. Constant-current source for driving LEDs



High efficiency

Battery life is critical in portable applications. For an LED driver to be useful, it must be efficient. An efficiency measurement of an LED driver differs from that of a typical power supply. An efficiency measurement of a typical power supply is defined as the output power divided by the input power. With an LED driver, the output power is not the parameter of interest. What is important is the amount of input power required to generate the desired LED brightness. This is easily determined by dividing the power in the LEDs by the input power. Defining the efficiency in this way means that the power dissipated in the current-sense resistor contributes to the power lost in the

supply. The following equation shows that smaller current-sense voltages contribute to higher-efficiency LED drivers.

$$\text{Efficiency} = \frac{P_{LED}}{P_{LED} + P_{Supply\_Losses} + P_{Current\_Sense}}$$

Figure 3 shows that choosing a power supply with a 0.25-V reference voltage versus a supply with a 1-V reference voltage improves efficiency. A supply with a lower current-sense voltage is more efficient regardless of input voltage or LED current. With all else being equal, a lower reference voltage significantly improves efficiency and extends battery life.

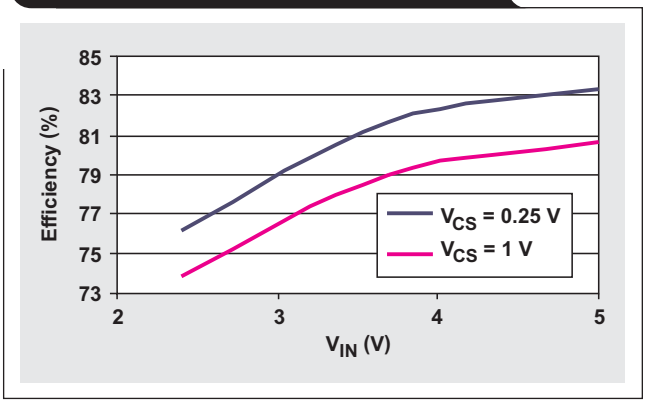
PWM dimming

Many portable LED applications require dimming. In applications such as LCD backlighting, dimming provides brightness and contrast adjustment. Two types of dimming are available: analog and PWM. With analog dimming, 50% brightness is achieved by applying 50% of the maximum current to the LED. Drawbacks to this method include LED color shift and the need for an analog control signal, which is not usually readily available. PWM dimming is achieved by applying full current to the LED at a reduced duty cycle. For 50% brightness, full current is applied at a 50% duty cycle. The frequency of the PWM signal must be above 100 Hz to ensure that the PWM pulsing is not visible to the human eye. The maximum PWM frequency depends upon the power-supply startup and response times. To provide the most flexibility and ease of integration, the LED driver should be able to accept PWM frequencies as high as 50 kHz.

Overvoltage protection

Operating a power supply in a constant-current mode requires overvoltage protection. A constant-current supply generates a constant output current regardless of load. If the load resistance increases, the supply's output voltage also must increase to supply a constant current. If the supply encounters an excessive load resistance, or if the load is disconnected, the output voltage can increase above the voltage rating of the IC or of the other discrete circuit components. Several overvoltage protection schemes are available for constant-current LED drivers. One scheme is to place a zener diode in parallel with the LEDs. This limits the output voltage to the zener's breakdown voltage plus the supply's reference voltage. During an overvoltage condition, the output voltage increases to the point where the zener breaks down and begins to conduct. The output current flows through the zener, then through the current-sense resistor to ground. The supply continues to generate the constant output current while the zener limits the maximum output voltage. A more preferred method of overvoltage protection is to monitor the output voltage and shut down the supply when the overvoltage trip point is reached. Shutting down the supply under an overvoltage condition reduces power dissipation and extends battery life in the event of a fault.

Figure 3. LED driver efficiency versus current sense voltage



Load disconnect

An often overlooked feature in an LED-driver supply is load disconnect. Load disconnect electrically removes the LEDs from the power supply when the supply is disabled. This is important in two situations: shutdown and PWM dimming. As shown in Figure 2, during shutdown of a boost converter, the load is still connected to the input through the inductor and catch diode. Since the input voltage is still connected to the LEDs, a small current continues to flow, even when the supply is disabled. Even small leakage currents significantly reduce battery life during extended periods of off time. Load disconnect is also important during PWM dimming. During the off time of the dimming period, the supply is disabled; but the output capacitor is still connected across the LEDs. Without load disconnect, the output capacitor discharges through the LEDs until the dimming pulse turns the supply on again. Since the capacitor is partially discharged at the beginning of each dimming cycle, the supply must charge up the output capacitor at the beginning of each dimming cycle. This creates a spike of inrush current during each dimming cycle. The inrush current lowers system efficiency and creates voltage transients on the input bus. With load disconnect, the LEDs are removed from the circuit so there is no leakage current when the supply is disabled, and the output capacitor remains fully charged during PWM dimming. A load-disconnect circuit is best implemented by placing a MOSFET between the LEDs and the current-sense resistor. Placing the MOSFET between the current-sense resistor and ground creates an additional voltage drop that manifests itself as an error in the output-current setpoint.

Ease of use

Ease of use is a relative concept. A circuit's ease of use not only encompasses the complexity of the initial design but also involves any future effort required to modify the circuit quickly and reuse it for other programs that may have slightly different requirements. In general, hysteretic controllers are very easy to use. A hysteretic controller

eliminates the need for the complicated frequency compensation required in a classical power-supply design. While frequency compensation is not difficult for an experienced power-supply designer, most novice power-supply designers find it tedious. Since the optimal compensation changes for different input and output conditions, a classical power-supply design does not lend itself to quick modifications for different operating conditions. A hysteretic controller is inherently stable and requires no changes as input and output conditions change.

Small size

Small size is an important feature for portable circuitry. Several factors contribute to the size of the circuit components. One factor is switching frequency. Higher switching frequencies allow the use of smaller passive components. A modern LED driver intended for portable applications should be able to switch at frequencies of up to 1 MHz. Switching at frequencies greater than 1 MHz is not typically recommended because it does not significantly reduce circuit size; but it does reduce efficiency and lower battery life due to the higher switching losses. Integration of features into the control IC is the single most important factor that contributes to a small-driver solution. If all the features described in the preceding paragraphs were implemented with discrete components, the board area required would take up more space than the power supply itself. Integrating these features into the control IC significantly reduces the overall driver size. A second but equally important benefit of feature integration is a reduction in the total solution cost. Implemented discretely, all desirable features in an LED driver can add an additional sixty to seventy cents in component cost. When integrated into the control IC, these features typically add only pennies to the cost of the IC.

Practical solution

The TPS61042 is an excellent example of a modern LED-driver control IC. Figure 4 is a block diagram of the TPS61042 with a highly integrated control IC. Q1 is a low-resistance, integrated power FET. The low resistance of this component contributes to an extremely high efficiency. The 0.25-V reference voltage reduces losses in the current-sense resistor. PWM dimming is easily implemented with this IC by applying a PWM signal to the CTRL pin at frequencies as high as 50 kHz. Q2 implements the integrated load-disconnect circuitry. Since it is integrated, this circuitry is perfectly synchronized to the PWM dimming frequency.

Figure 4. Block diagram of TPS61042 with high level of integration

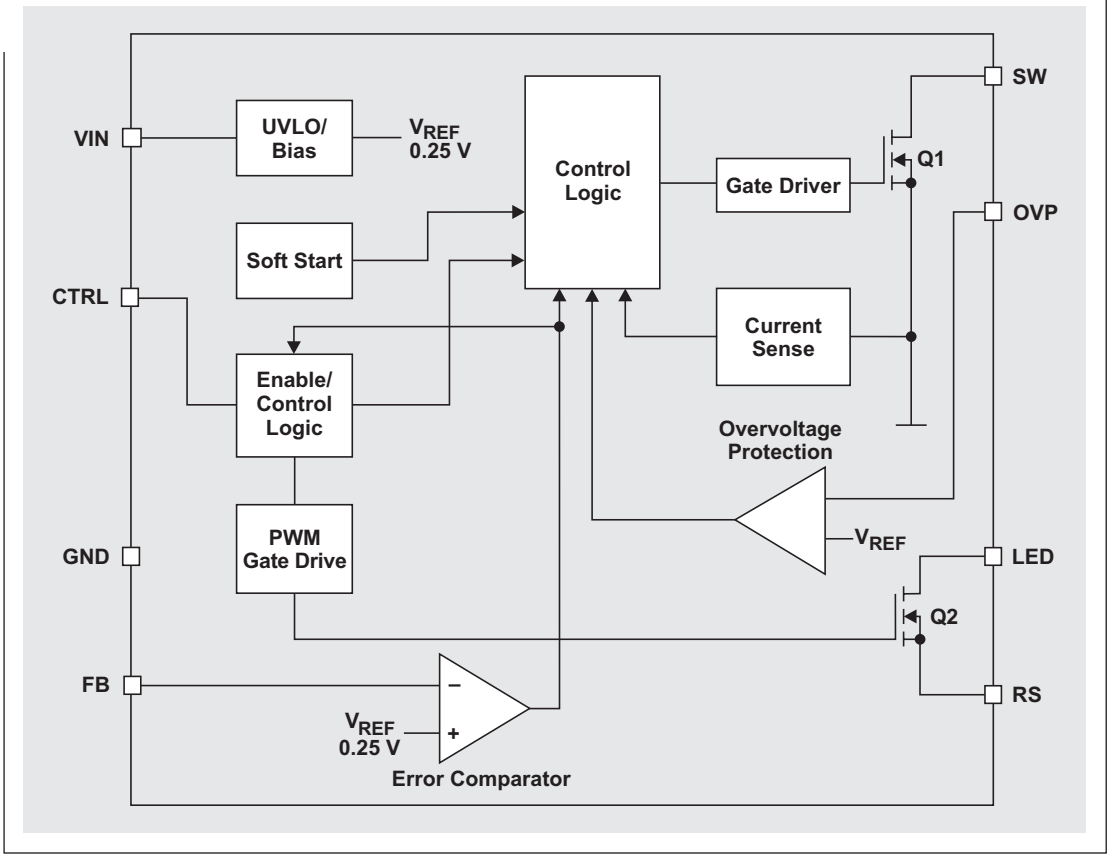
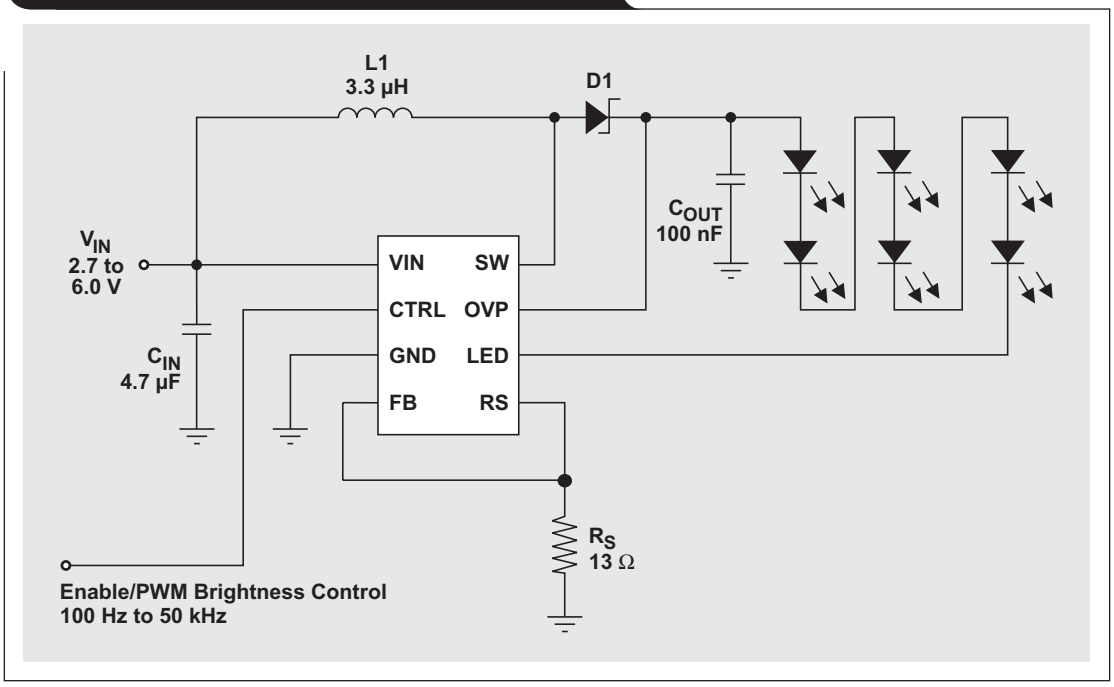


Figure 5. Typical TPS61042 LED-driver solution



Overvoltage protection is also integrated into the IC. Most seasoned power-supply designers will note the absence of an error amplifier and any associated compensation circuitry. This function has been replaced by the error comparator. This IC operates with hysteretic-control feedback topology, which requires no compensation and is inherently stable. Not shown in the block diagram is the physical size of the IC. All control circuitry and features are integrated into a 3 mm × 3 mm QFN package. Figure 5 shows a typical LED-driver application that drives four LEDs with 20 mA of forward current and operates from an input voltage range of 1.8 to 6.0 V. The entire circuit consists of the control IC, two small ceramic caps, an inductor, a diode, and a current-sense resistor. This small circuit shows the high level of integration that is achieved with today's LED drivers. The primary power-supply functions and the secondary features such as load disconnect, overvoltage protection, and PWM dimming have been implemented with a control IC and five small surface-mount passive components.

Related Web sites

analog.ti.com
www.ti.com/sc/device/TPS61042

Estimating available application power for Power-over-Ethernet applications*

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Introduction

Many existing Ethernet devices are being converted from wall-adapter power sources to utilize the newly released IEEE 802.3af Power-over-Ethernet (PoE) standard. Power-system efficiency formerly was not much of an issue with a wall adapter—but PoE changes that. Applications whose functional circuits begin to draw power in the 10-W range need close control of their power usage. This article helps the designer determine how much power is available when an application operates from a PoE source.

First we will determine the net power available once the functions required by the 802.3af standard are performed. Then a method of modeling the usual DC/DC converters to compute the power available for the applications circuits will be presented, with two example topologies for comparison. The modeling process allows the designer to identify topology and technology issues before the first circuit is designed. In this discussion, application circuits are considered to be everything in the powered device (PD) except the PoE front end and DC/DC converters.

PoE front-end losses

Figure 1 is a basic block diagram that shows the interconnection of the power-source equipment (PSE) through the DC/DC converter and application circuits. Calculations yielding the results in Table 1 assume that the PSE output (44 V minimum) is connected through 20 Ω of cable into a PD. The PD front end has a transformer (1 Ω total, with

Table 1. Analysis of PoE distribution and front-end losses

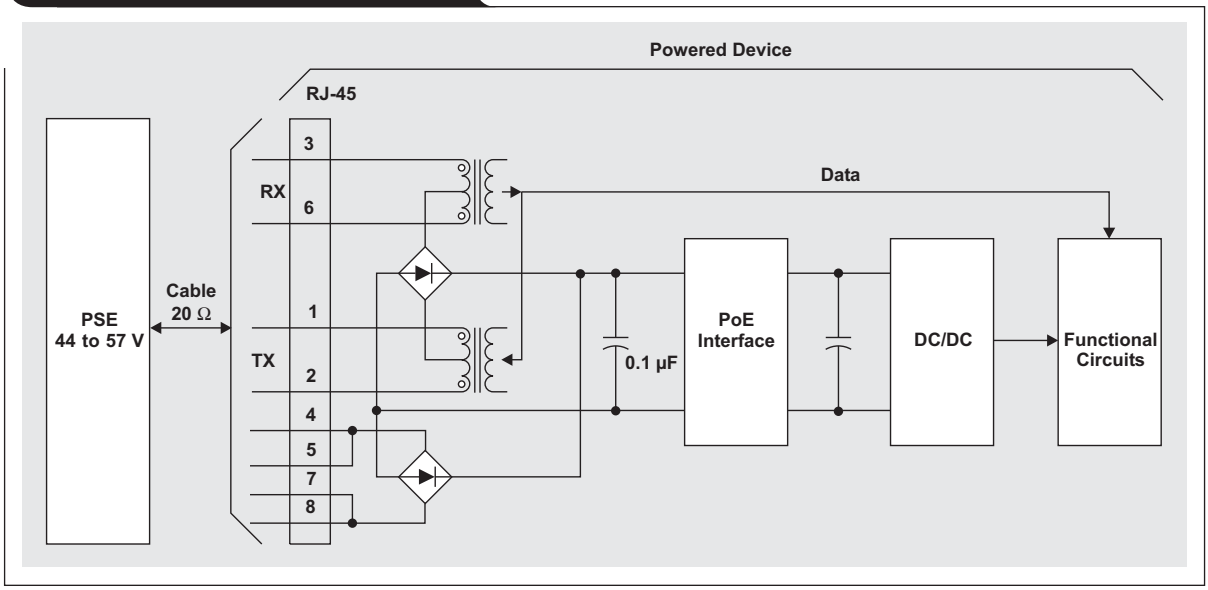
PARAMETERS	MIN	TYP	MAX
PSE output (V)	44	—	57
Distribution resistance (Ω)	—	—	20
Source power (W)	—	—	15.4
PD average current (A)	—	—	0.35
Constants			
Diode forward drop (V)	—	0.8	—
Transformer resistance (Ω)	—	—	1
PD-controller switch resistance (Ω)	—	1	—
PD-controller bias power (A)	—	0.0012	—

LOSS SOURCE	LOSS (W)	AVAILABLE POWER (W)
		15.40**
Distribution	2.45	12.95
Input diode	0.56	12.39
Input transformer	0.06	12.33
PD-controller switch	0.12	12.21
PD-controller bias	0.04	12.16

**Total PoE power available

*An edited version of this article was published December 3, 2003, on PlanetAnalog.com, an *EE Times* online community.

Figure 1. Basic PoE block diagram



0.5 Ω each side to the center tap), a full-wave bridge, and a hot-swap controller (or PD controller) with a 1-Ω switch (FET) in series.

There is a maximum of 12.16 W available for PD functional circuits. The 802.3af standard defines the 2.45-W worst-case cable loss, and the input diode bridge dominates the additional front-end losses of 0.78 W.

Modeling of power-conversion stage

Simple modeling techniques allow the designer to understand the effects of different topology and technology choices before an actual design is done. Simple efficiency assumptions give quick, qualitative results to allow topology comparison and optimization. The end results will be only as good as the assumptions, so the designer should always allow some margin by specifying the available power below these results.

First, let's look at the baseline of a single-stage conversion to one output voltage. A single 3.3-V output converter at 90% efficiency will yield an available output power of $0.9 \times 12.16 = 10.9$ W. Although the 90% efficiency may be viewed as optimistic, it does provide a baseline for comparison to other topologies.

Next we will estimate the output power available from a more complex power supply. A simple modeling technique is used to study how the topology and technology for each regulator affect output power. Output voltages of +5 V at 0.2 A, 3.3 V at 2 A, 2.5 V at 0.25 A, and 1.8 V at 0.25 A are assumed. These add up to a reasonable 9.6 W.

Figure 2 shows two possible supply architectures and technology choices. Topology 1 represents adaptation of an existing appliance design that had a 12-V wall adapter, which was replaced with a 48-V to 12-V front end. Topology 2 attempts to maximize the available power.

To evaluate the model, start at the right-most regulators, calculating their loss and total input power, and then use these results to evaluate the next regulator to the left. For simplification, assume 90% efficiency for a switcher and no bias current for linear regulators. These calculations are summarized for the regulator types as follows.

Definitions

I_{OUT} = application load current
$P_{IN\_Next\_Stage}$ = power drawn by a downstream converter or linear regulator

Linear regulator stage

$$P_{OUT} = \left(V_{OUT} \times I_{OUT}\right) + P_{IN\_Next\_Stage}$$

$$P_{IN} = V_{IN} \times \frac{P_{OUT}}{V_{OUT}}$$

$$P_{Loss} = P_{IN} - P_{OUT}$$

Switching regulator stage

$$P_{OUT} = \left(V_{OUT} \times I_{OUT}\right) + P_{IN\_Next\_Stage}$$

$$P_{IN} = \frac{P_{OUT}}{\text{Efficiency}}$$

$$P_{Loss} = P_{IN} - P_{OUT}$$

Figure 2. Alternative supply topologies

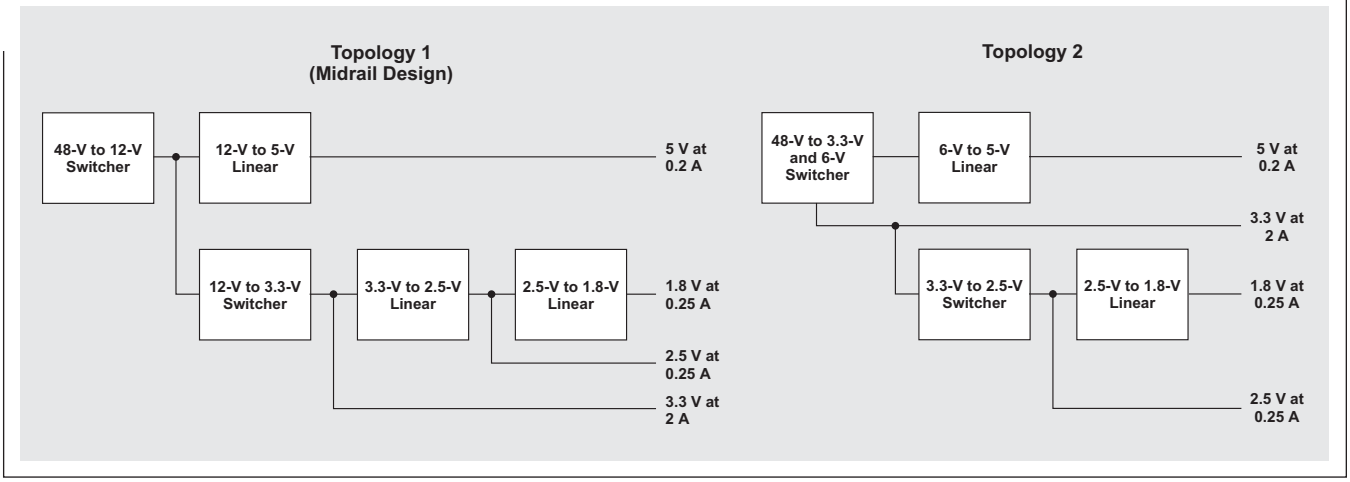


Table 2. Topology 1 model

MODEL COMPONENTS	OUTPUT VOLTAGE (V)	REGULATOR TYPE	INPUT VOLTAGE (V)	REGULATOR EFFICIENCY (%)	APPLICATION CURRENT (A)	ADDITIONAL OUTPUT LOAD (W)	COMPUTED INPUT POWER (W)	STAGE LOSS (W)
Chain 1	1.8	Linear	2.5	—	0.25	0.00	0.63	0.18
	2.5	Linear	3.3	90	0.25	0.63	1.65	0.40
	3.3	Switcher	12	90	**1.83**	1.65	**8.54**	**0.85**
Chain 2	5	Linear	12	—	0.2	0.00	2.40	1.40
First-stage input power	—	Switcher	48	90	0	**10.94**	**12.16**	**1.22**
Total loss								**4.05**
Apparent efficiency = **67%** Available output power = **8.11 W**								

Table 3. Topology 2 model

MODEL COMPONENTS	OUTPUT VOLTAGE (V)	REGULATOR TYPE	INPUT VOLTAGE (V)	REGULATOR EFFICIENCY (%)	APPLICATION CURRENT (A)	ADDITIONAL OUTPUT LOAD (W)	COMPUTED INPUT POWER (W)	STAGE LOSS (W)
Chain 1	1.8	Linear	2.5	—	0.25	0.00	0.63	0.18
	2.5	Switcher	3.3	90	0.25	0.63	1.39	0.14
	3.3	—	—	100	2.532	1.39	9.74	0.00
Chain 2	5	Linear	6	—	0.2	0.00	1.20	0.20
First-stage input power	—	Switcher	48	90	0	10.94	12.16	1.22
Total loss								1.73
Apparent efficiency = 86% Available output power = 10.43 W								

Using data in Table 2, let's go through the calculations for the Topology 1 model shown in Figure 2. Looking at the lower branch, Chain 1, data in Table 2, start with the 1.8-V regulator's input power and loss; notice that there is no next-stage power. The 2.5-V regulator is computed similarly, with the output power now comprised of the 0.25 A to the load multiplied by 2.5 V, plus the 1.8-V regulator's input power previously computed. The 3.3-V switching regulator's input power is the total output power divided by the efficiency of this stage (0.9%). The power loss of the 3.3-V regulator is still the input power minus the output power. The upper branch is computed in a like manner with the Chain 2 data. The 48-V to 12-V regulator's parameters are calculated like those of the 3.3-V regulator, where the total output power is the sum of the upper- and lower-branch input powers. To get a handle on the topology's performance, the individual losses are summed and the apparent efficiency is computed as

$$\text{Efficiency} = 1 - \frac{\text{Total\_Losses}}{\text{Input\_Power}}.$$

The available output power in Table 2 is the input power minus all the computed individual losses.

Topology 1's input power exceeds the amount available. To provide a more interesting result, the 3.3-V load shown was adjusted until the input power was 12.16 W. Bold values in Table 2 reflect the reduction of the 3.3-V supply load from 2 A to 1.83 A.

Topology 2 is modeled with data in Table 3 much as Topology 1, with a small wrinkle. A dummy 3.3-V regulator is modeled with an efficiency of 1 for proper totaling of the power and loss.

The efficiency of 90% used for the 48-V to 3.3-V converter in Topology 2 is a fairly optimistic number for a practical, synchronous output-rectifier circuit.

Conclusion

After the 802.3af standard functions are considered, 12.16 W is the maximum power available for other electronics, including regulator losses.

The effects of topology and technology choices for PoE applications are quite startling. Topology 1 makes only 8.11 W available to the application's circuits, while Topology 2 makes 10.43 W available. This is an increase of 28%. The baseline single-output converter provided 10.9 W, so all the processing represented by the additional three outputs in Topology 2 cost only 0.47 W! Using a diode output converter (85% efficiency) instead of a synchronous rectifier for the 3.3-V converter drops the available power by 0.61 W.

This modeling technique allows the designer to calculate available output power rapidly based on topology and technology choices. The designer can use this information to trade off available power, complexity, and cost.

Related Web site

analog.ti.com

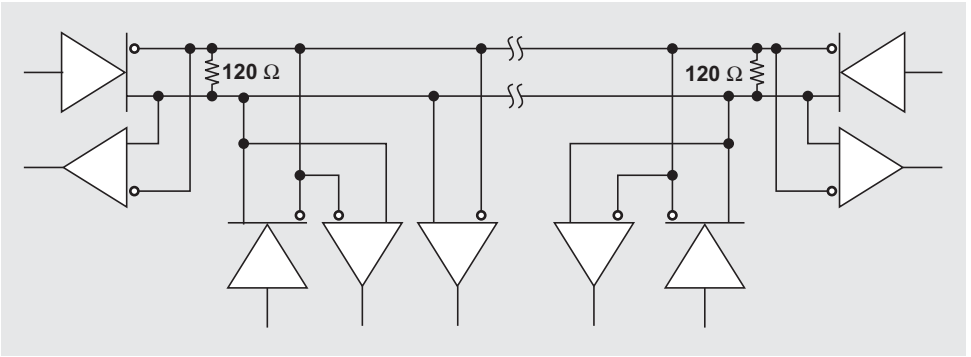
The RS-485 unit load and maximum number of bus connections

By Kevin Gingerich (Email: k-gingerich@ti.com)
High-Performance Analog/Interface Products

Introduction

TIA/EIA-485 (RS-485) is a popular electrical standard for data interchange over a multipoint differential bus. Multipoint buses are three or more stations connected to a common transmission medium that allow bidirectional data communication between any two nodes. Figure 1 schematically shows an example of a multipoint bus.

Figure 1. Schematic of an example multipoint bus



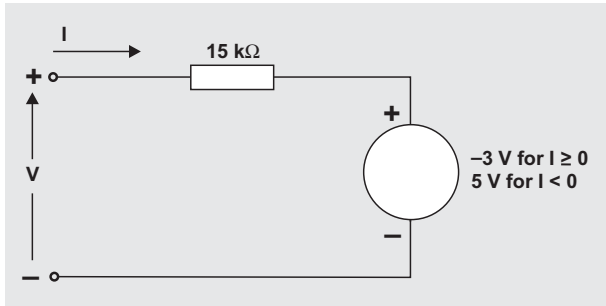
Maintaining a practical limit to the output-drive capability of an RS-485 driver requires that a limit be imposed on the steady-state load presented by the bus. This in turn constrains the input resistance of stations and, ultimately, the maximum number of connections.

RS-485 does not specify the maximum number of bus connections. Instead, the standard defines the steady-state electrical load presented by a bus connection in unit loads. The following paragraphs explain the unit load and how it is used to determine the maximum number of nodes connected to an RS-485 bus segment.

The unit load

TIA/EIA-485-A defines a unit load as a 15-kΩ resistor connected to a –3- or 5-V source (see Figure 2). The –3-V case applies for positive input current, and the 5-V case applies for negative bus current. The definition and model are valid for input voltages from –7 to 12 V to account for driver outputs between 0 and 5 V, with up to ±7 V of common-mode noise voltage between a driver and receiver.

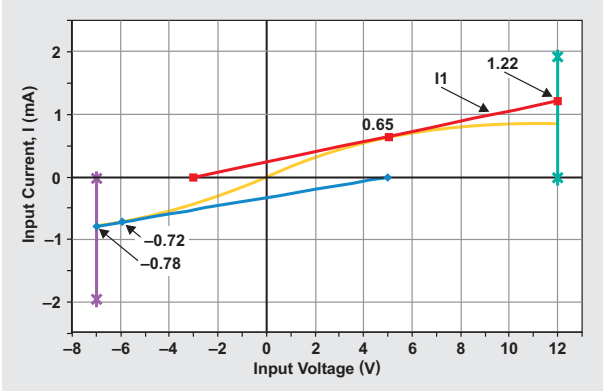
Figure 2. Electrical model of 1 unit load



The number of unit loads (nUL) presented by any proposed connection to the RS-485 bus is then determined as the ratio of its measured input current and the current of 1 unit load. Since the current of 1 unit load is a function of voltage, the input current must be measured and the ratio determined throughout the entire –7- to 12-V input-voltage range, with the highest ratio determining the unit-load rating.

Figure 3 shows a hypothetical example where the measured input current of a circuit is nonlinear. It can be shown (see sidebar on next page) that, at its maximum value, the ratio of the measured and unit-load current is equal to the ratio of the slopes of the two functions and lies on a line with an intercept at –3 V for positive current and 5 V for negative current. Conceptually, this amounts to rotating a line pivoted at I = 0 mA and V = –3 V until it is tangent to the curve of measured positive current versus

Figure 3. Example unit-load analysis



Proof that nUL is the slope ratios

Let the input current of a unit load be defined by f_1 (V) and the measured circuit by f_2 (V). The number of unit loads (nUL) is then

$$nUL = \frac{f_2(V)}{f_1(V)}$$

for –7 V < V < 12 V.

The maximum nUL occurs when the first derivative equals zero, or

$$\frac{d}{dV}\frac{f_2(V)}{f_1(V)} = \frac{1}{f_1(V)}\frac{d}{dV}f_2(V) - \frac{f_2(V)}{f_1^2(V)}\frac{d}{dV}f_1(V) = 0.$$

$$\frac{d}{dV}f_2(V) = \frac{f_2(V)}{f_1(V)}\frac{d}{dV}f_1(V).$$

$$\frac{f_2(V)}{f_1(V)} = \frac{\frac{d}{dV}f_2(V)}{\frac{d}{dV}f_1(V)}. \quad \textbf{(1)}$$

Therefore, the maximum nUL is equal to the ratio of the first derivative (slopes) of the input-current function.

The following equations are used to solve for the unit-load circuit:

$$f_1(V) = \frac{V+3}{15} \text{ mA or}$$

$$f_1(V) = \frac{V-5}{15} \text{ mA and } \frac{d}{dV}f_1(V) = \frac{1}{15} \text{ mho.}$$

Substituting these into Equation 1 yields

$$\frac{f_2(V)}{\frac{V+3}{15}} = \frac{\frac{d}{dV}f_2(V)}{\frac{1}{15}}$$

$$f_2(V) = \frac{d}{dV}f_2(V) \times (V+3)$$

or

$$\frac{f_2(V)}{\frac{V-5}{15}} = \frac{\frac{d}{dV}f_2(V)}{\frac{1}{15}}$$

$$f_2(V) = \frac{d}{dV}f_2(V) \times (V-5).$$

These line equations mean that the input current where the nUL is maximum lies on a line that intersects the points I = 0 mA and V = –3 V for positive current and I = 0 mA and V = 5 V for negative current.

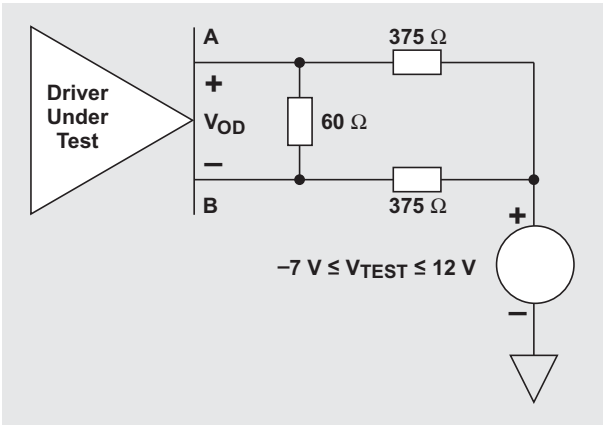
voltage. For negative currents, the line is pivoted at I = 0 mA and V = 5 V. In our example, the maximum ratio occurs at measured input currents of 0.65 mA and –0.72 mA.

The ratio and nUL may be calculated by dividing the measured value at the intercept by the value derived from solving the unit-load circuit; or, for convenience, the lines are often extended to the 12- or –7-V intercept. Since the slopes for 1 unit load and the tangential lines are constants, their ratios are constant and may be determined at any voltage. By definition, the current into 1 unit load at 12 V will be 1 mA, and at –7 V will be –0.8 mA. These values are respectively divided into the current-intercept values of the tangential lines at 12 V and –7 V, and the maximum number determines the nUL for the circuit. In the example, the input-current-versus-voltage characteristics of the hypothetical circuit result in 1.22 unit loads.

Maximum unit loads

The minimum output-drive capability of a standard RS-485 driver is established in clause 4.2.3 of TIA/EIA-485-A, which specifies a differential output voltage of at least 1.5 V with a common-mode load. Figure 4 shows a schematic of this test circuit.

Figure 4. Differential output voltages with a common-mode load



The 375-Ω resistors are certainly part of the common-mode load. What is not obvious is that the test voltage of –7 to 12 V actually represents a ±7-V common-mode noise source and a 0- to 5-V local supply voltage at the load(s). This is important in that the local supply is included in the unit-load determination for this test circuit. Figure 5 shows the common-mode test circuit with the insertion of a "local" ground used as the reference for the unit-load calculation.

To determine the unit load of this test circuit, we plot the input-current-versus-voltage function between point A or B and the "local" ground of Figure 5, then apply the unit-load definition described earlier. This is done in Figure 6, and we find that the current at the intercepts of the tangential lines is 32 mA at V = 12 V, and –32 mA at V = –7 V. By definition, this represents 32 unit loads and 40 unit loads, respectively.

Figure 5. Physical representation of the test circuit

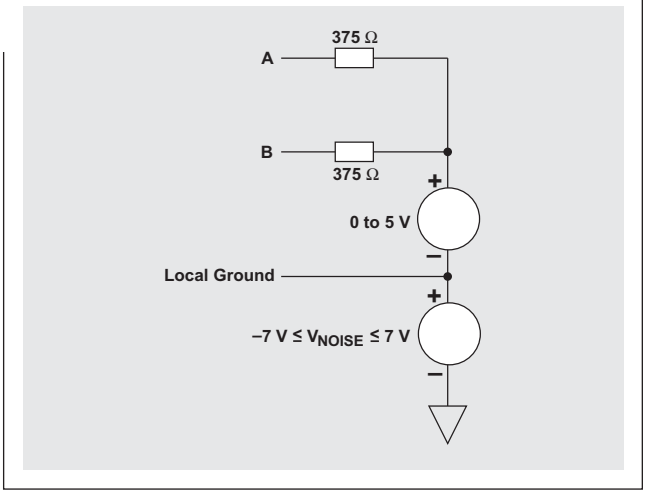
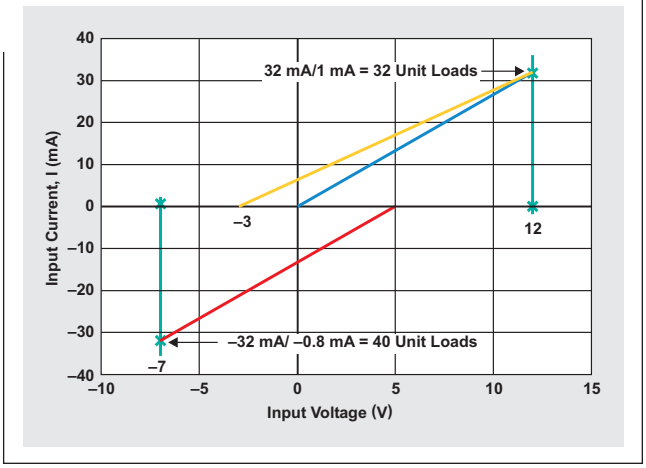


Figure 6. Unit load of common-mode test circuit



The reader may have noted the discrepancy between the unit-load model and the driver test circuit. One can only assume that this was an oversight or compromise by the authors of TIA/EIA-485. As tested, the unit-load model should consist of a 12-kΩ resistor to a 0- to 5-V source rather than 15 kΩ to a –3- to 5-V source. If we use this modified definition, the differential output voltage with common-mode load test of TIA/EIA-485-A ensures that a standard driver will work with 32 unit loads.

Using the unit load

Other than a refresher on analytic geometry, of what use is the unit-load concept to the designer of a data-interchange circuit? Primarily, it provides a single standard parameter for calculating the maximum number of connections and for specifying the input characteristics of possible line circuits. Since we know a driver will support 32 unit loads in a standard bus configuration, we need only divide 32 by the total number of nodes (N) to derive the maximum unit-load rating for each of the line circuits. For example, if 48 nodes were to be connected, each line receiver or transceiver would have to have no more than 0.67 unit loads (32/48).

The unit load also can be useful when nonstandard bus configurations are implemented. In addition to the differential termination of the differential signal pair, pull-up and pull-down resistors often are connected to the lines to provide a known bus state when all of the connected drivers are idle. The resistor values used for this fail-safe termination are usually around 1 kΩ. If so, this termination would consume 12 unit loads (12 mA at 12 V) out of the budget of 32 unit loads. This leaves 20 unit loads for the line circuits; and, if 48 nodes are still to be connected, each of the line circuits must now be no more than 0.42 unit loads (20/48).

Texas Instruments (TI) offers numerous options, some of which are shown in Table 1, for supporting a large number of RS-485 bus connections.

Table 1. Fractional unit-load devices from TI

UNIT LOADS	MAXIMUM NUMBER OF DEVICES ON A SINGLE BUS SEGMENT	PART NUMBER
0.5	64	SN65HVD05
		SN65HVD10
		SN65HVD20
		SN65HVD23
0.25	128	SN65LBC182
		SN65LBC184
0.125	256	SN65HVD06
		SN65HVD07
		SN65HVD08
		SN65HVD11
		SN65HVD12
		SN65HVD21
		SN65HVD22
		SN65HVD24

Conclusion

The unit load is a relative parameter that provides a basis for determining the maximum number of connections to an RS-485 bus segment or for specifying the input characteristics of line circuits. A standard RS-485 driver will handle 32 unit loads that could consist of 256 devices with a rating of ⅛ unit load.

Related Web sites

analog.ti.com

www.ti.com/sc/device/*partnumber*

Replace *partnumber* with SN65HVD05, SN65HVD06, SN65HVD07, SN65HVD08, SN65HVD10, SN65HVD11, SN65HVD12, SN65HVD20, SN65HVD21, SN65HVD22, SN65HVD23, SN65HVD24, SN65LBC182 or SN65LBC184

Op amp stability and input capacitance

By Ron Mancini (Email: rmancini@ti.com)
Staff Scientist, Advanced Analog Products

Introduction

Op amp instability is compensated out with the addition of an external RC network to the circuit. There are thousands of different op amps, but all of them fall into two categories: uncompensated and internally compensated. Uncompensated op amps always require external compensation components to achieve stability; while internally compensated op amps are stable, under limited conditions, with no additional external components.

Internally compensated op amps can be made unstable in several ways: by driving capacitive loads, by adding capacitance to the inverting input lead, and by adding in phase feedback with external components. Adding in phase feedback is a popular method of making an oscillator that is beyond the scope of this article. Input capacitance is hard to avoid because the op amp leads have stray capacitance and the printed circuit board contributes some stray capacitance, so many internally compensated op amp circuits require external compensation to restore stability. Output capacitance comes in the form of some kind of load—a cable, converter-input capacitance, or filter capacitance—and reduces stability in buffer configurations.

Stability theory review

The theory for the op amp circuit shown in Figure 1 is taken from Reference 1, Chapter 6. The loop gain, Aβ, is critical because it solely determines stability; input circuits and sources have no effect on stability because inputs are grounded for the stability analysis. Equation 1 is the loop-gain equation for the resistive case where Z = R.

$$A\beta = \frac{aR_G}{R_F + R_G} \qquad (1)$$

Beware of Equation 1; its simplicity fools people because they make the assumption that A = a, which is not true for all cases. Stability can be determined easily from a plot of the loop gain versus frequency. The critical point is when the loop gain equals 0 dB (gain equals 1) because a circuit must have a gain ≥1 to become unstable. The phase margin, which is the difference between the measured phase angle and 180°, is calculated at the 0-dB point. A typical open-loop-gain curve for the TLV278x family of op amps is used as a teaching example and is shown in Figure 2.

The op amp's open-loop gain and phase (a in Equation 1) are represented in Figure 2 by the left and right vertical axes, respectively. Never assume that the op amp open-loop-gain curve is identical to the loop gain because external components have to be accounted for to get the loop-gain

Figure 1. Equation 1 can be written from the op amp schematic by opening the feedback loop and calculating gain

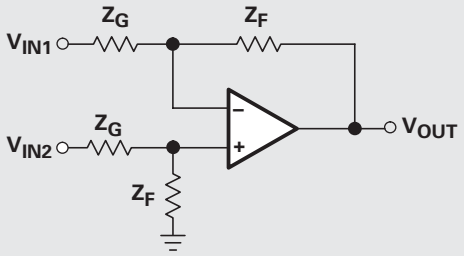
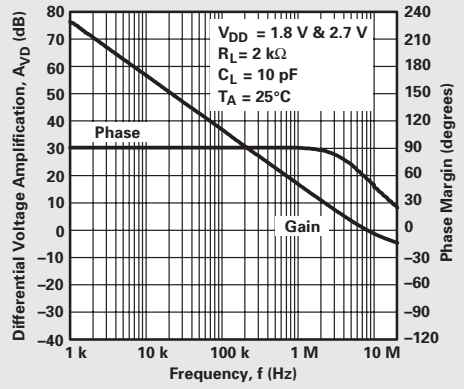


Figure 2. Open-loop-gain/phase curves are critical stability-analysis tools

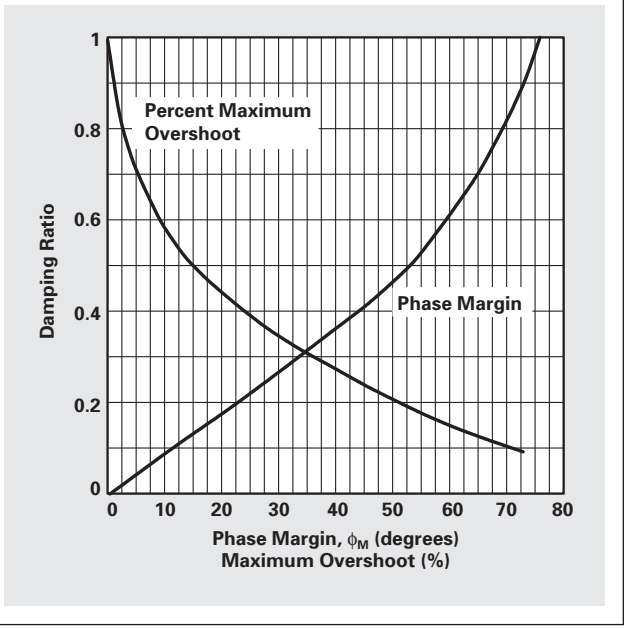


curve. When R_F = 0 and R_G = ∞, the op amp reduces to a noninverting buffer amp (unity gain) and the loop gain becomes equal to the op amp open-loop gain. We can obtain the buffer phase margin directly from Figure 2 by tracing the gain line down from its vertical intercept (at approximately 78 dB) to where it crosses the 0-dB line at approximately 8 MHz. Then we can trace the 8-MHz line up until it intersects the phase curve, and read the phase margin as approximately 56°. This plot was made with phase margin, but many plots are made instead with phase shift. For plots made with phase shift, the phase shift must be subtracted from 180° to obtain the phase margin.

Now that we have the phase margin, what can we do with it other than to say that the circuit does not oscillate?

Figure 3 is a plot of phase margin and percent maximum overshoot versus a dummy variable, the damping ratio. Enter this plot at a phase margin of 56° and go up to the phase curve intersection. At this point, go horizontally (constant damping ratio) to the intersection of the overshoot curve, and then drop down to read an overshoot of approximately 11%. This plot enables the designer to predict the transient step response from the phase margin, and transient response is a measure of relative stability.

Figure 3. Phase margin/percent overshoot versus damping ratio



The external resistors come into play when the op amp is conFigured as an inverting, noninverting, or differential amplifier. When $R_F = R_G$, Equation 1 reduces to $A\beta = a/2$; and the vertical intercept for the amplifier reduces from that of the buffer by 6 dB. Although the vertical intercept has changed, the pole location remains constant because gain is not tied to phase. The 0-dB crossover frequency changes to approximately 3 MHz because of the gain drop; the phase margin increases to approximately 87°; and the percent overshoot is negligible. Notice that the buffer is less stable than any of the amplifier circuits and that, at the same phase margin, the inverting gain is –1 while the noninverting gain is 2.

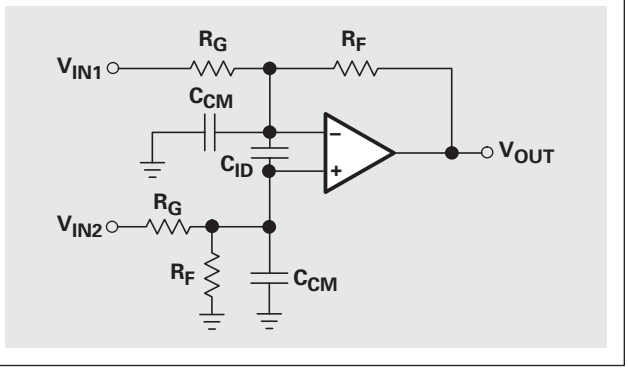
Added input capacitance and its effect

When input capacitors are added to the circuit (see Figure 4), they cause a pole to occur in the loop gain, as shown in Equation 2.

$$A\beta = \frac{aZ_G}{Z_G + R_F} = \frac{aR_G}{R_G + R_F} \times \frac{1}{R_G \| R_F C_{IN} + 1} \qquad (2)$$

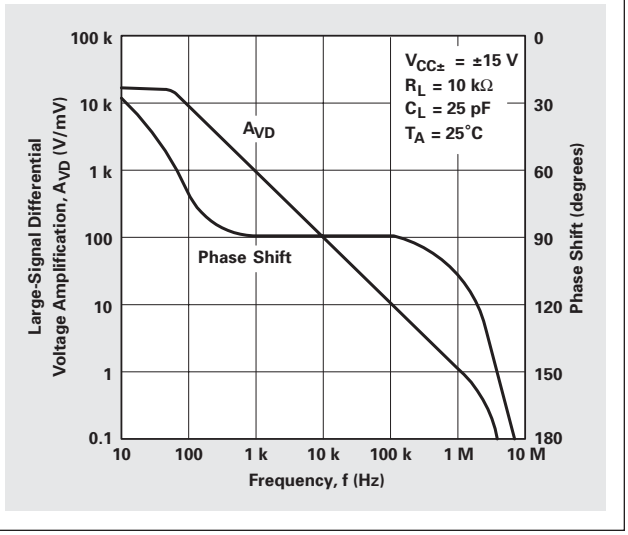
The input capacitor, C_{IN}, is the summation of all the inverting input capacitances, and it adds a pole to the loop

Figure 4. Input capacitance includes IC internal, lead, and PCB capacitance



gain. Adding a pole to the loop gain does not always change the stability because the pole location and its added phase shift may not affect the phase margin. Consider the case where the pole is located at a very high frequency—say, 100 MHz—for the TLV278x. Notice from Figure 2 that the op amp open-loop gain is so low above 10 MHz that the overall gain can never equal 1, so the added pole is of no value. The case where the pole is located at a very low frequency—say, 0.001 Hz—is harder to calculate because the low-frequency response is not shown in Figure 2. However, we can be sure that the phase shift is close to zero at this frequency. A pole with a frequency intercept that low would cause the gain to be down 120 dB at 1 kHz, and again the loop gain would be less than 1 before the phase margin went to zero. An op amp open-loop gain/phase plot that shows low-frequency response is shown in Figure 5. Notice that the phase shift (not phase margin in this plot) approaches zero at low frequencies. In addition, notice that the phase shift approaches 180° at very high frequencies and that the gain is given in ratios rather than in decibels.

Figure 5. Gain/phase plots of medium-frequency op amps show frequency extremes

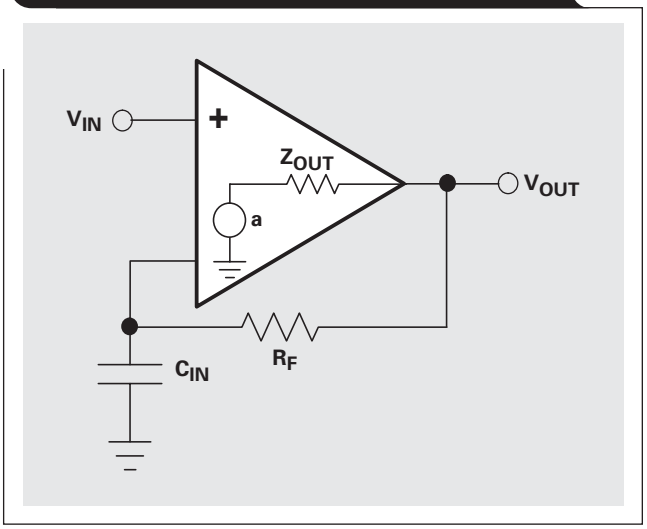


The DC gain in Equation 2 remains the same as it was without an input capacitor, but the pole is added at $f = 1/(2\pi R_F \| R_G C_{IN})$. If this pole occurs at approximately 3 MHz, it reduces the gain by 3 dB and adds a 45° phase shift at that frequency. Using C_{IN} = 20 pF and $R_G \| R_F$ = 2.7 kΩ yields a 3-dB frequency of 2.94 MHz, so it is reasonable to assume a pole frequency of 3 MHz. The gain in Figure 4 must be moved down 9 dB to account for the resistors and the pole. The new 0-dB crossover frequency is 2 MHz, and the phase margin at 2 MHz (as shown in Figure 4) is 89°. The pole phase shift of 45° must be subtracted from the curve phase margin to obtain the final circuit phase margin; thus $\phi = 89° - 45° = 44°$. The percent overshoot corresponding to the 44° phase margin is 24.45%. Adding C_{IN} reduces the phase margin from 87° in the purely resistive case to 44° with input capacitance. If the op amp initially had less than a 44° phase margin, the circuit would be unstable rather than just bouncy.

If the resistor values were larger than 5.4 kΩ, the pole would move down in frequency. The exact pole location that does the most damage to stability is hard to calculate because the phase is a nonlinear tangent function. In this case, it is best to move the resistors down in value to about 1 kΩ, thus moving the pole to 8 MHz and reducing the added phase shift to about 14°. A second problem crops up in the noninverting configuration because C_{ID} couples a portion of the input signal to the inverting input. This action reduces the common-mode rejection capability and introduces high-frequency distortion.

The buffer circuit with an input capacitance is shown in Figure 6. Notice that the input capacitance includes the output capacitance and load capacitance in the absence of a feedback resistor, and that the output impedance, Z_{OUT}, comes into play.

Figure 6. Input, output, and load capacitors are in parallel in the buffer circuit

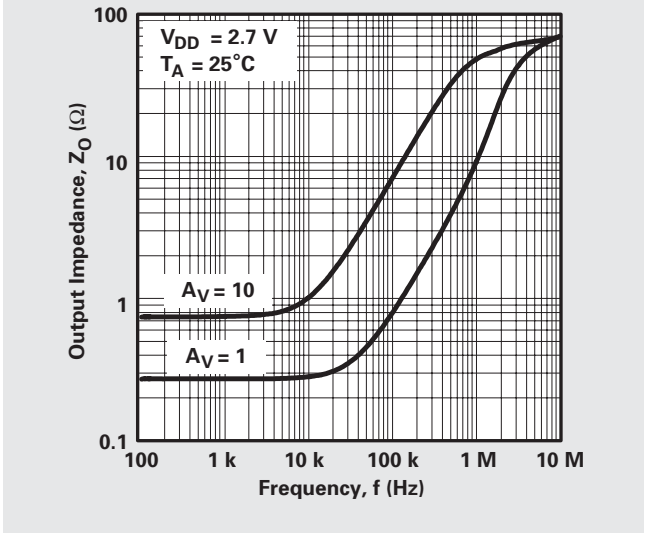


The buffer loop gain is given as

$$A\beta = \frac{a}{(R_F + Z_{OUT})C_{IN} + 1}. \quad (3)$$

First, consider the case when R_F = 0; Z_{OUT} is obtained from Figure 7 as 70 Ω at 8 MHz. Assuming that the input, output, and load capacitance is 100 pF, the pole frequency is located at 22.7 MHz; and this pole adds a 19.4° phase shift at the 0-dB crossover frequency. This added phase shift subtracts directly from the previously calculated phase margin of 56° because the pole attenuation doesn't

Figure 7. Op amp output impedance increases with increasing frequency



occur until after the 0-dB crossover frequency. This circuit has a phase margin of 56° – 19.4° = 36.6°, leading to an overshoot of 33%.

When R_F = 1 kΩ, the $R_F C_{IN}$ pole is located at 8 MHz; so it becomes dominant. Under these conditions, the gain curve moves down 3 dB and the phase shift is increased 45°. Moving the gain curve down 3 dB yields an 80° phase margin at f = 4 MHz. Subtracting 45° plus 19.4° from 80° yields a phase margin of 15.6°, and the overshoot increases to approximately 50%. It is obvious that increasing the value of R_F makes it dominant over Z_{OUT} and will quickly make the circuit oscillate.

C_F increases stability

Input and output capacitors always decrease stability. Input capacitors are a pole in the open-loop transfer function, but they are a zero in the closed-loop transfer function. The closed-loop zero increases the circuit (not the op amp) bandwidth, so sometimes input capacitors are added to the circuit to improve high-frequency response.

A capacitor placed in parallel with the feedback resistor, C_F, introduces a zero into the loop gain:

$$A\beta = \frac{aR_G}{R_F + R_G} \times \frac{R_F C_F + 1}{R_F \left\| R_G \left(C_F + C_G\right) + 1\right.} \quad \textbf{(4)}$$

When the closed-loop gain is greater than 1 and C_F is greater than C_G, the zero precedes the pole. In this case, which is not unusual, the zero contributes a positive phase shift to the loop-gain plot, causing an increase in stability. The more the zero leads the pole, the more stable the circuit becomes; but the pole always ends up canceling the zero. The idea is to place the zero so that we achieve the required overshoot and then to accept the pole location. The open-loop zero translates to a closed-loop pole; thus C_F always decreases high-frequency performance. Optimal performance is gained when the acceptable overshoot is obtained at an acceptable frequency response.

Conclusion

The addition of input, output, or load capacitance to an op amp circuit decreases stability, which leads to overshoot in the time domain. The stability decrease is worse for a buffer than for other amplifier configurations. Reducing the resistance value that makes up the RC circuit reduces the effect of the capacitance; this effect leads to the rule of thumb that high frequencies and low resistance go together. Input capacitance is easily compensated by adding a feedback capacitor into the circuit. The value of the feedback capacitor should be just large enough to achieve the desired overshoot response, because larger values cause a loss of high-frequency performance.

Reference

1. Ron Mancini, *Op Amps For Everyone* (Newnes Publishers, 2003). An earlier 2002 edition is available at www-s.ti.com/sc/techlit/slod006

Related Web sites

analog.ti.com
www.ti.com/sc/device/TLV278x

Integrated logarithmic amplifiers for industrial applications

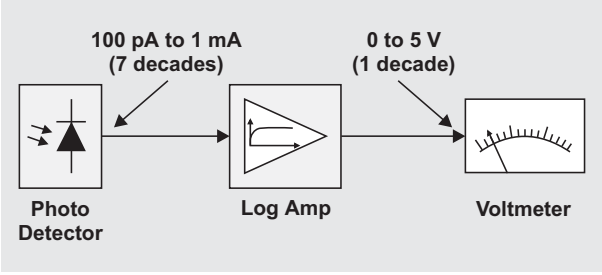
By Thomas Kugelstadt (Email: tk@ti.com)
Senior Systems Engineer, Industrial Systems

Many industrial applications measure physical quantities over a wide dynamic range. These applications use logarithmic amplifiers (log amps) to match a transmitter's dynamic output to the linear input range of a signal gauge. Figure 1 shows a typical signal chain to measure photo currents over a dynamic range of seven decades.

Log amps of the past were built with hybrid techniques. Today's CMOS technology enables the integration of the logging circuit and additional support functions, such as voltage references and uncommitted op amps, into a single chip.

This article describes the operation and architecture of integrated log amps and provides two application examples using the Texas Instruments (TI) LOG112 and LOG2112.

Figure 1. Matching a sensor's dynamic output to the linear input of a voltmeter



Operation

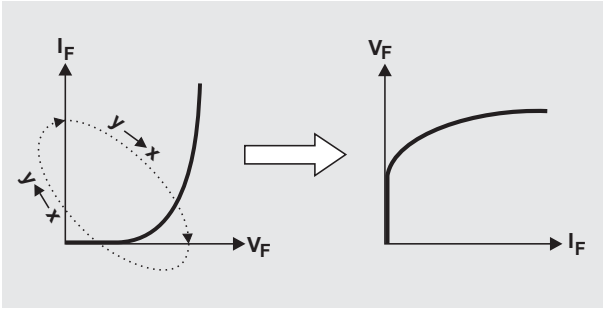
A log amp makes use of the logarithmic relationship between the voltage and current of a forward-biased diode. Figure 2 shows the characteristic of the forward current, given by the exponential function

$$I_F = I_{S(T)} \times \left(e^{\frac{V_F}{m \times V_T}} - 1 \right), \quad (1)$$

where V_F and I_F are the forward voltage and forward current of the diode, respectively; I_S is the theoretical reverse-saturation current; m is a correction factor; and V_T is the temperature-equivalent voltage. Exchanging the x for the y axes and vice versa yields the forward voltage as a logarithmic function of the forward current. Mathematically, this corresponds to solving Equation 1 for V_F:

$$V_F = m \times V_T \times \ln\left(\frac{I_F}{I_S} - 1 \right). \quad (2)$$

Figure 2. Diode characteristic in exponential and logarithmic form



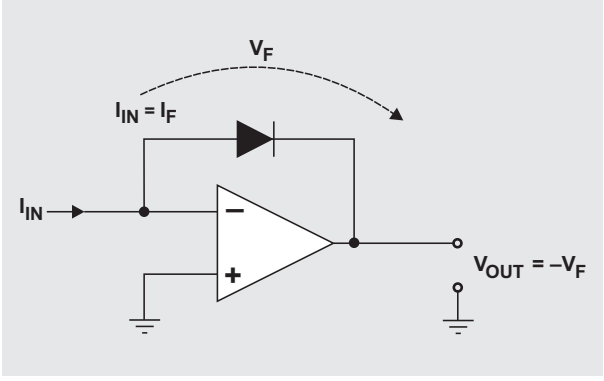
For a forward-biased diode, the forward current is larger by far than the reverse current ($I_F >> I_S$). Thus, Equation 2 simplifies to

$$V_F = m \times V_T \times \ln \frac{I_F}{I_S}. \quad (3)$$

A simple log amp whose transfer function satisfies Equation 3 is shown in Figure 3. The op amp operates as an inverting amplifier with a feedback diode. With the diode being virtually anode-grounded, the op amp needs to generate a negative output voltage to forward bias the diode. For a given input current, I_{IN}, the corresponding output voltage, V_{OUT}, is

$$V_{OUT} = -m \times V_T \times \ln \frac{I_{IN}}{I_S}. \quad (4)$$

Figure 3. Log amp with diode



The drawback of this circuit is that V_{OUT} depends not only on I_{IN} but also on m, $I_{S(T)}$, and V_T, all of which are either current- or temperature-dependent.

- The correction factor, m, takes into account the deviation between the diode characteristic and Shockley's simplified theory of diodes. However, m strongly depends on the forward current, thus varying its value between 1 and 2.
- The reverse-saturation current, I_S, is temperature-dependent. For a constant forward current, I_S doubles with every 10-K increase in temperature. Thus, for a 100-K rise in temperature, I_S increases by a factor of 1000.
- The temperature-equivalent voltage, $V_T = k \times T/e_0$, increases linearly with temperature. With Boltzman's constant $k = 1.38 \times 10^{-23}$ J/K, the electron charge $e_0 = 1.6 \times 10^{-19}$ C, and an ambient temperature of T = 296 K (23°C), V_T yields

$$V_T = \frac{1.38 \times 10^{-23}\ \text{J/K} \times 296\ \text{K}}{1.6 \times 10^{-19}\ \text{C}} = 25.5\ \text{mV}.$$

When the circuit operates at a constant temperature, the impact of m still limits the measurable input range to 1 or 2 decades of acceptable accuracy. To eliminate m, the diode is replaced by a transistor (Figure 4). Its exponential transfer characteristic in Figure 5 is similar to that of a diode. In contrast to a diode, however, the correction factor equals 1 and simplifies Equation 4 to

$$V_{OUT} = -V_T \times \ln\frac{I_C}{I_{ES}}, \text{ or } V_{BE} = V_T \times \ln\frac{I_C}{I_{ES}}. \quad \textbf{(5)}$$

The input current, I_{IN}, becomes the collector current, I_C; and I_S becomes the emitter reverse-saturation current, I_{ES}. The elimination of m increases the measurable input range to several decades. V_{OUT}, however, is still temperature-dependent via $I_{ES(T)}$ and V_T. Therefore, it is impossible to determine whether a change in V_{OUT} is caused by the input current or by a change in temperature.

Figure 4. Log amp with transistor

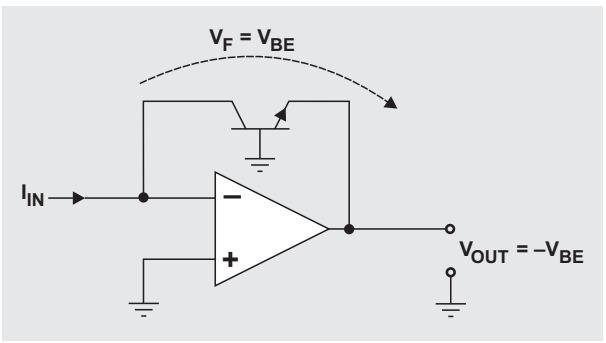
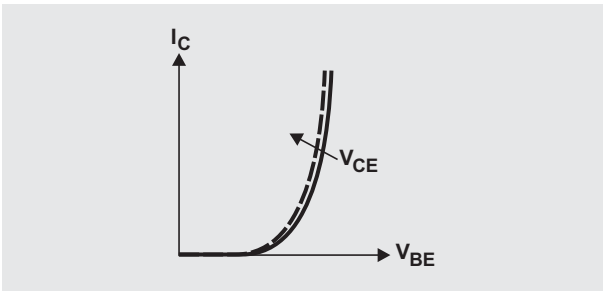


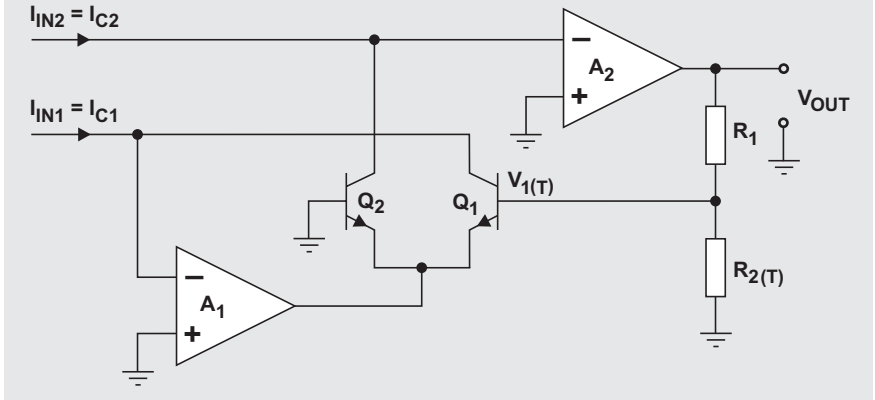
Figure 5. Transistor input characteristic



To avoid output changes due to temperature, the temperature-compensated log amp in Figure 6 is required. Here, generating the difference of two logarithms eliminates I_{ES}. From the previous example, we take the logarithmic relationship between the basis-emitter voltage, V_{BE}, and the collector current, I_C, for both transistors, Q_1 and Q_2:

$$V_{BE1} = V_T \times \ln\frac{I_{C1}}{I_{ES1}}, \text{ and } V_{BE2} = V_T \times \ln\frac{I_{C2}}{I_{ES2}}.$$

Figure 6. Temperature-compensated log amp



The two logging transistors build a difference amplifier whose output voltage, V_1, yields the difference of both base-emitter voltages:

$$V_1 = V_{BE1} - V_{BE2} = V_T \times \ln\frac{I_{C1}}{I_{ES1}} - V_T \times \ln\frac{I_{C2}}{I_{ES2}}. \quad (6)$$

With matched and isothermal transistors, $I_{ES1} = I_{ES2} = I_S$, and Equation 6 simplifies to

$$V_{1(T)} = V_T \times \ln\frac{I_{C1}}{I_{C2}}. \quad (7)$$

A remaining temperature dependency exists via only V_T. Via the voltage divider, R_1 and R_2, V_1 represents only a part of the entire circuit's output voltage, V_{OUT}:

$$V_{OUT(T)} = \left(1 + \frac{R_1}{R_2}\right) \times V_1 = \left(1 + \frac{R_1}{R_2}\right) \times V_T \times \ln\frac{I_{C1}}{I_{C2}}. \quad (8)$$

To compensate for the effect of V_T, R_2 is replaced by a temperature-dependent resistor with a positive temperature coefficient. This keeps

$$\left(1 + \frac{R_1}{R_{2(T)}}\right) \times V_T$$

constant over a certain temperature range. Practical values for the temperature coefficient vary between 3500 and 3700 ppm/K.

During the manufacturing process of log amps, the internal components and the temperature coefficient are trimmed to a fixed value. In addition, the natural logarithm is converted to $\log_{10}$ by applying a correction factor, n = 2.3, according to ln x = 2.3 × log x. The expression $(1 + R_1/R_{2(T)}) \times V_T \times 2.3$ becomes a constant, q, with the unit V/decade, simplifying the computation of V_{OUT} to

$$V_{OUT} = q \times \log\frac{I_{C1}}{I_{C2}}. \quad (9)$$

Log-amp structure

Figure 7 shows a block diagram of the integrated log amp, LOG112. The actual logging circuit consists of the amplifiers, A_1 and A_2, and the transistors, Q_1 and Q_2. The designation of the collector currents, I_{C1} and I_{C2}, changes to I_1 and I_2. In most cases, I_1 represents the input current to be measured, while I_2 is the reference current for the logarithmic computation.

The device minimizes external component count by providing a voltage reference and an uncommitted op amp, A_3, on-chip. The reference allows I_2 to be generated via an external resistor, R_{REF}. Via A_3, the logarithmic output signal, V_{LOGOUT}, can be filtered or further amplified. A_3 also can be configured as a comparator to provide a loss-of-signal indication.

The LOG112 is trimmed to provide an output voltage of 0.5 V per decade of input current. The device uses patented temperature compensation in which R_2 is laid out as an aluminum frame with a temperature coefficient of 3700 ppm/K, resulting in extremely temperature-stable operation. For an input current of 10 µA, for example, the output voltage changes by only 50 µV/K.

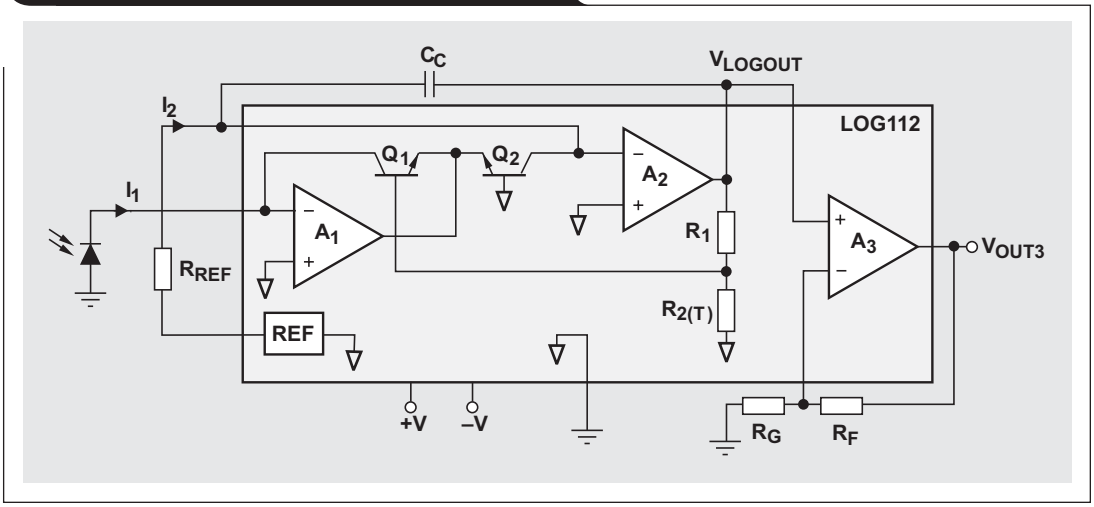
The output voltage of the log amp is made available at the V_{LOGOUT} pin:

$$V_{LOGOUT} = 0.5 \times \log\frac{I_1}{I_2},$$

with input currents ranging from 100 pA to 3.5 mA. The voltage at the V_{OUT3} pin is defined via the external gain, $G = 1 + R_F/R_G$, and yields

$$V_{OUT3} = G \times V_{LOGOUT} = G \times 0.5 \times \log\frac{I_1}{I_2}.$$

Figure 7. Internal block diagram of LOG112



Application examples

The circuit in Figure 8 controls the optical output power of a laser diode (LD_1). With the output power decreasing over the lifetime of the diode, a control loop that keeps the output power constant is required. In the feedback path, a fraction of the output signal is fed back via a photodiode (PD_1) and converted into electrical current.

The laser is calibrated by making the reference current, I_{REF}, equal to the PD_1 current, I_1. Deviations between I_{REF} and I_1 are converted into an error signal and applied to the bias input of the laser-diode driver. The driver then changes the bias current of LD_1 until the error signal diminishes to zero.

Another application example is the constant-gain control and gain adjustment of an op amp shown in Figure 9. Two log amps measure the optical input and output power of the amplifier. A difference amplifier subtracts the output signals of both log amps and applies an error voltage to the proportional-integral-derivative (PID) controller. The controller output adjusts a voltage-controlled current source (V_{CCS}), which then drives the actual pump laser. The amplifier operates at the desired optical gain when the error voltage at the PID output is zero.

Figure 8. Controlling the optical output power of a laser diode

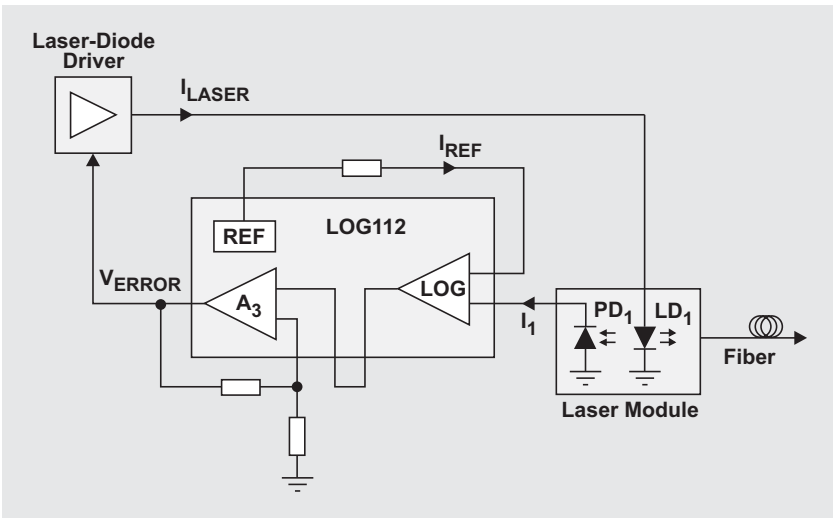
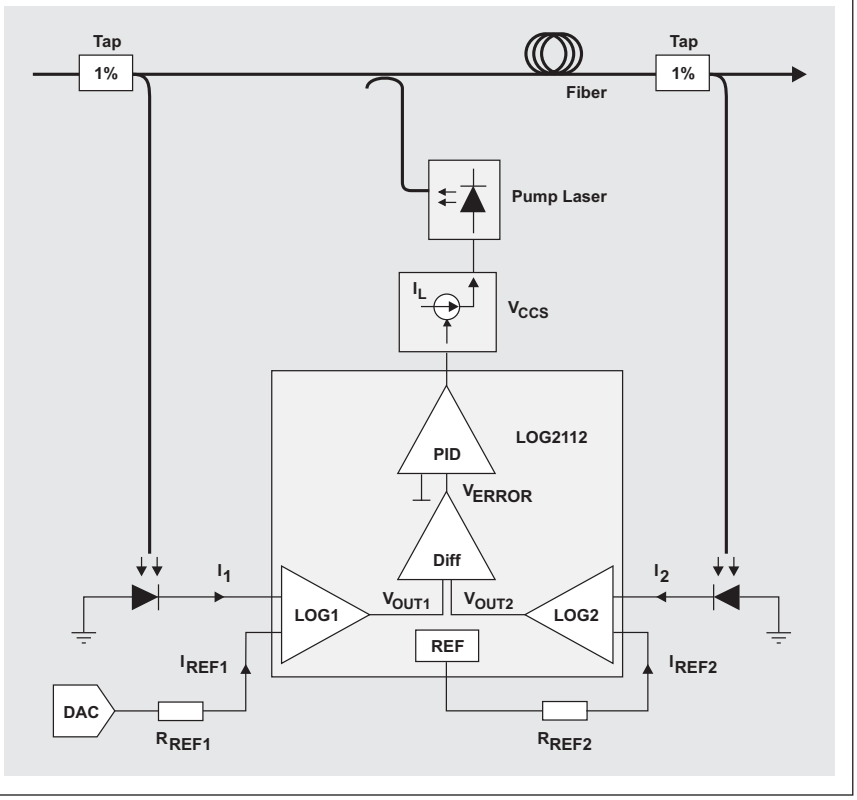


Figure 9. Constant-gain control and gain adjustment of an op amp



The log amp at the amplifier input builds the reference source. Its output voltage is

$$V_{OUT1} = \log \frac{I_1}{I_{REF1}},$$

where I_1 is the input photo current and I_{REF1} is an adjustable reference current. The log amp at the amplifier output provides an output voltage of

$$V_{OUT2} = \log \frac{I_2}{I_{REF2}},$$

where I_2 is the output photo current and I_{REF2} is a fixed reference current.

It is important to observe that $I_2 = I_1 \times G_{OPT}$, where G_{OPT} is the optical gain factor. In steady state, the output voltages of both log amps are equal ($V_1 = V_2$), and

$$\log \frac{I_1}{I_{REF1}} = \log \frac{I_1 \times G_{OPT}}{I_{REF2}}, \text{ or } \frac{I_1}{I_{REF1}} = \frac{I_1 \times G_{OPT}}{I_{REF2}}.$$

Solving for G_{OPT} yields

$$G_{OPT} = \frac{I_{REF2}}{I_{REF1}}.$$

The preceding equation shows that the optical gain of the amplifier is adjusted simply by reducing I_{REF1} by a factor of G_{OPT} smaller than I_{REF2}. In addition to the constant-gain control, this circuit also allows the electronic gain setting of G_{OPT} in the range of 0 to 30 dB.

LOG2112 is well suited for this application. The device contains two log amps to measure the input and output power; an on-chip voltage reference to generate I_{REF2}; and two uncommitted op amps configurable as difference amplifier and PID controller.

Conclusion

TI offers a series of integrated, high-precision log amps with varying input-current ranges and output-scale factors.

Related Web sites

analog.ti.com
www.ti.com/sc/device/LOG112

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