Runtime power control for DSPs using the TPS62000 buck converter

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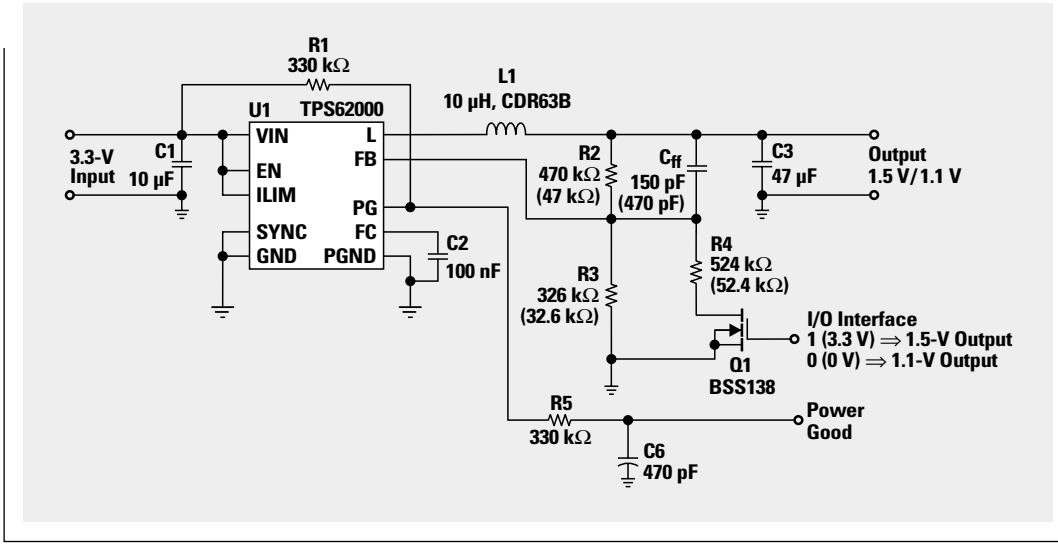
Introduction

This article describes how to reduce core power consumption of a digital signal processor (DSP) or microprocessor using runtime power control (RPC). This technique becomes more and more attractive for portable battery-powered systems where low power consumption is critical for extended operating time.

In many portable applications like Internet audio, MP3 players, or digital still cameras, the full processing power of a DSP is not needed all the time. This presents the opportunity to reduce the processor core power consumption by decreasing the core supply voltage and clock frequency. The technique of adjusting the core voltage to the required core performance is called dynamic voltage scaling (DVS) or RPC.

This article describes a circuit solution for DVS based on the TPS62000 buck converter. During the periods in which maximum DSP performance is not required, the core supply voltage is reduced and the DSP operates at a reduced clock rate. For the next generation of microprocessors and DSPs, the ability to handle this technology will become an important feature. RPC extends battery life in handheld applications like MP3 players, digital cameras, and PDAs. Actual measurements using an MP3 player application resulted in a 23% reduction of DSP core power.

Figure 1. Circuit diagram for dynamic voltage scaling



Core supply considerations

The DSP power supply can be separated into an I/O interface supply and a core supply. The I/O interface is typically powered by the 3.3-V system supply voltage; whereas the core supply requires voltages below 1.5 V. The minimum required core supply voltage depends on the clock rate, which is a function of the DSP performance that the application demands. For the MP3 player application chosen for this example, dynamic voltage scaling was implemented by switching the core supply between the two voltage levels, 1.5 V and 1.1 V. These two values seem practicable for modern DSP applications but need to be determined by the system designer and carefully validated against data sheet limits. The following simplified equation describes the power consumption of a DSP core:

$$P_C \sim (V_C)^2 \times f,$$

where P_C = core power consumption, V_C = core voltage, and f = core clock frequency. It can be seen that power consumption can be reduced by lowering the internal clock frequency and the core supply voltage.

Circuit description

The TPS62000 is a member of the TPS6200X high-efficiency synchronous buck converter family, which is specially designed for portable applications. The TPS62000 provides a wide adjustable output voltage range, going as low as 0.8 V. Efficiency up to 95% and output current up to 600 mA make this device ideally suited for core voltage supply. It comes in a tiny MSOP10 package and enables a wide input voltage range of 2 V to 5.5 V. Due to decreasing core supply voltages in modern DSP systems, using synchronous step-down converters like TPS62000 is far more efficient than using LDO regulators.

The TPS62000 buck converter is powered by a 3.3-V system supply. A general-purpose I/O (GPIO) port on the DSP selects the requested core voltage. Figure 1 illustrates the circuit that was used for the DVS implementation. By varying the feedback resistor network, the core voltage can be adjusted to between 1.1 V and 1.5 V. A MOSFET modifies the resistive voltage divider connected

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between the output of the DC/DC converter and its feedback (FB) pin by switching a parallel resistor in the circuit. In this application, a general-purpose BSS138 MOSFET is used with a V_{GSth} of 1.6 V. The GPIO 3.3-V port drives the MOSFET. The feedback resistor network consists of R2, R3, and R4. C_{ff} is a feed-forward capacitor that is used in the compensation network of the regulator to improve regulation.

Modifying the resistor network by switching R4 parallel to R3 is recommended. The parasitic capacitances of the MOSFET then have the least influence on the regulation behavior of the DC/DC converter. The proposed MOSFET has an $R_{DS(on)}$ below 10 Ω. This value is very small compared to the values of the resistive divider and can therefore be neglected in the calculation of the resistance values of the modified resistive divider.

General requirements for this application are:

- Output voltage 1 (DSP core): 1.5 V
- Output voltage 2 (DSP core): 1.1 V
- Input voltage: 3.3 V
- Output current: 150 mA (10-Ω load)

To keep current and power losses through the adjustment resistor network as low as possible, the resistors are calculated to R2 = 470 kΩ and R3 = 326 kΩ. For R3 and R4 in parallel to equal 201 kΩ, the value of R4 is calculated to 524 kΩ. The calculation of the feedback resistor network is described in Reference 1. With this resistor choice, the quiescent current through the resistor network is less than 2 µA. This is about 4% of the typical 50-µA quiescent current of the converter. To reduce the influence of the MOSFET's gate-drain capacity during switching, a 150-pF capacitor is recommended for C_{ff}. The calculation of the C_{ff} capacitor value is also explained in Reference 1.

Figure 2 shows a complete voltage scaling cycle. I_{OUT} is the output current, powered in a 10-Ω load. V_{SEL} represents the I/O voltage applied to the MOSFET gate. A low level of V_{SEL} scales the output voltage to 1.1 V; a high level to 1.5 V. Figures 3 and 4 show the V_{OUT} variation in more detail.

Influence of the MOSFET on the regulation loop

In Figure 3, a small voltage overshoot on V_{OUT} is generated when V_{SEL} is switched from high- to low-level. The reason for this is the gate-drain capacitance of the MOSFET, which injects the negative edge of the V_{SEL} signal into the feedback resistor network.

If lower values for the feedback resistor network are used, the influence of the gate-drain capacitance can be reduced. Lower resistor values result in higher values for C_{ff}. As an experiment, the resistor values are lowered with a factor of 10 to R2 = 47 kΩ, R3 = 32.6 kΩ, and R4 = 52.4 kΩ. C_{ff} is increased to 470 pF.

Figure 2. Complete voltage scaling cycle

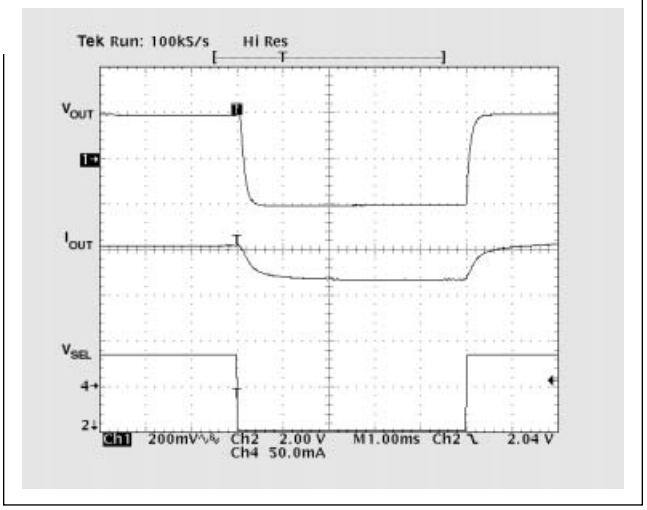


Figure 3. V_{OUT} scaled from 1.5 V to 1.1 V

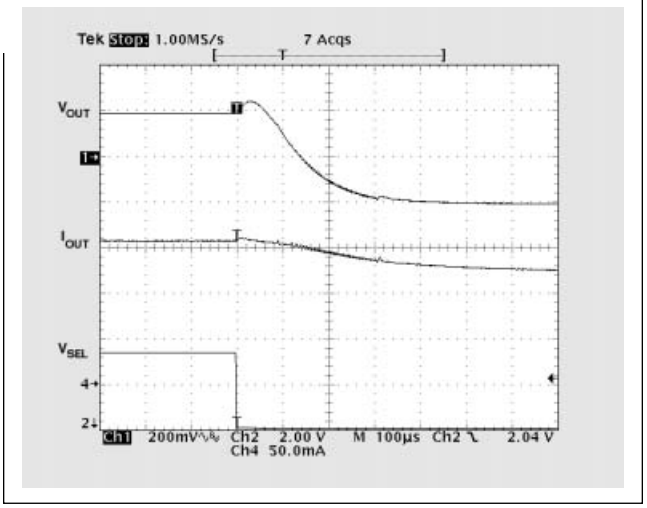
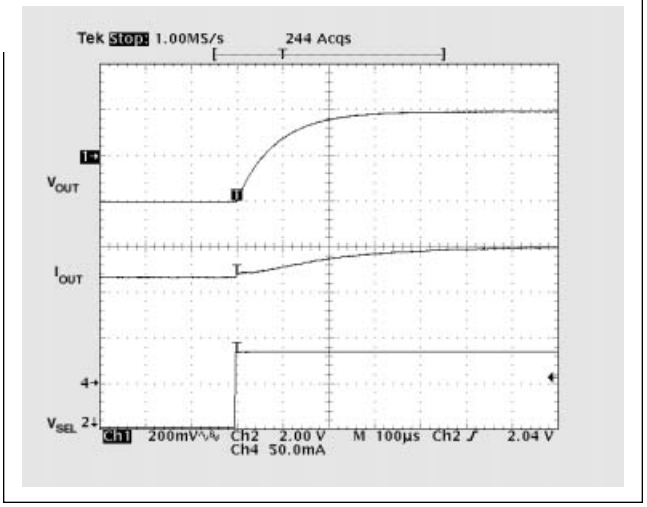


Figure 4. V_{OUT} scaled from 1.1 V to 1.5 V



With this modification, the overshoot (when the converter is switched to regulate to 1.1 V) is decreased to less than 20 mV, as can be observed in Figure 5.

Figure 6 shows the feedback resistor network with MOSFET gate-drain (C_{GD}) capacity. With an increased value of C_{ff}, the influence of gate-drain capacity C_{GD} is reduced. C_{ff} then works as a low-impedance connection to V_{OUT} and minimizes the docked V_{SEL} signal at the FB pin. Furthermore, the influence can be reduced if a MOSFET with lower internal capacitance is used instead of a general-purpose MOSFET.

Timing considerations

The timing behavior of the V_{OUT} signal depends on the values of the output and input capacitors, the coils, and the feedback resistor network. Exact values that are valid for all applications can't be specified here, because the fall time of V_{OUT} depends on the output current as well as on the inductor and output capacitor. During the fall time, the load must absorb the energy stored in the output capacitor until the lower voltage is in regulation.

As shown in Figure 7, the timings are described as follows:

- *Delay time t_0 to t_1:* Range within 50 µs in this application, measured with a 10-Ω load. This represents the settle time of the resistor network on the FB pin.
- *Fall time t_1 to t_2:* This time is mainly defined by the output current. It also depends on the values of the inductor and the output capacitor.
- *Delay time t_3 to t_4:* In this application, about 10 µs.
- *Rise time t_4 to t_5:* 125 µs to 150 µs measured in this application. This also depends on the components and the load current.

Power Good output

The Power Good comparator (see Figure 1) has an open-drain output that becomes active-high if the output voltage exceeds 94.5% of its nominal value. The dynamic variation of the resistor network can affect the Power Good detection circuit, because it compares the FB voltage with an internal reference. Depending on output current, a short /PG spike can occur during rise time from 1.1-V to 1.5-V core level. Using a little RC filter on PG output is recommended to eliminate this short spike and to get a defined PG signal, if used. R1 is the PG pull-up resistor, and R5 and C6 form the RC-filter network, as can be seen in Figure 1.

Core-voltage monitoring

After the core voltage reaches 1.5 V, the DSP can be switched to higher internal clock rates again. To do that, the time t_5, when the DC/DC converter output is in regulation again, must be detected. This can be achieved by either of the following alternatives.

- *A software timer* (activated after the DSP initiates the control signal to increase the supply voltage). Since the rise time of V_{OUT} is application-specific, the designer has to determine it based on measurements.

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Figure 5. Reduced voltage overshoot

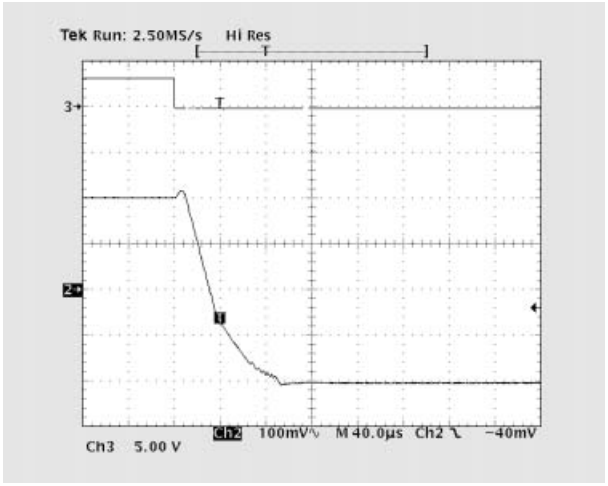


Figure 6. Feedback resistor network with gate-drain capacity

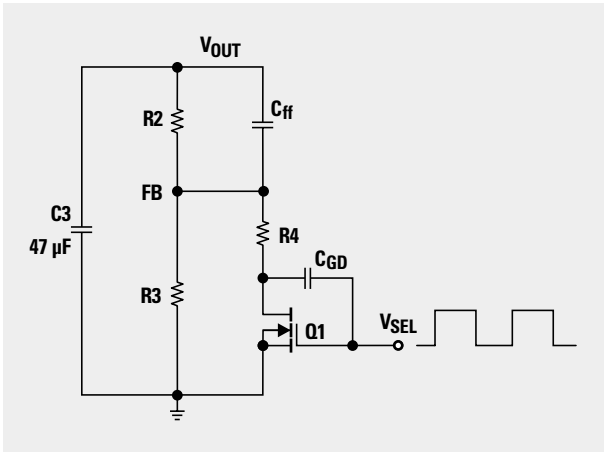
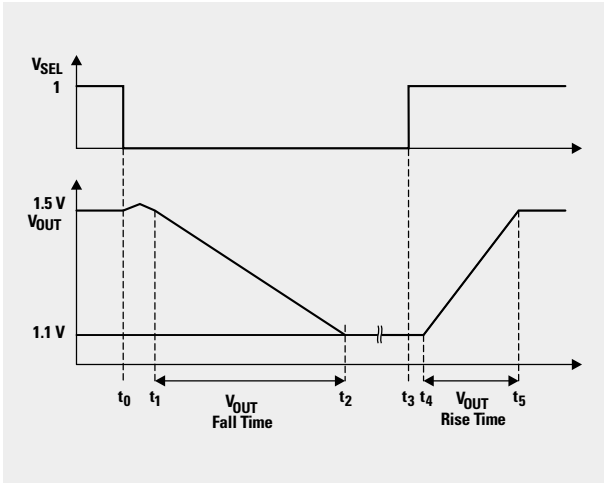


Figure 7. Timing



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- *Voltage monitoring.* Figure 8 shows the relation between V_{OUT} and the signal core-voltage detection (CVD). This CVD signal can be generated by the Power Fail comparator of a supply voltage supervisor (SVS) circuit, like the TPS3705 family with internal 1.25-V reference. This method detects the exact moment when the 1.5-V core voltage fails or matches. As many processors request negative edges for interrupt generation, inverting the CVD signal can be useful. The SVS circuit is supplied by the 3.3-V system supply. The threshold voltage for core-voltage detection can be adjusted by external resistors. The basic block diagram of this circuit is shown in Figure 9.

Conclusion

The solution for dynamic voltage scaling, as described in this article, is a simple approach to reduce the core power consumption of next-generation DSPs and microprocessors. Based on the TPS62000 high-efficiency step-down converter, only a few additional passive components and a general-purpose MOSFET are required. The benefit of reduced core power consumption will compensate the effort in additional components, especially in portable applications where power consumption is critical. Actual measurements using TI's Internet audio player reference design resulted in a 23% reduction of DSP core power consumption and an appropriately extended operating time from one battery set.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "TPS62000, TPS62001, TPS62002, TPS62003, TPS62004, TPS62005, TPS62006, TPS62007 High-Efficiency Step-Down Low Power DC-DC Converter," Data Sheet	.slvs294

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Figure 8. Timing of core-voltage detection

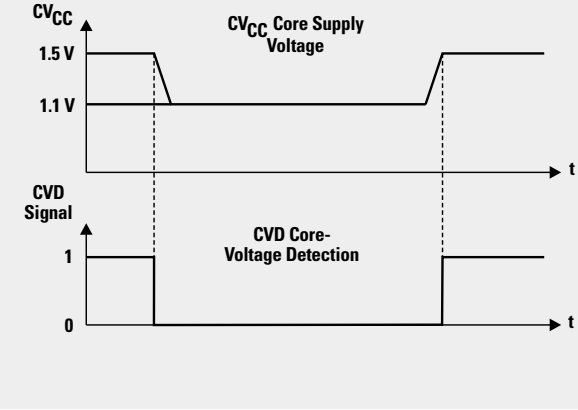
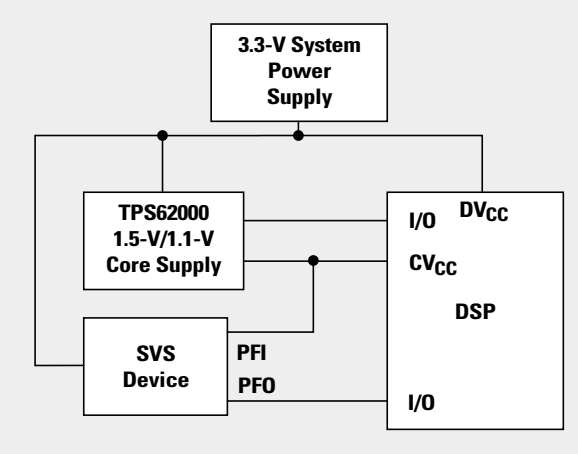


Figure 9. Basic block diagram for voltage monitoring



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