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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Understanding noise in linear regulators

By John C. Teel (Email: jteel@ti.com)
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Types of noise in analog circuits may include thermal, flicker, and shot noise, among others. In an LDO application, noise is sometimes confused with power supply ripple rejection (PSRR). Many times the two are lumped together and loosely called "noise" just because both cause unwanted signals on the output. This is incorrect. PSRR refers to the amount of ripple on the output coming from ripple on the input. Noise, on the other hand, is purely a physical phenomenon that occurs with transistors and resistors (capacitors are noise-free) on a very fundamental level.

Noise in an LDO is indicated in two fashions. One is spectral noise density, a curve that shows noise ($\mu V/\sqrt{Hz}$) versus frequency. The other is integrated output noise, also commonly called output noise voltage (in μV_{rms}); it is simply the spectral noise density integrated over a certain frequency range and can therefore be thought of as the total noise in a specified frequency range. Since the output noise voltage is represented by a single number, it is very useful for comparison purposes.

Typically, noise in an LDO is specified as output-referred noise (noise occurs throughout the LDO but eventually must be referred to the output). The typical approach to finding the output-referred noise of an LDO is first to refer all noise contributors to the input of the LDO differential amplifier. To *refer* means to divide each individual noise contributor by the gain that exists between it and the op amp input (assuming the noise contributor is located downstream on the signal path). The next step is now to refer the total input-referred noise to the output by multiplying by the closed-loop gain of the feedback network. The closed-loop gain of an LDO is simply

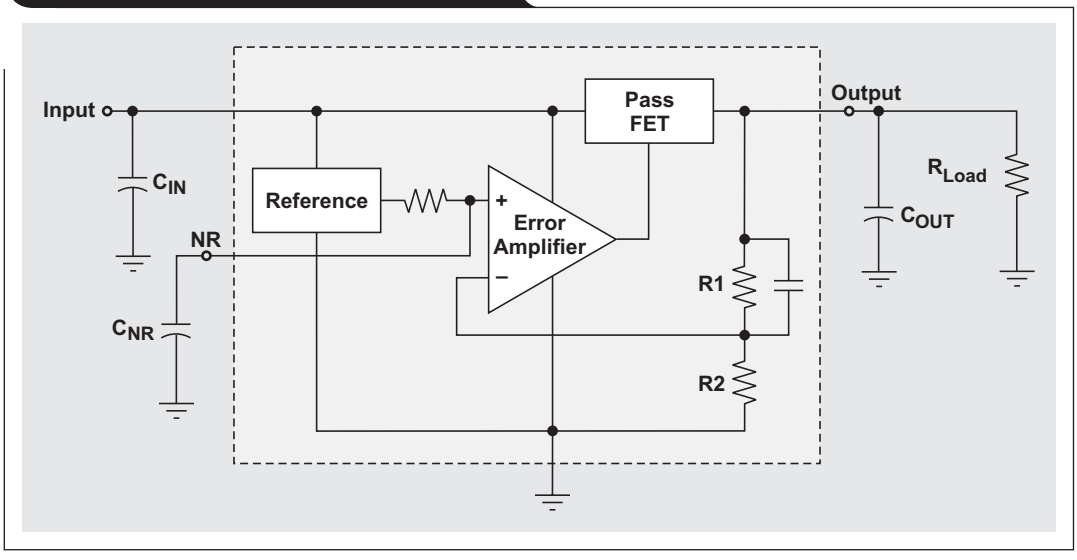
$$A_{CL(DC)} = \frac{V_{OUT}}{V_{BG}},$$

where V_{BG} is the internal bandgap reference. In many cases V_{BG} is about 1.2 V (although some LDOs have sub-bandgap references and thus a V_{BG} of less than 1.2 V). An LDO with an output voltage of 3.0 V will have almost twice the output noise voltage of a 1.5-V LDO; therefore it's very important when comparing noise on various LDOs always to compare those with identical output voltages. When this isn't possible, an approximation can be made by simply taking into account the ratio of the two output voltages. For example, when comparing the noise voltage of a 3.0-V LDO to that of a 1.5-V LDO, either multiply the noise voltage of the 1.5-V LDO by 2 or divide the noise voltage of the 3.0-V LDO by 2.

The simplified block diagram in Figure 1 shows the primary noise sources in an LDO-the bandgap, the resistor divider, and the input stage of the op amp. The effects of some of these noise sources can be reduced if the latter are properly understood.

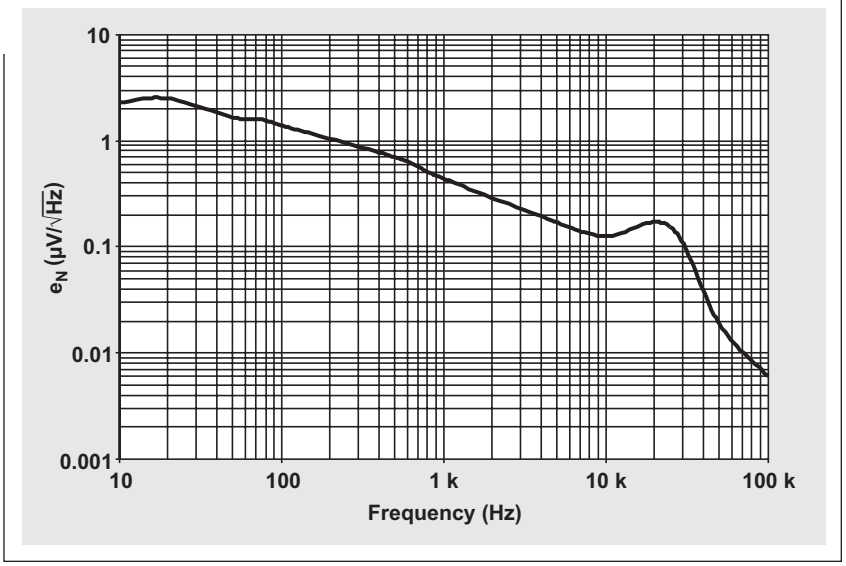
The dominant source of noise in an LDO is usually the bandgap. In most cases this is solved by adding a large low-pass filter (LPF) to the bandgap output so that none of the noise makes it into the gain stage. (This same filter

Figure 1. Simplified LDO block diagram



is also used to improve PSRR.) Typically this LPF is formed with a large internal resistor and an external capacitor. In most cases the cutoff frequency of this filter is set somewhere between 1 and 500 Hz, therefore filtering out nearly all of the noise coming from the bandgap. In many cases the down side of using too large an RC filter is that the time to charge the filtered bandgap increases drastically, which significantly slows down the output startup. This can be solved by using a low-noise, high-PSRR LDO with a fast-charge circuit such as the TPS793/4/5/6xx or one from the TPS799xx family. Even with a fairly large noise reduction capacitor of 0.01 µF, these LDOs are still able to start up in only 50 to 100 µs.

Figure 2. Spectral noise density example



Another source of noise in an LDO is the resistor divider network. This noise is known as thermal noise and is equal to 4kTR (sometimes called 4kTR noise), where k is Boltzmann's constant, T is temperature in Kelvin, and R is the resistance. The resistor divider is tied to the input of the LDO differential amplifier, so this noise is amplified by the closed-loop gain of the LDO. When calculating this noise source, you can simply use the parallel combination of R1 and R2 since the op amp input sees them as being virtually in parallel. Therefore, to reduce this noise source, the most important thing to remember is that smaller feedback resistors create less thermal noise. Of course, the disadvantage of using smaller resistors is that they burn more current through the feedback divider; but if noise is of prime importance, then this sacrifice must be made.

The other source of noise is the internal LDO differential amplifier, which is usually designed in such a way that the input stage has a large amount of gain—more specifically, transconductance (g_m). This is done so that any noise coming from devices in the signal path located after the input stage have their noise attenuated by the gain of the input stage when they are referred back to the input. There is nothing outside of the internal circuitry that can be done to reduce this noise source.

Many people are surprised that the huge power pass FET, which usually takes up at least half of the total die area in an LDO, isn't a primary noise contributor. The reason for this is the lack of gain. All of the primary noise sources (bandgap, resistor divider, and op amp input stage) are connected to the input of the differential amplifier and thus are not attenuated by any internal gain. Remember that the procedure for finding output noise is first to refer each noise contributor to the op amp input; so to find the noise from the pass FET you would first divide its noise contribution by the open-loop gain that exists between it and the op amp input. This gain is typically quite large; therefore, the noise contribution from the pass FET is usually negligible.

Also somewhat surprising is that neither the output capacitor, the load current, nor even the input voltage has any direct effect on the output noise, at least to a first order. However, load current and output capacitance do have an indirect second-order effect. As mentioned previously, output noise is calculated by multiplying the input-referred noise by the closed-loop gain. The closed-loop gain isn't constant at V_{OUT}/V_{BG} over the entire frequency range, and of course it eventually rolls off at high frequencies. A fundamental rule of feedback analysis is that low phase margin will cause peaking in the closed-loop gain near the unity-gain frequency. Since the closed-loop gain amplifies the noise, this peaking increases the noise in that frequency range even more, thus increasing the total output noise. This effect can often be seen in spectral noise density plots like the one in Figure 2.

High load currents and low output capacitance contribute to output noise because they both make the LDO less stable, which reduces the phase margin. This phase margin reduction increases the closed-loop gain peaking, which in turn increases the output noise. Another significant effect is that many times a higher equivalent series resistance (ESR) capacitor will actually reduce noise. This is because a larger ESR creates a lower-frequency zero, which many times may improve the LDO stability. Finally, note that the peaking effect explains why, as previously mentioned, the output noise voltage of a 3.0-V regulator usually isn't quite twice as much as that of a 1.5-V regulator. A 3.0-V regulator tends to be a bit more stable than a 1.5-V regulator due to its lower feedback factor. This improved stability increases the phase margin, reducing the closed-loop peaking and thus the output noise voltage.

One final trick sometimes used to reduce noise is to add a capacitor across the top resistor in the resistor feedback

divider. This works because at high frequencies the capacitor begins to reduce the closed-loop gain and thus the noise, so that the system begins to look like a unity-gain feedback configuration providing no noise gain. The trade-off is that this could potentially slow down start-up time significantly, since the capacitor would have to be charged by the current in the resistor divider. The TPS799xx implements this technique via an internal capacitor and also includes a fast-charge circuit.

In summary, there are many ways to reduce noise in an LDO application. The most important is to start with a low-noise, high-PSRR LDO optimized for low-noise applications such as one from the TPS793/4/5/6xx family or the low-I_q TPS799xx family. The second way is to use as large a noise-reduction capacitor as is feasible for startup while keeping in mind that there's a point where increasing this capacitance will offer no further improvement. Finally, use small resistances for the resistor divider network (if the LDO is an adjustable version) and a small capacitor across the top resistor, if possible. Some less obvious improvements are to optimize the output capacitor along with the load current for the highest phase margin to reduce closed-loop peaking. Many times, stability can be optimized by using the stability plots provided in some LDO data sheets.

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Understanding power supply ripple rejection in linear regulators

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Power supply ripple rejection ratio (PSRR) is a measure of how well a circuit rejects ripple coming from the input power supply at various frequencies and is very critical in many RF and wireless applications. In the case of an LDO, it is a measure of the output ripple compared to the input ripple over a wide frequency range (10 Hz to 10 MHz is common) and is expressed in decibels (dB). The basic equation for PSRR is

$$\text{PSRR} = 20\log\frac{\text{Ripple}_{\text{Input}}}{\text{Ripple}_{\text{Output}}}.$$

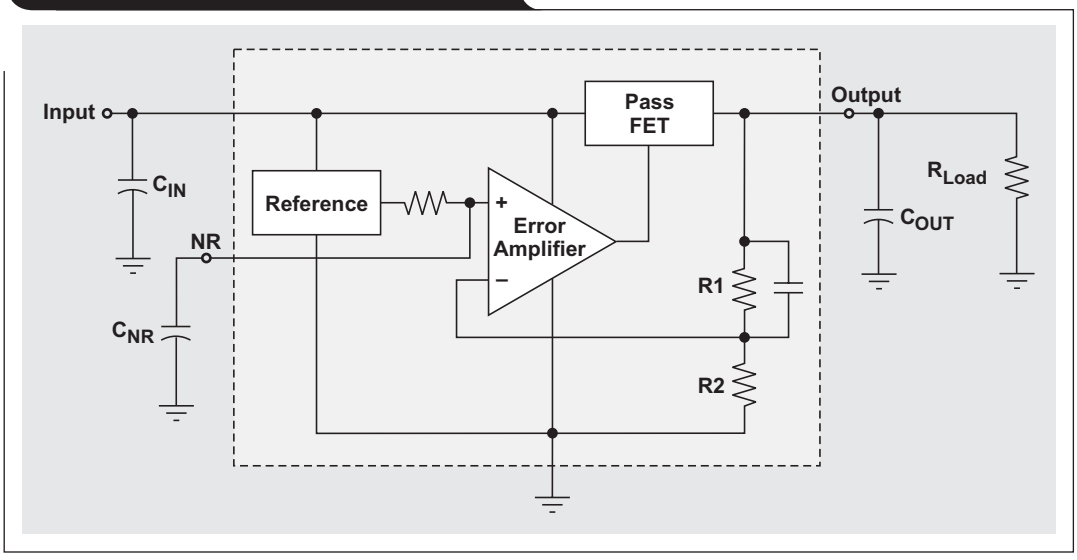
More specifically, PSRR for an LDO can be written as

$$\text{PSRR} = 20\log\frac{A_V}{A_{VO}},$$

where A_V is the open-loop gain of the regulator feedback loop, and A_{VO} is the gain from V_{IN} to V_{OUT} with the regulator feedback loop open. From this equation it can be seen that to increase the PSRR it is beneficial to increase the open-loop gain and decrease the gain from V_{IN} to V_{OUT}. Typically, A_{VO} is significantly less than 0 dB, with –10 to –15 dB being typical; this is entirely driven by internal and external parasitics from input to output and at the gate of the pass FET. Figure 1 shows a simplified regulator block diagram with a PMOS pass device.

Another parameter that is closely related to PSRR is line transient response. PSRR is specified at specific frequencies, whereas a line transient essentially contains all frequencies due to the Fourier components of a step function. However, the primary difference is that PSRR is based on small signals, whereas line transients are large signals and thus theoretically much more complicated in nature. Since improving PSRR typically improves line transient response and vice versa, all of the effects on PSRR discussed in this article will usually have a similar effect on the line transient response.

Figure 1. Simplified LDO block diagram



A curve showing PSRR over a wide frequency range is shown in Figure 2.

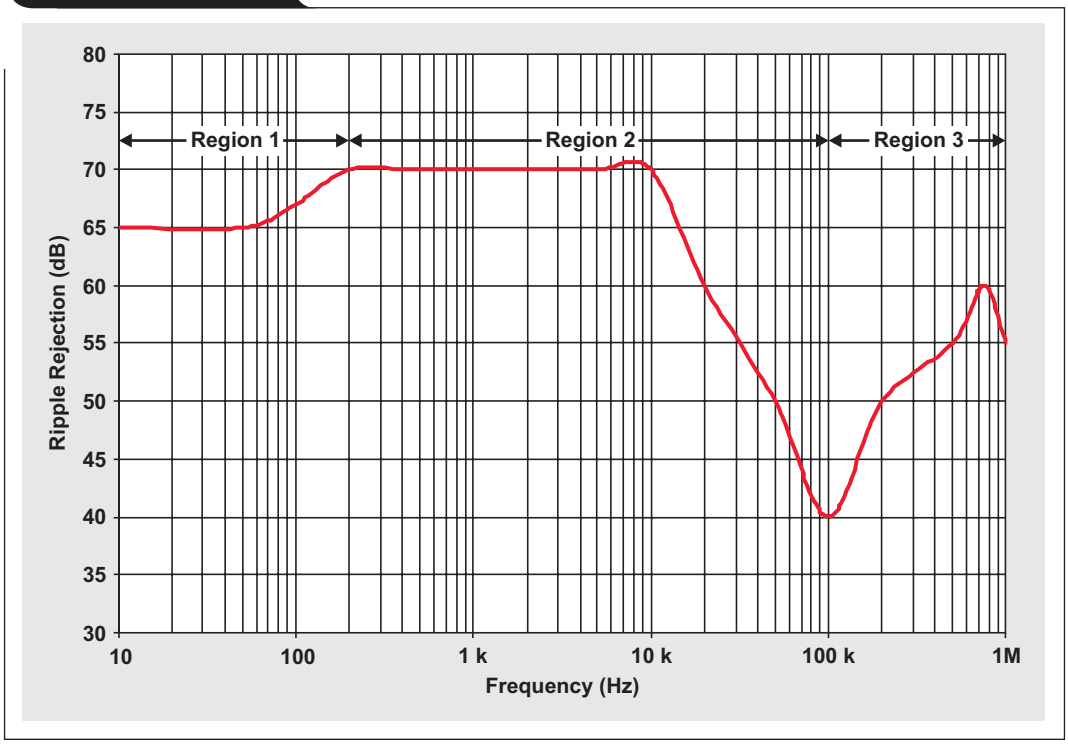
As mentioned previously, the open-loop gain of the LDO feedback circuit is the dominant factor in PSRR (at least in a limited frequency range); therefore, LDOs requiring good PSRR typically have high gain with a high unity-gain frequency (large gain-bandwidth product). However, this makes the loop more difficult to stabilize, which limits how much the gain-bandwidth product can be increased to improve PSRR. It is important to have a high unity-gain frequency so that the amplifier does not lose open-loop gain at relatively low frequencies, causing PSRR to roll off also.

The curve in Figure 2 shows that PSRR for an LDO can be broken down into three basic frequency regions. Region 1 is from dc to the roll-off frequency of the bandgap filter and is dominated by both open-loop gain and bandgap PSRR. Region 2 extends from the bandgap filter roll-off frequency up to the unity-gain frequency where PSRR is dominated mainly by the open-loop gain of the regulator. Region 3 is above the unity-gain frequency, where the feedback loop has very little effect, so the output capacitor dominates along with any parasitics from V_{IN} to V_{OUT}. The gate driver's ability to drive the pass-FET gate at high frequencies also has an effect in Region 3. A larger output capacitor with less equivalent series resistance (ESR) will typically improve PSRR in this region, but it can also actually decrease the PSRR at some frequencies. This is because increasing the output capacitor lowers the unity-gain frequency, causing the open-loop gain to roll off earlier and thus lowering PSRR. Nevertheless, the minimum PSRR that occurs at the unity-gain frequency will typically be improved.

Anything affecting the gain of the feedback loop also affects PSRR in Region 2. One example is load current. As load current increases, the open-loop output impedance of the LDO decreases (since a MOSFET's output impedance is inversely proportional to the drain current), thus lowering the gain. Increasing the load current also pushes the output pole to higher frequencies, which increases the feedback loop bandwidth.The net effect of increasing the load is therefore reduced PSRR at lower frequencies (because of the reduced gain) along with increased PSRR at higher frequencies.

The differential dc voltage between input and output is another example of how a change in the feedback loop gain also affects PSRR. As V_{IN}–V_{OUT} is lowered to less than about 1 V, the internal pass FET (which provides gain in a PMOS design) starts to be pushed out of the active (saturation) region of operation and into the triode/linear region, which causes the feedback loop to lose gain. The dividing line between the active region and the triode region is proportional to the square root of the drain (load) current. So as the load current is increased, the voltage across the device (V_{IN}–V_{OUT}) necessary to keep it in the active region increases as a function of the square root of the load current. For example, having V_{IN}–V_{OUT} at only 0.5 V may have no negative effect on PSRR at light load currents because the pass FET device doesn't need much headroom to stay in the active region and to preserve gain. At heavier loads,

Figure 2. PSRR curve



however, 0.5 V may no longer be sufficient and the pass FET device may enter the triode region, causing the circuit to lose gain, thus reducing PSRR. When PSRR is compared among various LDOs, it's important always to compare LDOs with identical $V_{IN}–V_{OUT}$ and I_{Load} conditions. It's also important to compare LDOs with identical output voltages, since PSRR is usually better at lower output voltages.

One of the dominant internal sources of PSRR in an LDO is the bandgap reference. Any ripple that makes its way onto the reference will be amplified and sent to the output, so it's important to have a bandgap reference with high PSRR. Typically, the solution is simply to filter the bandgap with a low-pass filter (LPF). This LPF is almost always accomplished with a large internal resistor and an external capacitor. The effect of the LPF can be seen in Region 1 of Figure 2, where the PSRR is somewhat reduced because the LPF passes bandgap ripple in this frequency range.

As has been shown, there are many ways to improve the PSRR in an LDO application. The most important is to start with a low-noise, high-PSRR LDO designed for high-PSRR applications such as one from the TPS793/4/5/6xx family or the low-I_q TPS799xx family. The next most important way is to choose a low-ESR ceramic output capacitor and to determine the capacitance value based on the frequencies at which PSRR is most important. Finally, board layout must be carefully done to reduce the feedthrough from input to output via board parasitics.

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Maximizing signal integrity with M-LVDS backplanes

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As the demand for higher clock and data transfer rates across backplane systems continues to grow, fundamental elements of high-speed printed circuit board design become essential. This article identifies issues associated with high-speed multipoint backplane design and provides recommendations that include the use of multipoint low-voltage differential signaling (M-LVDS) (TIA/EIA-899) technology. M-LVDS provides multipoint communication with up to 32 M-LVDS circuits connected to the same media. Test results demonstrating the use of M-LVDS across a custom-designed backplane will be presented along with development guidelines for aiding the design of a high-performance system.

Backplane signaling technologies

The good news is that there are many choices available for transferring information within a backplane environment, but this can also make it difficult to decide which technology should be used in a particular application. The key to selecting the right signaling technology for a backplane is having a good understanding of the system requirements such as signaling rate, power, topology, EMI, transmission distance, and loading conditions.

Some of the single-ended signaling technologies available include transistor-transistor logic (TTL), low-voltage TTL (LVTTL), backplane transceiver logic (BTL), gunning transceiver logic (GTL), and GTL plus (GTLP) (see Table 1). Single-ended transmission occurs when information is sent over a single line referenced to ground, helping to keep the costs lower for cabling or connectors. However, single-ended signal transmission is also more susceptible to noise, crosstalk, and ground offsets, all of which can result in receiving false data.

TTL and LVTTL standard logic devices abound, providing not only many choices for signal transmission across the backplane but also the cost advantage of single-ended transmission. However, TTL standard logic devices have large voltage swings that typically translate into EMI. Maintaining these large voltage swings becomes a problem in heavily loaded systems, and TTL is susceptible to signal integrity issues associated with single-ended data transmission (noise, crosstalk, and ground offsets).

BTL also uses single-ended transmission but lowers the voltage swing to 1.1 V, which can lead to higher transmission rates and reduced EMI radiation relative to TTL. This reduced voltage swing is achieved by an open-collector output with the bus terminated through a resistor to 2.1 V. When the driver is activated, the bus is pulled down to the saturation point of the driver plus the voltage drop across a series diode, resulting in a 1-V low. The value of the termination resistor should match the characteristic impedance of the signal path.

GTL uses an open drain but, unlike BTL, does not use a series diode. This results in an active-low condition of only 0.4 V. The bus termination voltage is reduced to 1.2 V, providing a total voltage swing of 0.8 V. This lower voltage swing can further reduce EMI and provide for higher transmission rates relative to BTL. However, the sink current is reduced to 40 mA, which is acceptable for onboard chip-to-chip applications but limits the capabilities for driving a heavily loaded backplane. GTL is primarily recommended for point-to-point technologies. GTLP is much better suited for multipoint (backplane) environments than GTL.

GTLP is similar to GTL, with slight variations in output voltage and termination levels (see Table 1) that were introduced to improve the noise margin relative to ground. More significantly, GTLP offers two drive options (50 mA or 100 mA) that can accommodate a more heavily loaded backplane. GTLP also features output edge control and internal precharge circuitry enabling live insertion, further improving performance within the backplane environment.

Table 1. Single-ended signaling technologies

PARAMETER	TTL (LVTTL)	BTL	GTL	GTLP
V_{IN}, high (V)	2.0	1.62	0.85	1.05
V_{IN}, low (V)	0.8	1.47	0.75	0.95
V_t, V_{REF} (V)	1.4	1.55	0.8	1.0
V_{OUT}, high (V)	2.4	2.1	1.2	1.5
V_{OUT}, low (V)	0.4	1	0.4	0.55
Standard driver load (Ω)	—	11	11	11
Drive sink current (mA)	—	100	40	50 or 100
Standard	JESD8-1	IEEE 1194.1	JESD8-3	—

When information is transmitted within a system, it is possible for the ground reference on the transmission end to be offset relative to the ground reference on the receiving end. For single-ended transmission, the signal is referenced to ground; so this ground offset could result in receiving the wrong information. Also, noise within the backplane environment can couple onto the signal path, which again can lead to receiving corrupt information.

Differential signaling provides several benefits over single-ended transmission. For instance, the issue of ground offset within the application is diminished since the signals are referenced to each other rather than to ground. Further, noise within a backplane environment can be alleviated if careful consideration is given to the board layout. If the signal path of the differential pair is routed closely together, noise coupled onto one signal will likely couple onto the other signal of the differential pair. Since these signal pairs are referenced to each other, the noise is effectively canceled out. It is important to note that the magnitude of the resulting offset voltage cannot exceed the input signal range of the receiver. If it does, the information will be corrupt, even with differential signaling.

Of course, with differential signaling, two signal paths per channel will increase the number of cables or connector pins in the system. This must be weighed against the benefits associated with differential signaling and the needs of the applications. Some of the differential signaling technologies available include RS-485, positive emitter-coupled logic (PECL), low-voltage PECL (LVPECL), low-voltage differential signaling (LVDS), BusLVDS, and multipoint LVDS (M-LVDS) (see Table 2).

RS-485 employs the advantages associated with differential signaling and is ideally suited for transmitting data over long distances (up to 1200 m) or noisy environments. Multiple drivers and receivers can share the same transmission pair (see Figure 1), which is accomplished by properly terminating each end of the signal path. RS-485 is widely accepted in industrial applications, providing an economic and robust solution.

PECL and LVPECL provide reduced voltage swings and faster transition times than RS-485, making them capable of much higher speeds. PECL transmission may require a separate supply terminating the load resistor to $V_{CC} - 2$ V.

LVDS, with reduced voltage swings and faster transition times, is also capable of much higher speeds than RS-485. LVDS has an added benefit of using less power than PECL and does not require a separate supply for terminating the load resistor at the end of the transmission line. However, LVDS is not intended to support multipoint configurations.

BusLVDS has characteristics similar to those of LVDS, except that it is intended to support multipoint configurations. Since the multipoint configuration requires termination at both ends of the transmission path, the equivalent resistance is half that of a point-to-point configuration.

Figure 1. Multipoint configuration

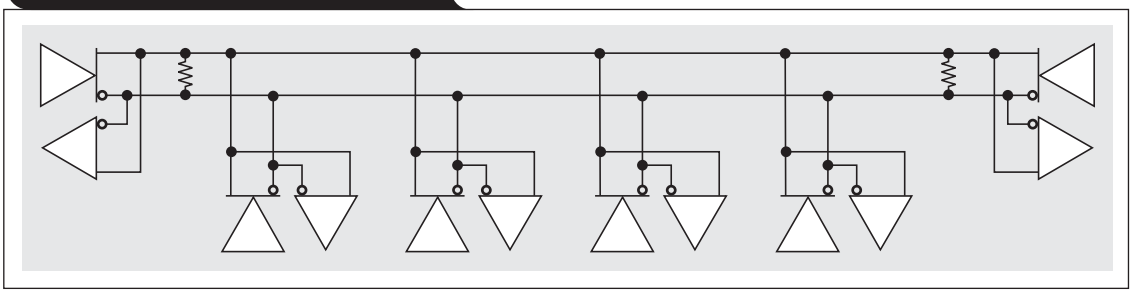


Table 2. Differential signaling technologies

PARAMETER	RS-485	PECL (LVPECL)	LVDS	BusLVDS	M-LVDS
V_{IN}, high	$V_{DIFF} > 200$ mV	$V_{DIFF} > 100$ mV	$V_{DIFF} > 100$ mV	$V_{DIFF} > 100$ mV	$V_{DIFF} > 50$ mV*
V_{IN}, low	$V_{DIFF} < -200$ mV	$V_{DIFF} < -100$ mV	$V_{DIFF} < -100$ mV	$V_{DIFF} < -100$ mV	$V_{DIFF} < -50$ mV*
V_{IN} range (V)	–7 to 12	Varies	0 to 2.4	0 to 2.4	–1.4 to 3.8
V_{OUT}, high**	1.5 V < V_{DIFF}	800 mV	350 mV	300 mV	550 mV
V_{OUT}, low**	–1.5 V > V_{DIFF}	–800 mV	–350 mV	–300 mV	–550 mV
Common-mode output	–1 V < V_{OS} < 3 V	3.6 V (1.95 V)	1.125 V < V_{OS} < 1.375 V	1.1 V < V_{OS} < 1.5 V	0.3 V < V_{OS} < 2.1 V
Standard driver load (Ω)	60	50†	100	27	50
Drive current (mA)	> 25	16	3.5	11	11
Standard	TIA/EIA-485-A	—	TIA/EIA-644-A	—	TIA/EIA-899

* Type 1 receiver threshold is –50 mV < V_{ID} < 50 mV. Type 2 receiver threshold is 50 mV < V_{ID} < 150 mV.
** These are nominal differential output voltage levels relative to the common-mode voltage and may vary with the vendor.
† Each line is terminated with 50 Ω or a Thevenin equivalent.

BusLVDS addresses this issue by increasing the drive current so that, even though the equivalent resistance is cut in half, the desired differential signal level is still maintained.

M-LVDS is a technology designed specifically for heavily loaded backplanes to transfer clock or data signals. The PCI Industrial Computer Manufacturers Group (PICMG®) 3.0 AdvancedTCA™ specification identifies M-LVDS for clock signaling sources across the backplane. M-LVDS provides the following features and benefits (refer to TIA/EIA-899):

- Lower voltage swings relative to RS-485, which can translate into reduced EMI
- Controlled transition times (>1 ns) that help to hide stubs and also reduce EMI
- Receivers that can typically withstand up to ±2 V of ground offset and have common-mode noise immunity
- Support for multipoint configuration
- No need for a separate supply voltage for termination

The standards and corresponding signaling technologies are designed to accommodate certain speeds, transmission lengths, and loading conditions. However, actual performance is highly dependent on how well the overall system is designed. Board layout, effective impedance, proper termination, and stub effects can all degrade signal integrity. Careful system-level design is necessary to optimize performance of the chosen signaling technology. These considerations will be discussed next.

M-LVDS backplane design considerations

According to TIA/EIA-899, M-LVDS is intended for use in point-to-point applications, multidrop clock or data distribution applications, and multipoint data bus applications with multiple drivers sharing the same bus. The receiver input thresholds that are tighter than standard LVDS and the controlled edge rates are added qualities of M-LVDS that can contribute to the success of a high-performance system design.

A backplane test system was constructed with 8-, 19-, and 30-slot bus lengths to demonstrate the capabilities of M-LVDS in several backplane loading scenarios. The guidelines presented here describe high-performance system design practices for success with using M-LVDS in a backplane environment.

The backplane design was a collaborative effort between Texas Instruments (TI) and North East Systems Associates (NESA). The system is based on the CompactPCI® 6U standard with an 0.8″ slot pitch, standard 6U cards, and a 21-slot backplane (2 slots are reserved for power and 19 are used for test cards) that fits into a standard chassis for a 19″ rack. NESA built several multipoint backplane models for the purpose of simulating 8-, 19-, and 30-slot buses. Different edge rates, card and connector stub lengths, backplane differential impedance, termination resistance, and number of slots loaded for each bus length were also variables included in the simulations. IBIS and H-SPICE models of TI M-LVDS devices were provided to NESA and incorporated into the modeling and simulation stage of the backplane system to ensure the accuracy of the final system.

The physical system was constructed based on the simulation results NESA provided. Measurements of active M-LVDS devices operating on the multidrop buses were performed for verification of those simulation results. NESA also simulated and measured the passive backplane traces to ensure that the impedance and other signal integrity parameters specified in the backplane design rules were met. The result of this effort was a controlled impedance design consisting of 10 FR-4 layers, including 4 controlled impedance layers, 2 power layers, and continuous ground layers. Each slot on the backplane uses differentially fed, standard 2-mm HM connectors. This optimized M-LVDS backplane system operates at a data rate of >200 Mbps and a clock rate of >100 MHz across the 8-, 19-, and 30-slot designed bus systems.

The differential M-LVDS bus paths on the backplane were designed to meet a 130-Ω differential impedance, as this was the recommended backplane impedance suggested by the simulation results. A 100-Ω differential impedance is normally used in standard differential bus and backplane design, but the higher impedance helps to alleviate the effect of low effective path impedance created from the close slot pitch and large card load. In simulation, the raw backplane impedance and connector stub lengths were varied to aid in optimizing the former. As connector stub lengths increase, so does the overall capacitance of the loaded backplane bus, lowering the system differential impedance. Keeping connector stub lengths to a minimum will maximize the loaded impedance of the system bus. Results of the time domain reflectometry (TDR) and time domain transmission (TDT) simulations performed by NESA are shown in Table 3 and Table 4, respectively. The PICMG 3.0 AdvancedTCA base specification also recommends using a 130-Ω differential trace impedance to help increase the effective impedance of the clock bus in a heavily loaded backplane.

Table 3. Simulated TDR results from fully loaded 30-slot backplane*

RAW BACKPLANE IMPEDANCE (Ω)	MINIMUM IMPEDANCE LOADED (Ω)	MAXIMUM IMPEDANCE LOADED (Ω)	APPROXIMATE AVERAGE IMPEDANCE LOADED (Ω)
100	45.1	50.2	46
130	52.7	58.8	54
150	57.3	63.9	58

*1″ stubs; TDR rise time = 1 ns.

Table 4. Simulated TDT results from fully loaded 30-slot backplane

RAW BACKPLANE IMPEDANCE (Ω)	RISE TIME INPUT (ns)	RISE TIME OUTPUT (ns)	PROPAGATION DELAY (ns)	PER UNIT DELAY (ps/in)
100	1.07	3.07	9.63	388
130	1.07	2.98	10.6	427
150	1.07	3.01	11.2	452

With a raw impedance of 130 Ω, the effective differential impedance of the fully loaded 30-slot backplane is raised to 54 Ω from the 46 Ω provided by a standard 100-Ω raw impedance. This reduces the load on the device driving the bus and increases the differential voltage of the bus. The drawback of the 130-Ω differential impedance is that it increases the delay from 388 ps/in to 427 ps/in. Based on the results in Table 3, using a 150-Ω differential impedance would further increase the effective impedance of the backplane. However, a 150-Ω differential impedance is not easily manufactured, which increases the difficulty of providing a reliable and repeatable printed circuit board.

A trade-off between slot pitch and daughtercard stub length had to be accounted for during the backplane design. As pitch between slots is decreased, the "per unit" distributed loading on the backplane increases and the effective backplane impedance is reduced. The plug-in card stubs can significantly lower the effective impedance due to their capacitive effect on the backplane traces. As the card stub lengths increase, their capacitance increases and the effective impedance of the backplane is reduced, signal rise times are slowed, and propagation delay through the backplane is increased. If slot pitch is increased, the card stubs can be longer for a particular effective backplane impedance and vice versa. Table 5 and Table 6 show simulation results of TDR and TDT, respectively, on a 130-Ω raw impedance differential trace with 0.8″ slot pitch and different daughtercard stub lengths. Based on the correlated simulation and empirical results, a 1″ or shorter stub length is recommended to prevent the effective backplane impedance from falling below 54 Ω.

Except for delay differences, the 8-, 19-, and 30-slot backplane buses look very similar in passive testing. This is because they all share the same parameters, including 0.8″ slot spacing, identical connectors, and identical card stub lengths. The impedance and transmission profiles are similar to the 30-slot case presented.

Passive and active simulations along with empirical measurements were completed for the various backplane cases with 8-, 19-, and 30-slot buses. As mentioned earlier, the distributed load is similar for all the backplane buses, but actual driver and receiver waveforms can look quite different due to the distance to the terminations and the slot driving the bus. The resistor value used to terminate either end of the multipoint bus was chosen as a good compromise between the heavily and lightly loaded backplane configurations. Through analysis of the passive simulations and empirical results, 80 Ω was chosen to terminate the bus at either end; and all active simulation and empirical results were gathered with the 80-Ω terminations. Ringing, overshoot, and undershoot can be improved by using termination resistors closer to the effective bus impedance for the loading condition being tested.

Table 5. Simulated TDR results from fully loaded 30-slot backplane*

STUB LENGTH (in)	MINIMUM IMPEDANCE LOADED (Ω)	MAXIMUM IMPEDANCE LOADED (Ω)	APPROXIMATE AVERAGE IMPEDANCE LOADED (Ω)
0.5	57.5	62	58
1.0	52.8	58.8	54
1.5	45.9	56.6	50
2.0	40.3	55	48
2.5	35.9	53.6	45
3.0	32.3	52.3	43

*Raw impedance = 130 Ω; TDR rise time = 1 ns.

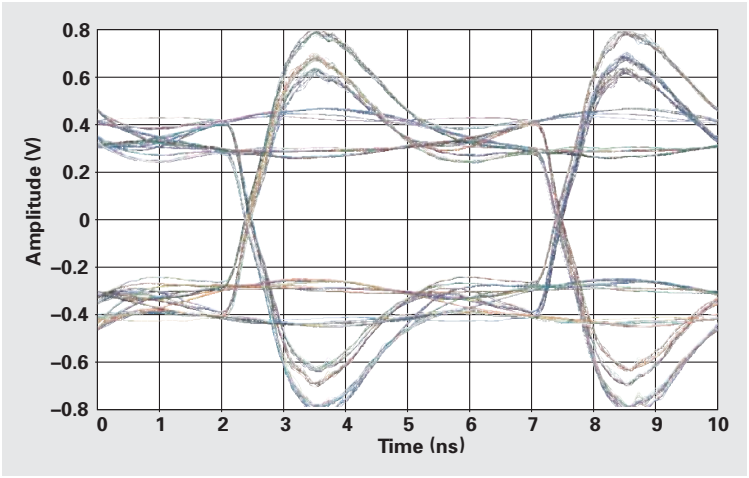
Table 6. Simulated TDT results from fully loaded 30-slot backplane

STUB LENGTH (in)	RISE TIME INPUT (ns)	RISE TIME OUTPUT (ns)	PROPAGATION DELAY (ns)	PER UNIT DELAY (ps/in)
0.5	1.07	2.60	9.68	390
1.0	1.07	2.98	10.6	427
1.5	1.07	3.40	11.5	464
2.0	1.07	3.84	12.3	496
2.5	1.07	4.28	13.1	528
3.0	1.07	4.78	13.8	556

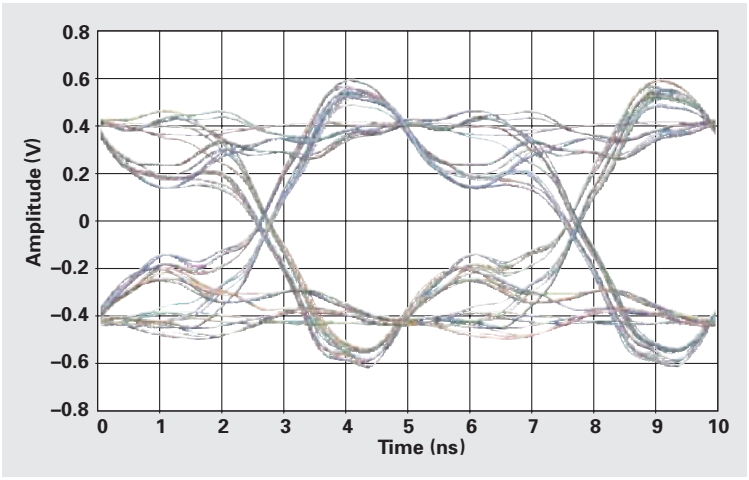
Figure 2 shows simulated 200-Mbps eye patterns at the driver output pins of slot 1 and the receiver inputs of slots 10 and 19 when slot 1 is driving a fully loaded 19-slot backplane bus. The differential voltage drops at slot 10 because it is in the middle of the bus, far away from the termination resistors, but it is still at acceptable levels. Slot 19 shows an improvement in differential voltage because the termination resistor is nearby.

Figure 2. Simulated 200-Mbps eye patterns when slot 1 drives 19-load bus

(a) At slot 1 driver output



(b) At slot 10 receiver input



(c) At slot 19 receiver input

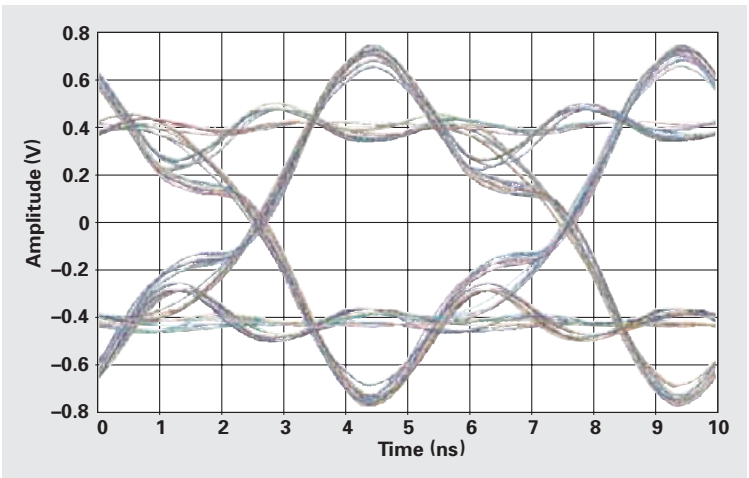
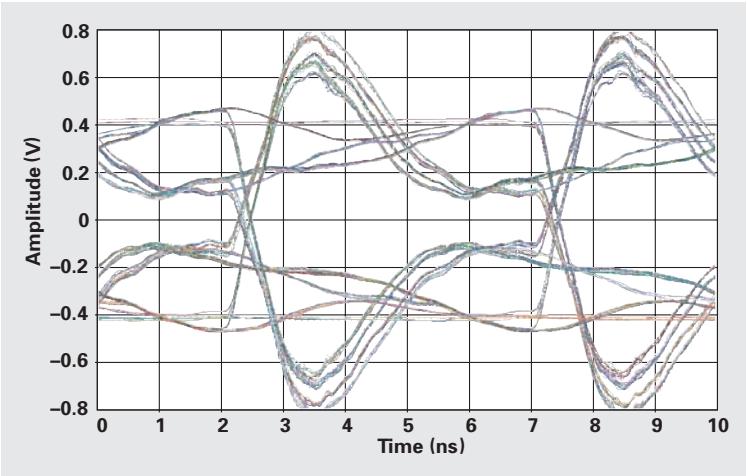


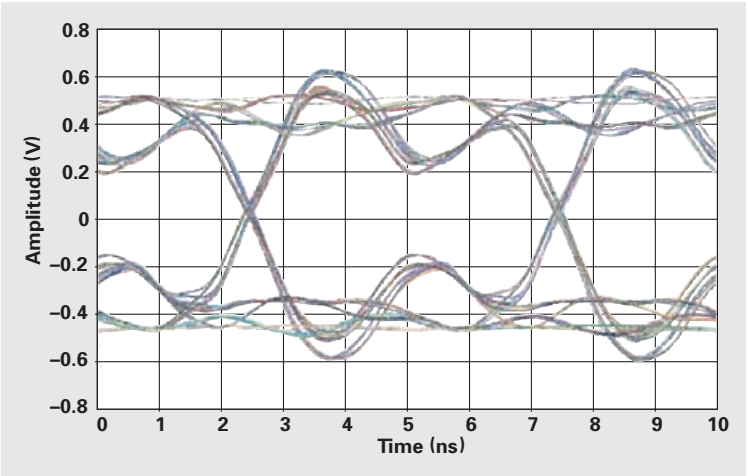
Figure 3 shows simulated 200-Mbps eye patterns at the driver output pins of slot 10 and the receiver inputs of slots 15 and 1 when slot 10 is driving a fully loaded 19-slot backplane bus. The effects of driving into the middle of a heavily loaded bus are evident in the jitter displayed in Figure 3a. However, by the time the signals reach slots 15 and 1, the initial amount of jitter at the driver output pins is masked by the increased rise and fall times. This effect is due to the capacitance encountered at each connector along the backplane by the signals from the driver at slot 10.

Figure 3. Simulated 200-Mbps eye patterns when slot 10 drives 19-load bus

(a) At slot 10 driver output



(b) At slot 15 receiver input



(c) At slot 1 receiver input

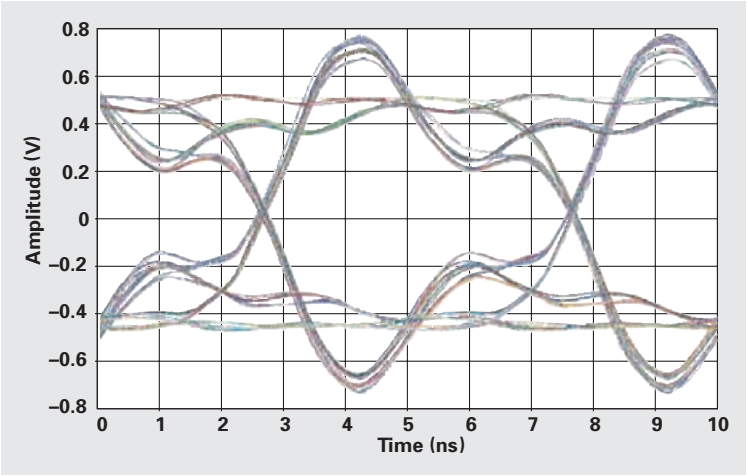
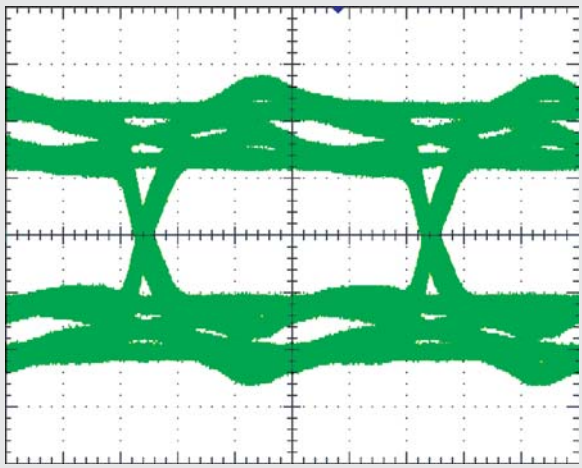
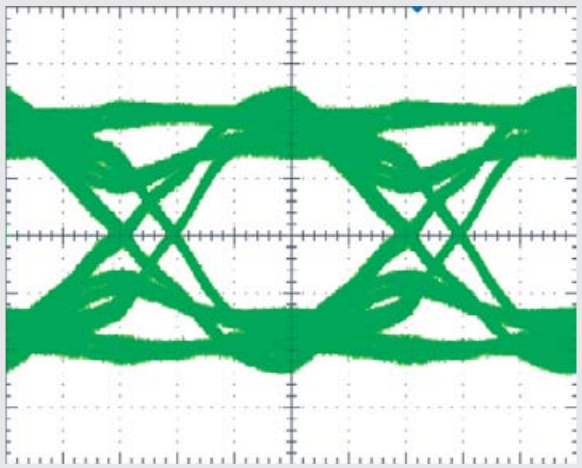


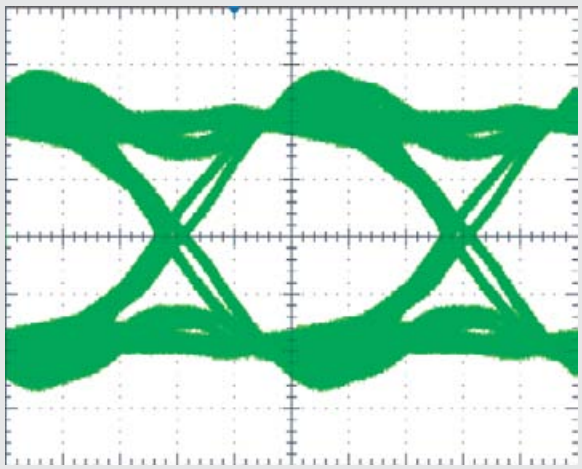
Figure 4. Measured 200-Mbps eye patterns when slot 1 drives 19-load bus



(a) At slot 1 driver output



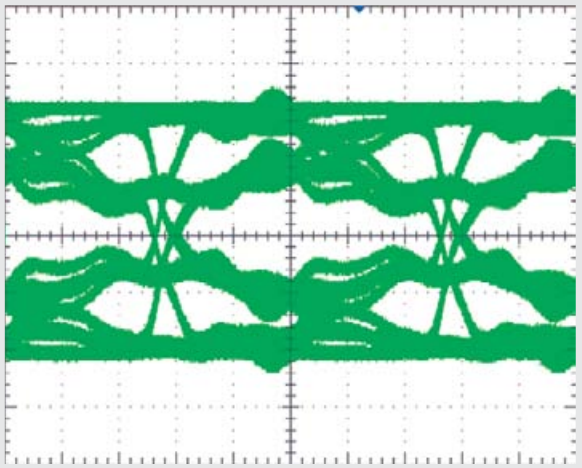
(b) At slot 10 receiver input



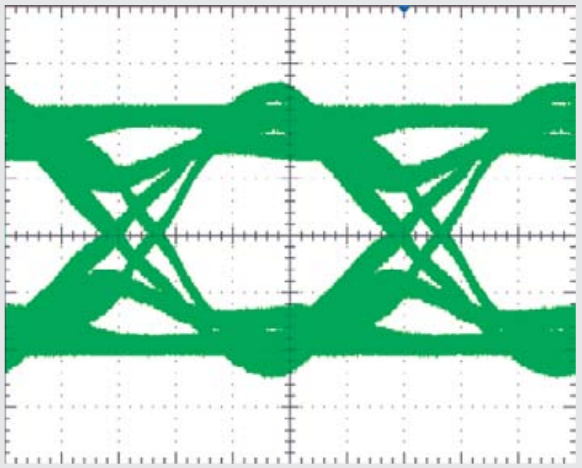
(c) At slot 19 receiver input

Figures 4 and 5 depict the measured results of the simulated waveforms in Figures 2 and 3. Comparing the simulation data to the measured data reveals that the modeling and simulation efforts in predicting the actual signal behavior on the bus are fairly accurate. For instance, the actual 200-Mbps eye pattern at the slot 1 driver output in Figure 4a has a lower amount of overshoot and more jitter than the simulation of the same case in Figure 2a. Because the voltage overshoot in the actual system is more dampened than that in the simulations, the signals in the actual

Figure 5. Measured 200-Mbps eye patterns when slot 10 drives 19-load bus



(a) At slot 10 driver output



(b) At slot 1 receiver input

system fall sooner than those in the simulated system. This causes the simulated results to predict a lower amount of jitter than that measured in the actual results. The simulated results, however, do accurately predict the minimum differential voltage in the measured eye pattern. Similar comparisons of overshoot, jitter, and differential voltage can be made between all of the simulated and actual results.

In conclusion, it is important to consider all aspects of backplane system design. As pitch between slots is decreased, the "per unit" distributed loading on the backplane increases and the effective backplane impedance is reduced. This can be mitigated by using a 130-Ω differential trace impedance, which helps increase the effective impedance in a heavily loaded backplane. Stub lengths should be kept short to minimize associated capacitance. The differential signal path should be carefully considered to help preserve data transmission within a noisy environment.

Each of the signaling technologies mentioned will satisfy certain needs. M-LVDS incorporates a controlled edge rate with LVDS-compatible signal levels. With the design guidelines previously discussed, implementing M-LVDS in a point-to-point, multidrop, or multipoint system can be successfully achieved. The 30-slot system demonstrates the robustness of M-LVDS drivers and the low capacitance of M-LVDS receivers supporting large bus systems up to and beyond 200-Mbps data rates (100-MHz clock rates). The PICMG 3.0 AdvancedTCA base specification calls for the use of M-LVDS for synchronization clocks across the backplane.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

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Auto-zero amplifiers ease the design of high-precision circuits

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A wide variety of electronic applications deal with the conditioning of small input signals. These systems require signal paths with very low offset voltage and low offset voltage drift over time and temperature. With standard linear components, the only way to achieve this is to use system-level auto-calibration. However, adding auto-calibration requires more complicated hardware and software and can slow down time to market for new products.

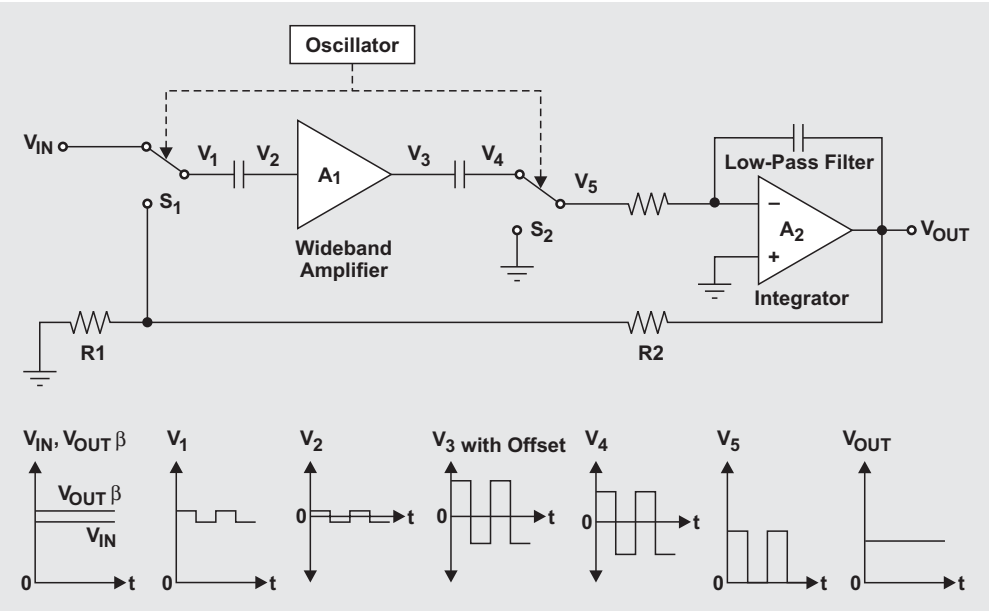
The alternative is to use components with low offset and low drift. The amplifiers with by far the lowest offset and drift available are the auto-zero amplifiers (AZAs). These amplifiers achieve high dc precision through a continuously running calibration mechanism that is implemented on-chip. With a typical input offset of 1 µV, a temperature-related drift of 20 nV/ºC, and a long-term drift of 20 nV/month, these amplifiers satisfy even the highest requirements of dc accuracy.

Today's AZAs differ neither in form nor in the application from standard operational amplifiers. There is, however, some hesitation when it comes to using AZAs, as most engineers associate them with the older chopper amplifiers and chopper-stabilized amplifier designs. This stigma has been perpetuated either by engineers who worked with the older chopper amplifiers and remember the difficulties they had with them, or younger engineers who learned about chopper amplifiers in school but probably did not understand them very well.

The original chopper amplifier heralded the beginning of the new era of self-calibrating amplifiers more than 50 years ago. This amplifier provided extreme low values for offset and drift, but its design was complicated and expensive. In addition, ac performance was limited to a few hertz of input bandwidth accompanied by a high level of output noise. Over the years, unfortunately, the term "chopper amplifier" became a synonym for any amplifier with internal calibration capability. Therefore, AZAs, often wrongly designated as chopper or chopper-stabilized amplifiers, are associated with the stigma of the older chopper technique.

This article shows that the auto-zero calibration technique is very different from the chopper technique and is one that, when implemented through modern process technology, allows the economical manufacturing of wideband, high-precision amplifiers with low output noise. The following discussion presents the functional principles of the chopper amplifier, the chopper-stabilized amplifier, and the AZA. It then compares the efficiencies of low-frequency filtering when applied to AZAs and standard operational amplifiers. Finally, three application examples demonstrate the use of an AZA as a signal amplifier and as a calibrating amplifier in dc—and wideband ac—applications.

Figure 1. Chopping principle in the time domain



Note: Labels for amplifiers such as A_{IN}, G_B, and A_M are used to identify amplifiers in figures and to represent amplifier gain in equations.

The chopper amplifier

Figure 1 shows a simplified block diagram of a chopper amplifier.

A dc input signal is chopped into an ac voltage and amplified by an ac-coupled amplifier. A phase-sensitive demodulator converts the output of A_1

back to dc. The demodulator consists of a switch S_2 that is synchronously driven to S_1. An integrator then smooths the switch output and presents the final dc output.

The circuit benefits from high overall dc gain and low baseband noise. The dc gain, being the product of the ac stage and the dc gain of the integrator, easily reaches an open-loop gain of 160 dB and reduces the gain error,

$$\frac{V_{OUT}}{A_1 A_2},$$

to almost zero.

The baseband is defined as the maximum usable input bandwidth. Baseband noise consists of the input offset voltage (also known as dc noise), the 1/f noise, and low-frequency white noise. The reduction of baseband noise happens in several steps:

- Offset and drift in the output integrator stage are nulled by the dc gain of the preceding ac stage.
- dc drifts in the ac stage are also irrelevant because they are isolated from the rest of the amplifier by the coupling capacitors.
- The 1/f noise of the ac amplifier is modulated to higher frequencies via the demodulator.

Figure 2 clarifies the process of noise reduction by demonstrating the effects of chopping in the frequency domain.

The chopping of the input signal constitutes an amplitude modulation (AM), with the chopping frequency, f_{CH}, being the carrier, and the input voltage representing the modulating signal. Both switches, S_1 and S_2, are replaced by the modulators, M_1 and M_2.

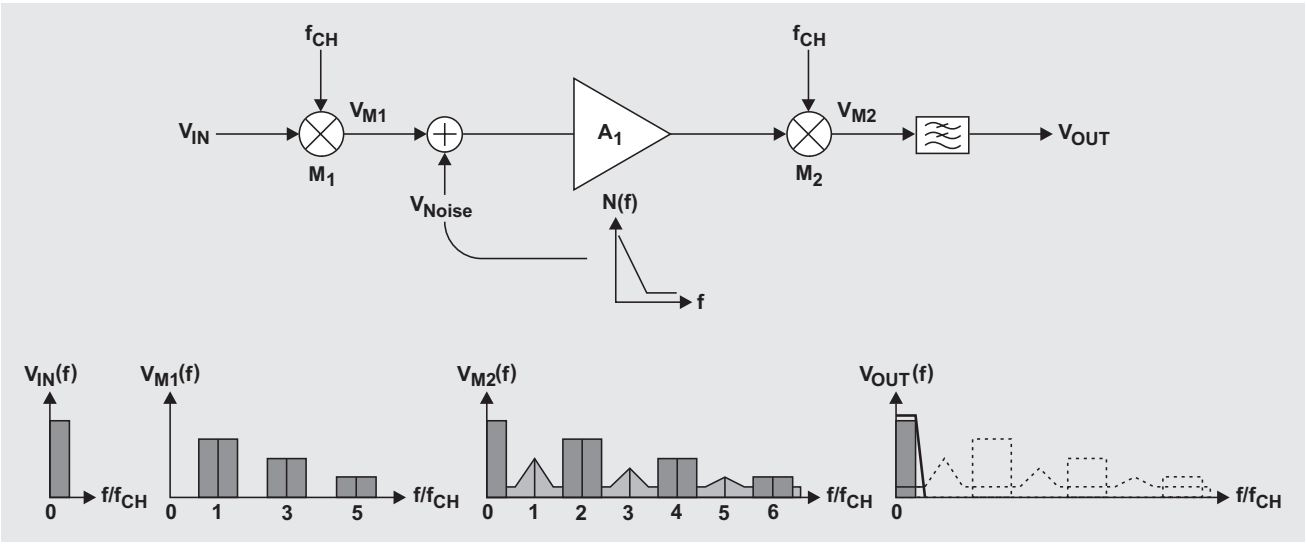
$V_{M1}(f)$ in Figure 2 shows that the modulation of a square wave causes sidebands of the input signal to appear on both sides of the odd harmonics of the chopper frequency. The amplitudes of the harmonics and their sidebands decrease following a 1/n function, with n indicating the order of the harmonic.

The 1/f noise of A_1 present in the baseband adds to the modulated input signal after the first modulation stage, M_1. The combined signal is amplified by A_1 and fed into the demodulator, M_2. The 1/f noise, experiencing its first modulation through M_2, introduces sidebands on both sides of the odd harmonics of f_{CH}. For the modulated input signal, however, M_2 represents the second modulating stage. V_{M1} is now demodulated, causing sidebands of the input signal to occur around the even harmonics of f_{CH}. The input signal reappears in the baseband, and the roll-off of the subsequent low-pass filter limits the baseband to frequencies far below the chopper frequency.

Note that the AM does not change the spectral density of the white noise. The residual baseband noise is therefore limited, low-frequency white noise.

Despite the small values for offset, drift and baseband noise, this approach has some drawbacks. First, the amplifier has a single-ended, noninverting input and cannot accept differential signals without additional circuitry at the front end. Second, the carrier-based approach constitutes a sampled data system, and overall amplifier bandwidth is limited to a small fraction of the chopper frequency. The chopper frequency, in turn, is restricted by ac amplifier gain-phase limitations and errors induced by switch response time. Maintaining good dc performance involves keeping the effects of these considerations small. Chopper frequencies are therefore in the low-kilohertz range, dictating low overall bandwidth.

Figure 2. Chopping principle in the frequency domain



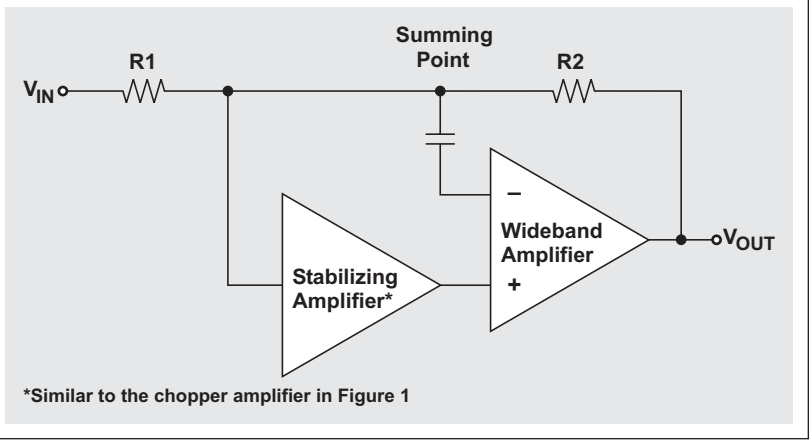
The chopper-stabilized amplifier

The classic chopper-stabilized amplifier solves the chopper amplifier's low-bandwidth problem. It uses a parallel path approach (Figure 3) to provide wider bandwidth while maintaining good dc characteristics. The stabilizing amplifier, a chopper type, biases the fast amplifier's positive terminal to force the summing point to zero.

Fast signals directly drive the ac amplifier, while slow ones are handled by the stabilizing chopper amplifier. The low-frequency cutoff of the fast amplifier must coincide with the high-frequency roll-off of the stabilizing amplifier to achieve smooth overall gain-frequency characteristics. With proper design, the chopper-stabilized approach yields bandwidths of several megahertz with the low-drift characteristic of the chopper amplifier. Unfortunately, because the stabilizing amplifier controls the fast amplifier's positive terminal, the classic chopper-stabilized approach is restricted to inverting operation only.

In addition, the high residual output noise of the chopper amplifier is amplified by the fast amplifier's noise gain. Keeping output noise small dictates additional filter effort, thus increasing complexity and cost of the chopper-stabilized design.

Figure 3. Chopper-stabilized amplifier

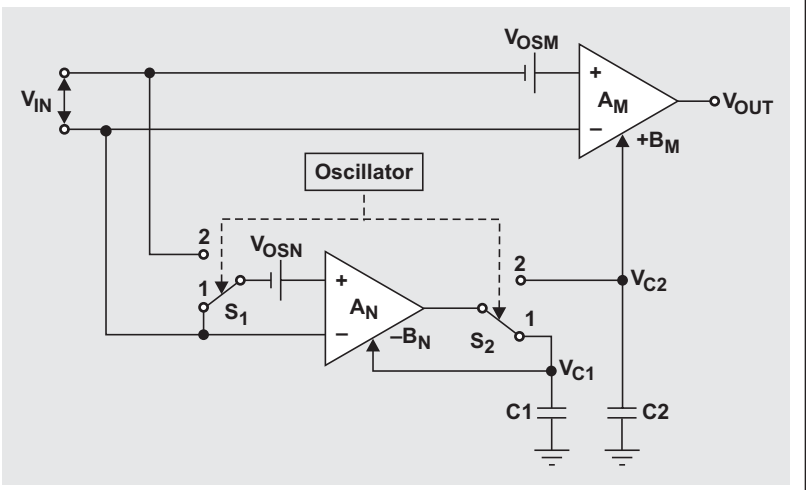


The auto-zero amplifier (AZA)

Similar to the chopper-stabilized approach, the AZA uses a main amplifier for wideband signal amplification and a nulling amplifier for offset correction. Figure 4 shows a block diagram of the TLC2654, an AZA developed by Texas Instruments in the mid-80s.

With the calibration path lying in parallel with the signal path, both inputs of the main amplifier are available for differential input operation.

Figure 4. Simplified TLC2654 block diagram



Note: Labels for amplifiers such as A_{IN}, G_B, and A_M are used to identify amplifiers in figures and to represent amplifier gain in equations.

The main amplifier, A_M, and the nulling amplifier, A_N, each have an associated input offset voltage (V_{OSM} and V_{OSN}, respectively) modeled as a dc offset voltage in series with the noninverting input. The open-loop gain of the signal inputs is given as A_M and A_N. Both amplifiers also have additional voltage inputs with the associated open-loop gains of $+B_M$ and $-B_N$.

Offset correction of the overall amplifier occurs within one cycle, f_{AZ}, of the auto-zero clock and is split into two modes of operation: an auto-zero phase and an amplification phase. The oscillator, generating f_{AZ}, initiates the auto-zero phase by driving both switches into position 1. The inputs of the nulling amplifier are shorted together, while its output is connected to capacitor C1. In this configuration A_N measures its input offset voltage and stores it via C1. Mathematically we can express the voltage at C1 as

$$V_{C1} = A_N V_{OSN} - B_N V_{C1},$$

which, by simple rearrangement, is

$$V_{C1} = V_{OSN}\left(\frac{A_N}{1+B_N}\right). \quad (1)$$

This shows that the offset voltage of the nulling amplifier times a gain factor appears at the output of A_N and thus on the C1 capacitor.

In the amplification phase, when both switches are in position 2, this offset voltage remains on C1 and essentially corrects any error from the nulling amplifier. A_N amplifies

V_{C1} by the factor B_N and subtracts it from the amplified input signal,

$$A_N(V_{IN} + V_{OSN}).$$

At the same time, the output of A_N charges capacitor C2 to

$$V_{ON} = V_{C2} = A_N(V_{IN} + V_{OSN}) - B_N V_{C1}.$$

Replacing V_{C1} with Equation 1 results in

$$V_{C2} = A_N\left(V_{IN} + \frac{V_{OSN}}{1 + B_N}\right). \quad \textbf{(2)}$$

Equation 2 shows that V_{OSN} has been reduced by a factor $1 + B_N$, indicating how the nulling amplifier reduces its own offset voltage error even before correcting the main amplifier. The potential, V_{C2}, now serves the main amplifier as an offset correcting voltage, forcing its output, and thus the output of the complete AZA, to

$$V_{OUT} = A_M(V_{IN} + V_{OSM}) + B_M V_{C2}.$$

Replacing V_{C2} with Equation 2 and combining terms gives us

$$V_{OUT} = V_{IN}(A_M + A_N B_N) + V_{OSM}A_M + V_{OSN}\left(\frac{A_N B_M}{1 + B_N}\right). \quad \textbf{(3)}$$

The auto-zero architecture is optimized in such a way that $A_M = A_N$, $B_M = B_N$, and $B_N >> 1$. This allows Equation 3 to be simplified to

$$V_{OUT} = V_{IN}A_N B_N + A_N(V_{OSM} + V_{OSN}). \quad \textbf{(4)}$$

Most obvious is the gain product of both the main and nulling amplifiers. The $A_N B_N$ term in Equation 3 explains why AZAs have extremely high open-loop gain. To understand how V_{OSM} and V_{OSN} relate to the overall effective input offset voltage of the complete amplifier, we should set up the equation for the generic amplifier in Figure 5:

$$V_{OUT} = k(V_{IN} + V_{OS\_Eff}), \quad \textbf{(5)}$$

where k is the open-loop gain of the amplifier and V_{OS_Eff} is its effective offset voltage.

Putting Equation 4 into the form of Equation 5 gives us

$$V_{OUT} = A_N B_N\left(V_{IN} + \frac{V_{OSM} + V_{OSN}}{B_N}\right).$$

From here it is easy to see that $k = A_N B_N$ and

$$V_{OS\_Eff} = \frac{V_{OSM} + V_{OSN}}{B_N}.$$

Thus, the offset voltages of both the main and the nulling amplifiers are reduced by the gain factor B_N. If we consider the open-loop gains of the local amplifiers, A_N and A_M, to be in the region of 10,000 or higher, it quickly becomes evident that even an inherent offset voltage of millivolts is reduced to an effective input offset voltage of microvolts for the complete AZA.

The AZA constitutes a sampled data system. The process of sampling therefore generates frequencies consisting of the sum and difference of the input signal frequency, f_S, and the auto-zero clock frequency, f_{AZ}. The summing frequency, $f_{AZ} + f_S$, can be filtered easily and is therefore of little importance. However, the difference frequency, $f_{AZ} - f_S$, can alias into the baseband if $f_S \geq f_{AZ}/2$. Older AZA designs therefore required the limitation of the input bandwidth to less than half of the auto-zero frequency. Most of the amplifiers available in the mid-80s had typical clock frequencies in the range of only 400 to 500 Hz, thus narrowing the signal bandwidth down to 250 Hz. The TLC2654 was one of the first amplifiers that allowed high-frequency auto-zeroing at 10 kHz, thus extending the input bandwidth up to 5 kHz.

The breakthrough to real wideband operation happened only with the recent introduction of AZAs such as the OPA335. Modern process technology, with gate structures in the submicron region, made the economical integration of complex anti-aliasing circuitry possible. The strong attenuation of alias frequencies enabled wideband operation across the entire amplifier bandwidth.

Figure 5. Generic amplifier with effective offset

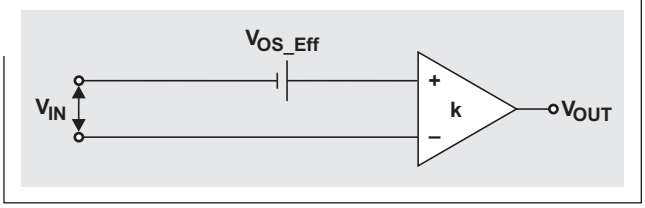


Figure 6 shows the inner structure of the OPA335. The two nulling amplifiers, A_{N1} and A_{N2}, operate in an alternate mode in parallel with the main amplifier, A_M. While A_{N1} nulls its offset during the auto-zero phase, A_{N2} is in the amplification phase, correcting the main amplifier's offset voltage and vice versa.

The alternating operation of the nulling amplifiers minimizes output voltage ripple and intermodulation distortion (IMD) by keeping the amplifier's gain bandwidth constant during operation. Proprietary circuit design has made further improvements to the nulling amplifiers. Each amplifier consists of a multistage composite amplifier. This configuration drastically reduces the quiescent current down to 300 µA (versus the 1.5 mA of the TLC2654) while maintaining a high open-loop gain of 130 dB. In addition, the previous external capacitors have been made redundant by achieving the same effective capacity values through Miller equivalence.

Let's return to the process of auto-zeroing. The nulling amplifier, whose switches are in position 1, is in the auto-zero phase, thus charging its capacitor to

$$V_C = G_B(A_{IN}V_{OSN} - A_Z V_C) = V_{OSN}\left(\frac{G_B A_{IN}}{1+G_B A_Z}\right). \quad \textbf{(6)}$$

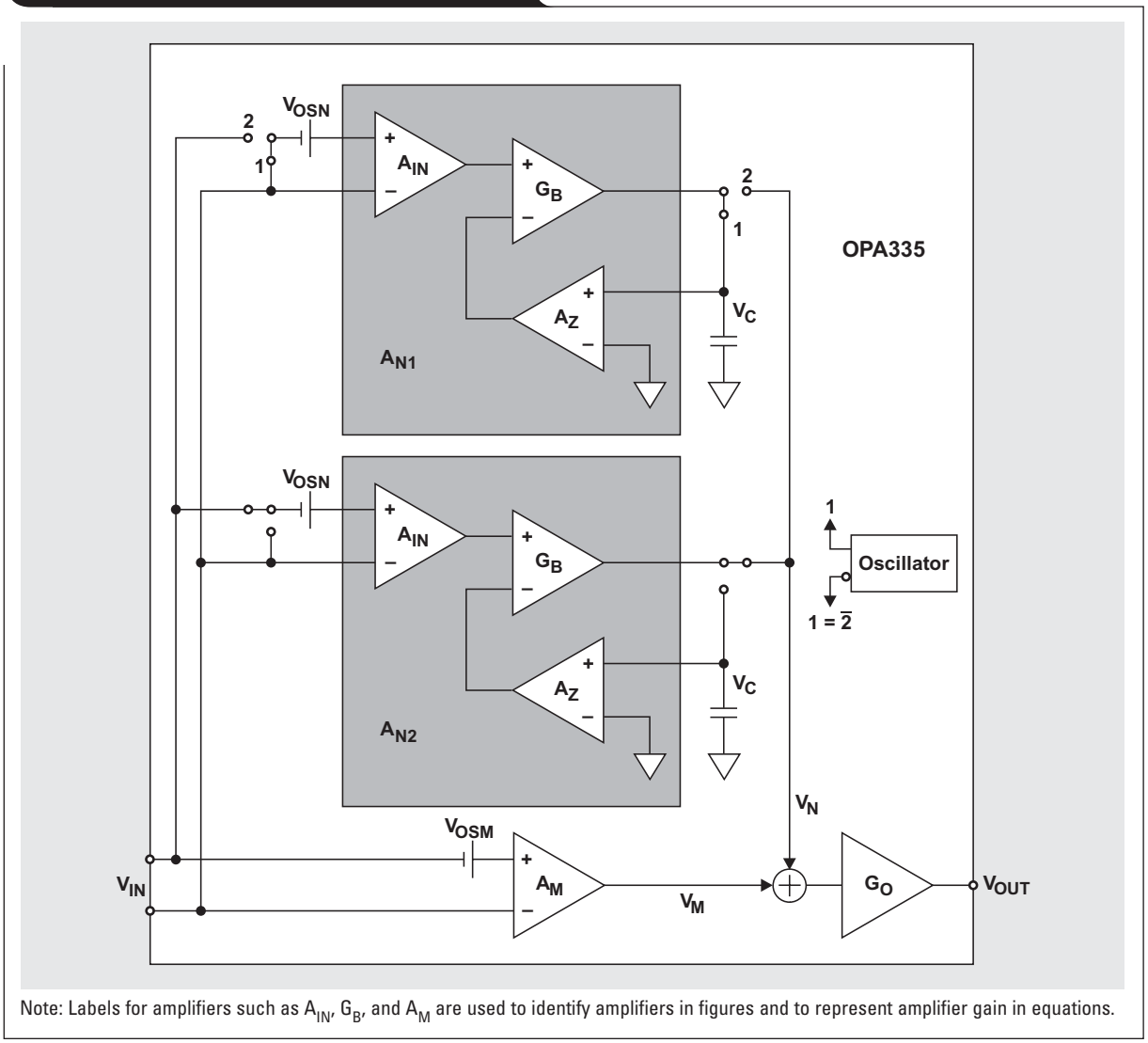
During the amplification phase (with switches in position 2), the output voltage of the nulling amplifier, V_N, adds to the output voltage of the main amplifier, V_M. With

$$V_N = G_B\left[A_{IN}(V_{IN} + V_{OSN}) - A_Z V_C\right],$$

we can replace V_C with Equation 6 to obtain

$$V_N = G_B A_{IN}\left(V_{IN} + \frac{V_{OSN}}{1+G_B A_Z}\right). \quad \textbf{(7)}$$

Figure 6. Simplified OPA335 block diagram



Note: Labels for amplifiers such as A_{IN}, G_B, and A_M are used to identify amplifiers in figures and to represent amplifier gain in equations.

The output of the main amplifier is simply

$$V_M = A_M\left(V_{IN} + V_{OSM}\right). \quad \textbf{(8)}$$

The following output stage amplifies the summing signal by the factor G_O to

$$V_{OUT} = G_O(V_N + V_M). \quad \textbf{(9)}$$

Inserting Equations 7 and 8 into Equation 9 yields

$$V_{OUT} = G_O\left[A_M(V_{OSM} + V_{OSN}) + G_B A_{IN}\left(V_{IN} + \frac{V_{OSN}}{1 + G_B A_Z}\right)\right]. \quad \textbf{(10)}$$

During the design process, the auto-zero structure is so optimized that $A_M = A_N$ and $G_B >> 1$. This simplifies Equation 10 to

$$V_{OUT} = G_O G_B A_{IN}\left(V_{IN} + \frac{V_{OSM} + \frac{V_{OSN}}{A_Z}}{G_B}\right),$$

with $G_O G_B A_{IN}$ as the overall open-loop gain and

$$\frac{V_{OSM} + \frac{V_{OSN}}{A_Z}}{G_B}$$

as the effective input offset voltage of the complete AZA.

Output noise filtering

High dc accuracy often requires additional noise filtering. How low a filter's 3-dB frequency can be to provide effective noise filtering is all too often ignored. A comparison between a standard CMOS op amp and an AZA provides valuable insight.

Figure 7 shows that the spectral noise density of a standard op amp consists of two noise characteristics: the 1/f region where noise density decreases with increasing frequency, and the white noise region with constant spectral density. At corner frequency f_C, the magnitude of 1/f noise equals the magnitude of white noise density.

For signal-to-noise ratio calculations we require the rms value of the noise within a defined frequency band. Applying a first-order low-pass filter with a –3-dB cutoff at frequency f_H yields an rms noise voltage of

$$V_{rms} = v_{nw}\sqrt{f_C \ln\frac{f_H}{f_L} + 1.57f_H - f_L},$$

where v_{nw} is the white noise spectral density, f_C is the corner frequency of the 1/f- and white-noise transition, f_H is the upper frequency of the noise frequency band and filter cutoff, and f_L is the lower frequency of the noise frequency band (here assumed to be 10^{-30} Hz).

Various rms voltages have been calculated with the preceding equation by varying the –3-dB frequency of a first-order low-pass filter. The resulting plot is shown in Figure 8. It is important to notice that lowering the filter's cutoff below $10f_C$ seems inefficient, since the rms noise hardly decreases.

In contrast to a standard op amp, the continuous offset cancellation of an AZA removes the typical 1/f characteristic and creates the white noise spectral density in Figure 7 instead. Applying the same low-pass filter provides an rms noise of

$$V_{rms} = v_{nw}\sqrt{1.57f_H}.$$

Plotting the rms values for various cutoff frequencies results in the positive slope in Figure 8. It can be seen that reducing the filter cutoff down to low frequencies is effective in establishing high dc accuracy.

One contributor to high-frequency output noise is clock feedthrough. This term is broadly used to indicate visibility of the auto-zero clock frequency in the amplifier output spectrum. There are typically two types of clock feedthrough. The first is caused by the settling time of the

Figure 7. Spectral noise density

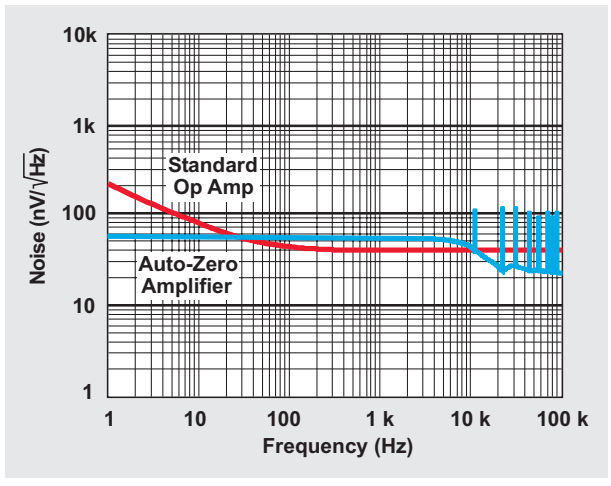


Figure 8. rms noise voltage

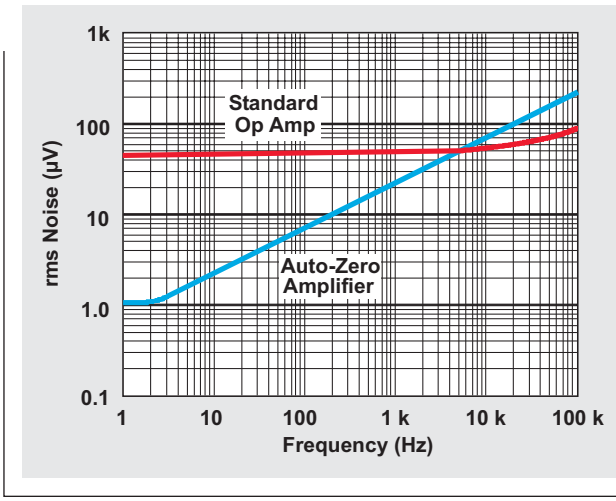
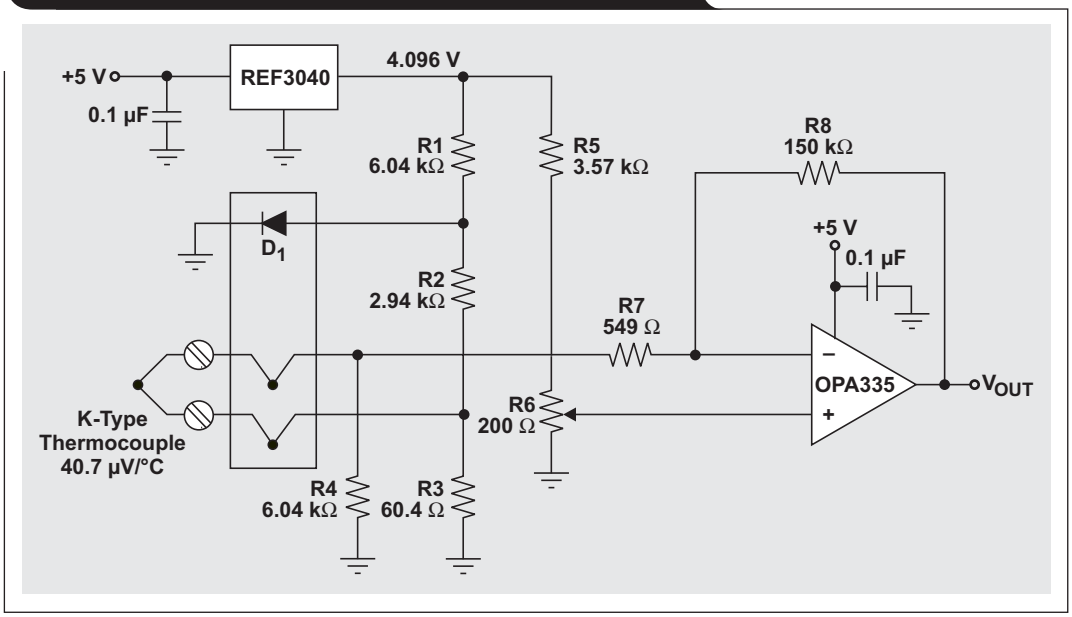


Figure 9. Temperature measurement via thermocouple



internal sampling capacitors and is input-referred. The second is caused by the small amount of charge injection occurring during the sampling and holding of the amplifier's input offset voltage.

The OPA335, however, has remarkably little noise. Although zero correction occurs at a 10-kHz rate, there is virtually no fundamental noise energy present at that frequency. For all practical purposes, any glitches have energy at 20 MHz or higher and are easily filtered if required. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

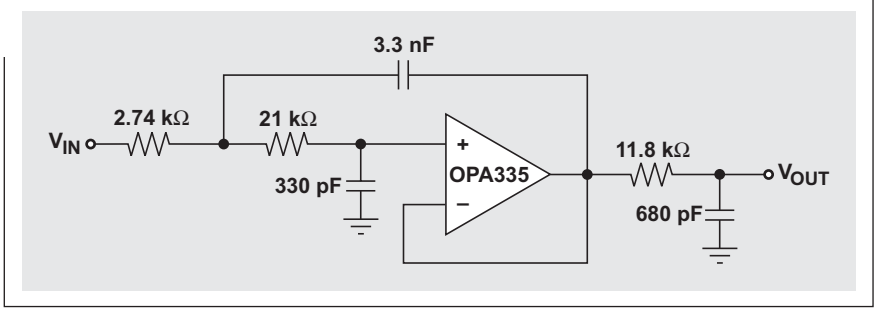
Applications

The temperature measurement circuit in Figure 9 is a low-frequency application that allows the OPA335 to be switched directly into the signal path.

A precision voltage reference provides the 4.096-V bridge supply. The forward voltage of diode D1 has a negative temperature coefficient of –2 mV/°C and provides cold-junction compensation via the resistor network R1 to R3. The zero adjustment for a defined minimum temperature is achieved via R6, while R7 and R8 set the gain for the output amplifier. The single-supply amplifier providing an open-loop gain of 130 dB allows 16-bit or better accuracy at high gain in low-voltage applications. Auto-zeroing removes 1/f noise and provides typical values of 1 µV of input offset and 20 nV/°C of offset drift over temperature. Thus, AZAs ideally suit single-supply precision applications where high accuracy, low drift, and low noise are imperative.

The third-order low-pass filter in Figure 10 has a corner frequency of 20 kHz, which is twice as high as the auto-zero clock frequency. Aliasing and intermodulation noise are highly attenuated, which permits input signal operation across its entire gain bandwidth. In addition, the amplifier's output provides rail-to-rail drive capability, allowing for a high signal-to-noise ratio at low supply voltages.

Figure 10. A 20-kHz, third-order low-pass filter



In wideband applications with bandwidths in the tens of megahertz, the AZA provides dc accuracy to a wideband amplifier. Figure 11 shows the required circuit configuration in the form of a composite amplifier design.

The AZA functions as an integrator operating in the "bias path" of the wideband amplifier. The signal path still runs from V_{IN} via R_G and R_F to V_{OUT}. The integrator has two functions. At low frequencies, it provides high gain to the offset-cancellation loop, reducing the input offset of the wideband amplifier down to the input offset of the AZA. At high frequencies, a large time constant (R_{INT}, C_{INT}) ensures that the integrator's closed-loop gain quickly decreases to prevent signal transfer to the noninverting input of the wideband amplifier.

Note that the amplifier's input noise is amplified by the noninverting closed-loop gain of the integrator. Thus, at high frequencies, the OPA335 operates as a voltage follower (gain = 1), passing its input noise on to the wideband amplifier. To eliminate this noise, a low-pass filter (R2, C2) with low-frequency cutoff is added to the output of the AZA. The same precaution is taken for the OPA353. Here the low-pass filter (R1, C1) limits the output noise of the wideband amplifier.

To compensate for the signal voltage drop across R1, the feedback loop is closed by connecting the right side of R_F to the filter output. The internal feedback loop via C_F establishes stability at high frequencies by compensating the phase shift of the low-pass filter.

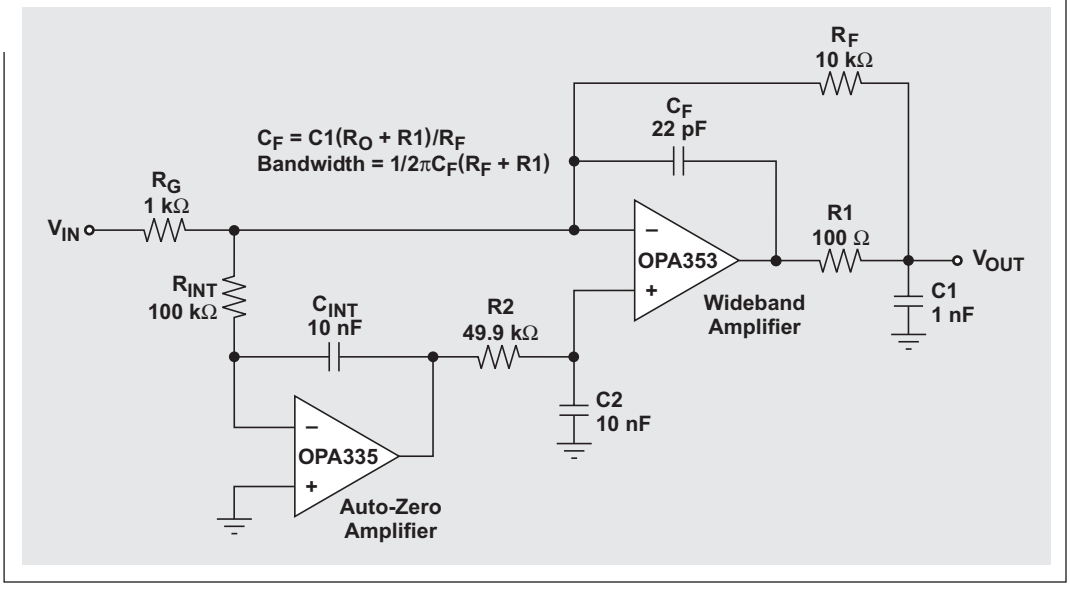
Summary

True chopper- and chopper-stabilized amplifiers perform offset correction through amplitude modulation. These amplifiers are not available as integrated circuits but require multiple amplifier integrated circuits instead. The circuit design is therefore complicated and time- and cost-intensive. Despite the extreme low values for input offset voltage and drift, ac performance is limited to a small fraction of the chopper frequency and is accompanied by high levels of output noise.

AZAs perform offset correction by a sample-and-hold method. Older-generation amplifier designs benefited from integrated circuit design. Aliasing and IMD, however, narrowed the input bandwidth down to half the auto-zero clock frequency. These devices required supply voltages of 10 V minimum and had quiescent currents in the range of milliamperes. In addition, external capacitors were needed to store the offset-correcting voltages.

Today's AZAs are by far the most sophisticated precision amplifiers available. Advancements in process technologies have drastically lowered the effects of aliasing and IMD, thus enabling true differential signal operation across the entire gain bandwidth of the amplifier. Proprietary circuit design has reduced the amount of supply voltage and quiescent current significantly, allowing for low-power operation in high-gain, high-precision applications. The integration of the external storage capacitors in combination with the given performance enhancements makes AZAs as easy to use as standard CMOS op amps.

Figure 11. Auto-zeroed wideband amplifier



In addition to operational amplifiers, the auto-zero technique has also been implemented in a wide range of other signal conditioning components such as:

- the OPA734/735 op amps with extended supply range from 2.7 to 12 V;
- the OPA380 wideband transimpedance amplifier;
- the INA326 instrumentation amplifier for single-supply applications;
- the INA330 instrumentation amplifier for constant temperature control; and
- the PGA309, a fully integrated pressure sensor conditioning system on-chip.

Future design ideas aim to shape the noise floor of extremely high-gain-bandwidth amplifiers by shifting energy from the baseband to higher, out-of-band frequencies. This would approach the ideal op amp—an interesting concept that may not be far in the future.

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with INA326, INA330, OPA335, OPA353, OPA380, OPA734, OPA735, PGA309, REF3040, or TLC2654

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