Powering today's multi-rail FPGAs and DSPs, Part 1

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Applications, Portable Power

Introduction

Most electronics have one or more digital processing ICs, such as FPGAs or DSPs, that require multiple power-supply rails. There are various options to consider and potential pitfalls to avoid in powering these digital ICs. This article, Part 1 of a two-part series, provides recommendations and guidance for developing a power solution for multi-rail applications where the input power supply voltage is assumed to be equal to or greater than the system rail voltage (e.g., 12, 5, or 3.3 V). Part 2, which will appear in a future issue of *Analog Applications Journal*, will focus on how to choose between the types of dc/dc converters and how to design them to meet dc accuracy, start-up, and transient requirements.

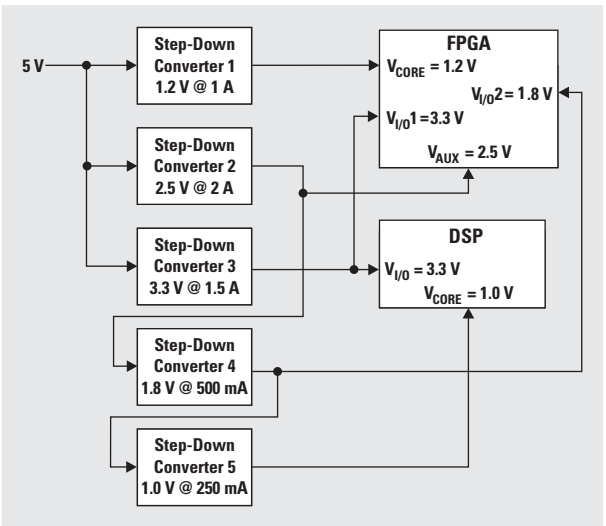
Application-specific requirements

Application-specific requirements drive the overall dc/dc power solution. While most system designers desire a simple power solution with low component cost, they must also consider the type of circuitry being powered as well as the differential between the input power supply and each power rail. FPGA and DSP core and I/O voltage rails already have switching noise riding on the rail due to the millions of internal transistors that are switching on and off. So, in general, these "digital" rails can be powered from switching power supplies without concern for the switching noise. Conversely, rails that power audio circuitry, transceiver circuitry, clock signals, phase-lock loops, or other noise-sensitive circuitry—termed "analog" rails—should be powered from a linear regulator or low-noise, fixed-frequency PWM converter. These rails may even require additional filtering on the power rail as specified by the analog IC vendor. In addition, noise-sensitive circuitry may be affected by noise emitted from switching regulators, so recommended board layouts for switching regulators should be followed and shielded inductors used. Restrictions on the range of switching frequency and/or synchronization of all switching regulators to one switching frequency may be necessary to make filtering easier. Once the type of circuitry being powered has been reviewed, the differential between the input power supply voltage and each power rail voltage—and therefore the power dissipation that each rail's converter must withstand—must be considered. An easy way to do this is to prepare a power budget.

The power budget

Shrinking process nodes have resulted in core rails dropping from 2.5 to 1.2 V or even below 1.0 V. However, wall-brick voltages and many bus voltages used as the input supply to the point-of-load (POL) dc/dc converters that provide the core voltages have remained at 12, 5, and 3.3 V. The dc/dc converters providing such voltages must be able to handle the power dissipation. Also, as the efficiency of the individual POL converters drops, the output power of the input power supply increases. Although the static or quiescent current for a digital IC is typically provided in the datasheet, estimating the maximum current for a specific FPGA configuration or software program (sometimes referred to as "dynamic current") is often difficult to do. Fortunately, all FPGA and DSP manufacturers provide either online power-consumption estimators or downloadable software that takes key, application-specific design criteria and provides at least a working estimate of the maximum current draw. Once the current, and therefore power, consumption for each rail is known, a power solution can be constructed. The block diagram in Figure 1 shows one of many possible power solutions for an application containing one FPGA and one DSP.

Figure 1. Simplified application with one FPGA and one DSP



Note that instead of pulling all of the rail voltages from the 5-V input supply, the design uses the FPGA's required 2.5-V rail as a mid-level bus voltage to more efficiently provide the 1.8-V rail and then uses the 1.8-V rail to provide the 1.0-V rail. If all of the POL converters are assumed to be inexpensive linear regulators, then the power budget in Table 1 shows that the input supply must provide at least 4.5 A. Also, converters 1 and 2 must dissipate 3.8 and 5 W, respectively, which is difficult for a surface-mount-packaged linear regulator to do without additional air flow or an external heat sink.

The power budget in Table 2 assumes that converters 1, 2, and 3 are buck-switching converters. With higher efficiencies as well as reduced input current, switching regulators eliminate power dissipation concerns and allow the use of a lower-power, less expensive wall brick for the input supply.

Good power-supply design techniques

Designing a multi-rail-powered system without considering the power-up timing of each rail poses several dangers that can threaten immediate and long-term device reliability. Improper rail timing can magnify latent faults and possibly damage I/O ports in the processor or supporting system devices such as memory, logic, or data-converter ICs. A long-term threat comes from the possibility of breakdown in the ESD protection and well-isolation structures that internally separate the two power-supply rails. If one rail is active while another is inactive for extended periods—i.e., months—or for repeated shorter periods that accumulate over the lifetime of the device, damage may occur.

A latch-up condition may cause damage that is immediately noticeable, or it may affect reliability over a long period of time. Latch-up occurs when current forced through the substrate of a CMOS device triggers a self-sustained conduction path in back-to-back, parasitic bipolar transistors (as in an SCR). Current continues to flow until the device fails or the supply powers down. The trigger current may occur if a supply powers one device, enabling it to source or sink current into or out of the second device before the second device fully powers up. A system can also trigger a latch-up if it drives an input pin above or below the power-supply rails after both devices have powered up. Bidirectional I/O ports have historically been another source of system failures. When a processor's I/O port and that of a supporting peripheral, such as memory or a data converter, do not share the same supply, the potential for latch-up exists. Bus contention occurs when multiple devices simultaneously attempt to control a bidirectional bus during power-up, which can affect I/O reliability. Similar undesirable conditions where a "sneak" path from the rising input rail(s) to ground is temporarily created by transistors in unknown states can cause a digital device to pull large inrush currents, which may cause immediate damage or cumulative long-term reliability concerns. Recently, FPGA and DSP manufacturers have improved protection circuits to reduce the risk of latch-up, bus contention, and similar undesirable states.

As further protection against these problems, the following simple-to-implement power-supply design practices are recommended. First, ensure that any logic peripheral connected to the processor I/O bus is powered from the same supply rail that powers the processor's I/O section. Second, ensure that the individual converters providing the rails regulate within the specified tolerance over the entire input voltage and load range during a transient

Table 1. Power budget assuming that all linear regulators are used

POL CONVERTER	V_{OUT} RAIL (V)	ESTIMATED I_{OUT} (A)	P_{OUT} (W)	POL CONVERTER V_{IN} (V)	ESTIMATED EFFICIENCY (%)	$P_{IN} = P_{OUT}/EFFICIENCY$ (W)	I_{IN} REQUIRED $= P_{IN}/V_{IN}$ (A)	POWER DISSIPATED (W)
5 Linear	1	0.25	0.25	1.8	56	0.45	0.25	0.20
4 Linear	1.8	0.5	0.9	2.5	72	1.25	0.50	0.35
3 Linear	3.3	1.5	4.95	5	66	7.50	1.50	2.55
2 Linear	2.5	2	5	5	50	10.00	2.00	5.00
1 Linear	1.2	1	1.2	5	24	5.00	1.00	3.80
TOTAL						**22.50**	**4.50**	

Table 2. Power budget assuming that switchers and linear regulators are used

POL CONVERTER	V_{OUT} RAIL (V)	ESTIMATED I_{OUT} (A)	P_{OUT} (W)	POL CONVERTER V_{IN} (V)	ESTIMATED EFFICIENCY (%)	$P_{IN} = P_{OUT}/EFFICIENCY$ (W)	I_{IN} REQUIRED $= P_{IN}/V_{IN}$ (A)	POWER DISSIPATED (W)
5 Linear	1	0.25	0.25	1.8	56	0.45	0.25	0.20
4 Linear	1.8	0.5	0.9	2.5	72	1.25	0.50	0.35
3 Switching	3.3	1.5	4.95	5	93	5.32	1.06	0.37
2 Switching	2.5	2	5	5	90	5.56	1.11	0.56
1 Switching	1.2	1	1.2	5	80	1.50	0.30	0.30
TOTAL						**12.38**	**2.47**	

event. This is explained more fully in Part 2 of this series. Third, ensure that all of the rails power up monotonically within a relatively short time (typically ≤ 100 ms) or the same time as each other so that the time of unexpected differential between the rails during startup is minimized.

Implementing sequencing

Sequencing refers not only to the order in which voltage rails power up and down but also to their timing and voltage-differential relationships. FPGA and DSP manufacturers rarely require a specific sequencing order for their power rails, but when they do, it should always be followed. A recommended sequencing order usually means that the manufacturer has performed at least a limited set of successful power-up tests with that device.

There are three methods for controlling power-up sequencing: simultaneous, ratiometric, and sequential. Figure 2 shows an example of simultaneous sequencing in which both rails ramp simultaneously, with the lower rail stopping at its regulation point. The rails initially rise at the same dv/dt, and the time that each rail is outside of its regulation tolerance is minimized. Therefore, simultaneous sequencing is generally considered to be the ideal sequencing method because it prevents latch-up, bus contention, and undesirable transistor states. However, it is also the most difficult to implement without special circuitry that allows interaction between each converter.

Ratiometric sequencing is shown in Figure 3. In ratiometric sequencing, the rails rise at different dv/dt rates, with the higher rail having a higher slew rate, so that they each arrive at their regulation point at the same time. Also, note that the maximum voltage differential occurs at the point of regulation. This sequencing method can be easily implemented if the dc/dc converters have an externally controllable soft start (discussed later).

Figure 4 shows the easiest and simplest method for soft-start sequential sequencing. By simply tying the output voltage (or available power good signal) of the first converter to the second converter and so on, sequential sequencing can be implemented. Maximum differential between the voltage rails can occur with this method; but as long as all of the rail voltages rise quickly enough relative to each other, the risk of immediate damage or long-term reliability problems is negligible. In addition, many of the recommended sequencing requirements for FPGAs and DSPs are sequential, since this is the simplest method around which to build a test setup.

Power-down sequencing is difficult to manage because the rail capacitance and resistive loading determine the voltage profile of each rail during power down. In other words, even if rail 1 is disabled before rail 2, rail 1 may have a larger capacitive load and smaller resistive load than rail 2; so rail 1 will discharge after rail 2. In addition, power down can occur as a result of several scenarios, including situations in which the loading on either rail changes during power down and is different from one power-down event to another. Additional circuitry is necessary that either discharges the rail voltages with a

Figure 2. Simultaneous sequencing

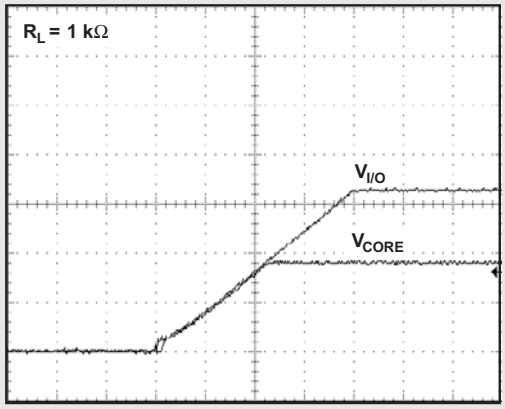


Figure 3. Ratiometric sequencing

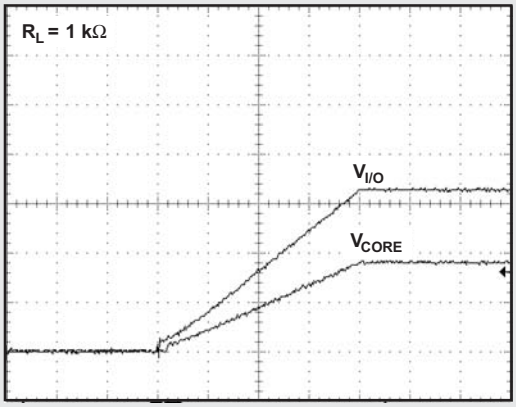
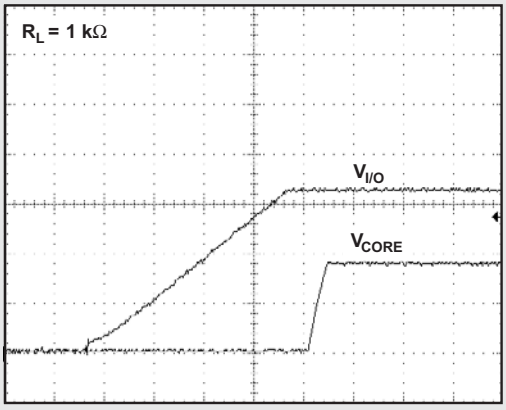


Figure 4. Sequential sequencing

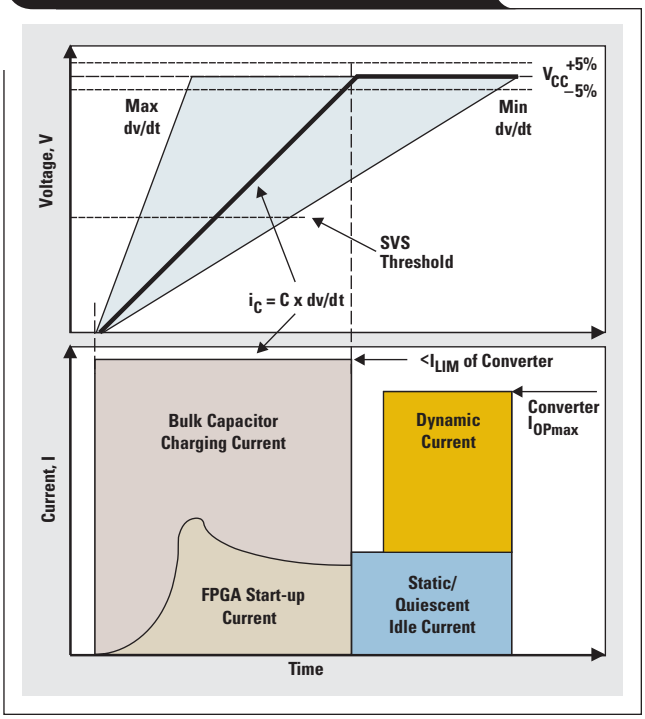


known load each time or actively monitors all rails and forces them to track each other (e.g., simultaneous sequencing). The smooth, monotonic rise of each individual rail, as Figures 2–4 show, may also be a requirement.

Implementing a controlled monotonic rise of the power rail

A monotonic rise at startup is shown in the top graph of Figure 5. Many FPGAs use an internal supply voltage supervisor (SVS) on each power rail, so a monotonic rise is necessary for the SVS circuit to successfully power up the rest of the IC. Many DSPs require an externally provided SVS or RESET signal that indicates when all the power rails are up, so monotonic rise is less important.

Figure 5. Start-up voltage and current



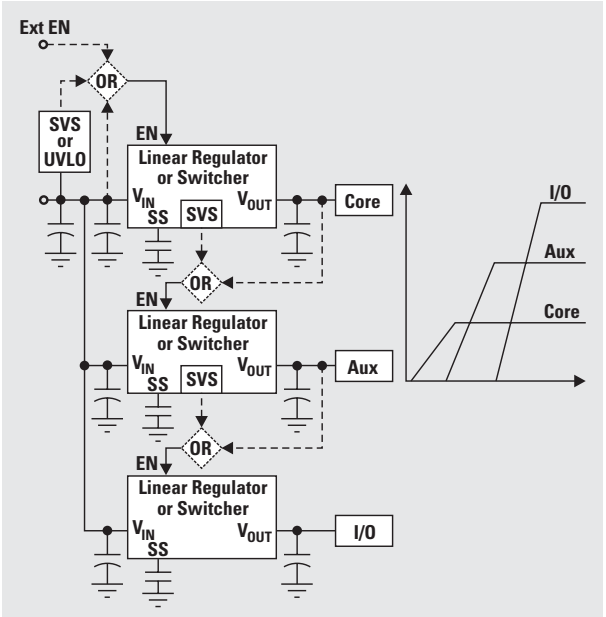
During startup, the capacitors on the power rail are charging due to current flowing into them. In addition to this current, some older, multi-rail FPGA and DSP ICs require large current surges during startup due to bus contention or other undesirable transistor states. Maximum voltage rail ramp time requirements (causing minimum dv/dt slew rates and slower start-up times) place a limit on the length of time that subcircuits within the IC are held below their operating voltage. In some older digital ICs, slower ramping core voltage rails reduced the start-up surge current into the IC. As illustrated in the bottom graph of Figure 5, many of the newer FPGAs and DSPs have resolved such start-up issues (e.g., by sequentially starting up different sections of the IC), and their start-up currents are well below the expected dynamic current levels. So for the most recent FPGAs and DSPs, the current for charging bulk capacitance in the rail's decoupling network dominates the start-up inrush current. Using $i_C = C \times dv/dt$, where C is the bulk capacitance and dv/dt is the selected ramp rate, we can easily see that the peak current could potentially be larger than the digital IC's dynamic current or the maximum operating current of that rail's converter. Minimum voltage ramp time requirements (resulting in maximum dv/dt slew rates and fast start-up times) for FPGA or DSP voltage rails arise for a variety of reasons, including IC testing limitations. Regardless of whether or not minimum ramp time requirements are present, the POL converter should be soft started to ensure that the inrush current for charging bulk capacitance does not exceed the current limit of the converter, potentially causing it to start up improperly as it protects itself from damage from the overcurrent. Part 2 of this series shows examples of two common start-up problems seen when converters/regulators are used and explains how to use soft start to control the voltage rail ramp rate and fix these problems.

Methodology

Compiling the previous recommendations, Figure 6 provides a simple method for powering up each of the digital ICs in the simplified application in Figure 1.

The choice of linear or switching regulators depends on the rail's power consumption (i.e., the efficiency needed for power dissipation) and/or the application needs (i.e., low-noise requirements). This method assumes that the application is configured to allow the FPGA or DSP to be powered up before the other (i.e., sequentially). The power solution in Figure 6 uses sequential sequencing of each digital device by tying the output voltage, if high enough, or the integrated or external SVS of the first rail

Figure 6. Block diagram of power solution



to the enable pin of the next rail. Although the example in Figure 6 shows the default sequencing order of core voltage, auxiliary voltage(s), and I/O voltage, the exact sequencing order should follow the FPGA or DSP manufacturer's recommendations, if any. In some cases, the recommended sequencing order may not be required for successful power up or to prevent damage, but it may reduce start-up currents. Compared to the other sequencing methods, sequential sequencing is easier to implement and further minimizes start-up currents by staggering power-rail startup. Using a POL converter with a soft start that allows the power rail's rise time to be controlled is also highly recommended and may even be required if the FPGA or DSP has minimum rise- and fall-time requirements for one or more power rails. The external SVS with controlled delay is necessary for many DSPs requiring an external RESET signal. The last, but arguably the most important, step in the power-supply design process is designing for load transients.

Conclusion

Designing a multi-rail power solution involves more than simply minimizing size and cost. System level and/or application requirements, such as noise sensitivity or ambient temperature, may require or prevent the use of a low-cost linear regulator. Considering how the rails interact during startup is also critical for a robust system. How to choose the right converter and then design it for a multi-rail application is covered in Part 2 of this series.

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