

High-Performance Analog Products

Analog Applications Journal

Fourth Quarter, 2006



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Contents

Introduction	4
Data Acquisition	
Clamp function of high-speed ADC THS1041	5
The THS1041 clamp function enables it to generate and output a buffered dc voltage for a variety of ADC applications. This article presents test data related to dc stability when the clamp function and SE input configuration are applied at the same time. Included is an evaluation of how to obtain the best ac performance and maximum input range with the THS1041 when using the clamp function.	
Power Management	
A 3-A, 1.2-V_{OUT} linear regulator with 80% efficiency and $P_{LOST} < 1\text{ W}$	10
Using linear regulators for higher-current, low-output voltage applications has been a challenge for many years. The dual-input rail, low dropout voltage, controllable soft starting, tracking, and integrated PG features of the TPS74x01 family have made linear regulators more appealing. An evaluation of stability, transient response, soft starting and sequencing is included in this article.	
bq25012 single-chip, Li-ion charger and dc/dc converter for Bluetooth® headsets .	13
A typical Bluetooth headset needs a rechargeable battery, a battery charger, and a 1.8-V dc/dc converter to power the core chip. This article describes the capabilities of the bq25012, which has a fully integrated 500-mA, single-cell Li-ion battery charger with a high-efficiency, 1-MHz, synchronous switching step-down dc/dc converter.	
Fully integrated TPS6300x buck-boost converter extends Li-ion battery life	15
A standard buck or boost converter has limitations when a 3.3-V output is required from a single-cell Li-ion source. This article describes how the TPS6300x family excels in low-voltage portable applications when efficiency, cost, and small size are important.	
Interface (Data Transmission)	
Detection of RS-485 signal loss	18
Fault isolation and safety shutdown protocols are critical in many applications. This article shows how a differential window comparator can be constructed with the passive-failsafe feature of two SN65HVD3088E RS-485 transceivers and an AND gate.	
Index of Articles	20
TI Worldwide Technical Support	23

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as “how-to” instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Clamp function of high-speed ADC THS1041

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Introduction

The THS1041 from Texas Instruments (TI) is a 10-bit, 40-MSPS, CMOS high-speed analog-to-digital converter (ADC). It has many good features, including a single 3-V supply, low power, a flexible input configuration, a built-in programmable gain amplifier (PGA), and a built-in clamp function. Because of these features, especially the built-in clamp function, the THS1041 has been used in various applications for many years. The clamp function enables the device to generate and output a buffered dc voltage for flexible ADC applications—for example, to provide a common-mode voltage for the ADC or to allow dc restoration on an ac-coupled video signal at the ADC analog input. This function can be enabled or disabled. As shown in Figure 1, the THS1041 clamp function consists of an on-chip digital-to-analog converter (DAC), logic control, a clamp input, a buffer, and a clamp output. The clamp output can be a continuous or interrupted dc signal depending on whether its Clamp pin receives a dc or pulse signal from an external source. When this interrupted dc signal is applied to the ADC single-ended (SE) input circuit to provide common-mode voltage, the dc stability at the ADC analog input becomes a concern. Some users have questioned dc stability when the clamp function and SE input configuration are applied at the same time. This article presents some test data that explains how the dc voltage behaves in

this kind of application condition and how to get the best ADC performance when the clamp function is on.

Clamp function

Figure 1 shows that the THS1041 clamp function is implemented by setting four pins—Clampin, Clampout, Clamp, and Mode—as well as the device internal registers. With on-chip DAC, digital data from the THS1041 internal register written by data bus b0 to b9 can be converted into an analog dc voltage. This dc voltage is then buffered and output to Clampout through internal switches. The internal switch between the buffer and DAC can be on or off depending on how the register is set. The DAC can provide different dc voltages with a range between reference voltages REFT and REFB for different application needs. Setting different voltage levels at the Mode pin permits the input of the internal buffer to also simply be connected to an internal fixed dc voltage or to Clampin for an external dc voltage input. The Clampout pin can be connected to or disconnected from the buffer output of the clamp function by controlling either the dc or the pulse signal on the Clamp pin. The THS1041 clamp function can be on with an ADC differential input or SE input configuration. Its output from Clampout can be connected to both analog inputs, AIN+ and AIN-, to provide common-mode voltage, or to only one of them for other applications.

Figure 1. THS1041 clamp function block diagram

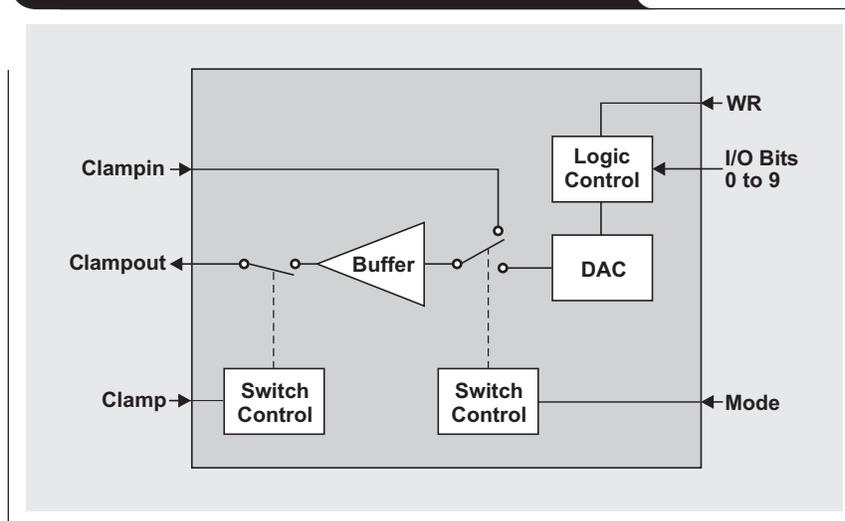


Figure 2 shows a fundamental configuration of the THS1041 with the clamp function at the SE input. Setting Mode as $AV_{DD}/2$ puts the device in an internal reference mode; and dc voltage at Clampout is from Clampin, not an internal DAC. The output of the clamp function, Clampout, is connected to AIN+ and also to a capacitor C2 through a small resistor R for a clamp pulse control application.¹ Capacitor C2 is used to hold dc voltage when Clampout is disconnected internally during the clamp pulse interval. It is also used to couple ac signals from the source to AIN+. Another ADC analog input, AIN-, is connected to an external dc source and should have the same dc voltage as AIN+ for normal operation. The Clamp pin controls the internal switch between Clampout and the buffer output. When Clamp is logic high, Clampout is internally connected to the buffer output; and when Clamp is logic low, Clampout is disconnected from the buffer output.

Testing dc behavior with clamp dc control

Clamp dc control means adding a dc signal at the Clamp pin to control the Clampout pin's access to the internal buffer. To see dc behavior at AIN+ and AIN- when the clamp function is on, two different dc voltages are added to AIN+ and AIN-, and the logic level at Clamp is controlled manually. Based on the configuration in Figure 2, V2 is set at 1.5 V at Clampin, V1 is set at 1 V at AIN-, C2 is 0.6 μ F, and R is 10 Ω . No ac signal is added to analog input AIN+ in this case. The ADC clock is running at 40 MHz. When Clamp is manually set to logic high (3 VDC), the AIN+ is stable at 1.5 V; and when Clamp is set to logic low (0 VDC), the AIN+ is stable at 1 V. In other words, when the Clamp pin is logic high, the voltage at AIN+ is driven by an internal buffer; and when the Clamp pin is logic low, AIN+ is disconnected from the buffer and its voltage drifts toward the voltage at AIN-. On the other hand, if AIN- is floating,

then the voltage at AIN- follows the voltage at AIN+. The dc voltages at AIN+ and AIN- drift toward each other after their voltage sources are disconnected. This is because significant charge or discharge occurs internally between the sampling capacitors in the ADC's sample-and-hold circuit during the hold phases after many clock cycles. The test data is shown in Tables 1 and 2.

The test data in Tables 1 and 2, measured when the ADC clock was active, shows that disconnecting the analog input pins from the source makes their dc voltages affect each other. When the ADC clock is not running, the dc

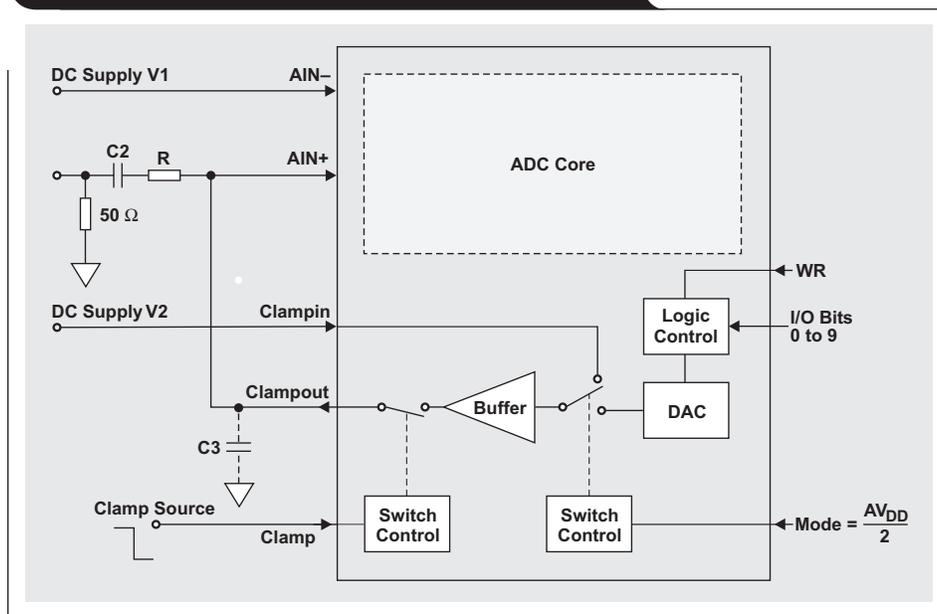
Table 1. Analog input dc voltage when clock is active and AIN- is connected to dc supply

Clamp Logic	Clampin (connected to dc supply) (V)	AIN- (connected to dc supply) (V)	AIN+ (charged or discharged based on Clamp logic) (V)
Low	1.5	1	1
High	1.5	1	1.5
Low	1.5	1	1

Table 2. Analog input dc voltage when clock is active and AIN- is floating

Clamp Logic	Clampin (connected to dc supply) (V)	AIN- (charged or discharged) (V)	AIN+ (charged or discharged based on Clamp logic) (V)
Low	1.5	0	0
High	1.5	1.5	1.5
Low	1.5	0	0

Figure 2. A clamp-mode configuration of THS1041



voltages at AIN+ and AIN– don't affect each other (see Tables 3 and 4). In addition, whether or not capacitor C2 is used does not affect the dc voltage test result but does affect the transition time of the voltage change at AIN+.

Table 3. Analog input dc voltage when clock is not active

Clamp Logic	Clampin (connected to dc supply) (V)	AIN– (connected to dc supply) (V)	AIN+ (charged or discharged based on Clamp logic) (V)
Low	1.5	1	0
High	1.5	1	1.5
Low	1.5	1	0*

*Discharge slowly

Table 4. Analog input dc voltage when clock is not active and AIN– is floating

Clamp Logic	Clampin (connected to dc supply) (V)	AIN– (charged or discharged) (V)	AIN+ (charged or discharged) (V)
Low	1.5	0	0
High	1.5	0	1.5
Low	1.5	0	0*

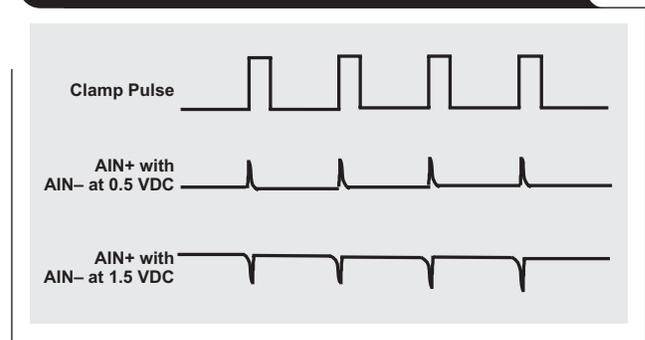
*Discharge slowly

Testing dc behavior with clamp pulse control

Clamp pulse control means adding a pulse signal at the Clamp pin to control the Clampout pin's access to the internal buffer. To observe dc behavior at the THS1041 analog input, a pulse signal instead of a dc signal is added to the Clamp pin with a frequency of 16 kHz and a duty cycle of 6% (see Figure 2). Similar to the previous test, a fixed dc voltage of 1 V from a well decoupled supply is added to Clampin, and a variable dc voltage is added to AIN–. In this case, AIN+ is driven to 1 V by the internal buffer during the clamp pulse and is well maintained at that level by capacitor C2 during the clamp pulse interval when AIN– is 1 V. The capacitance C2 must be large enough and the clamp pulse interval short enough to keep the dc voltage at AIN+ the same level as the dc voltage at Clampin.¹ However, the dc signal will be distorted if the dc offset at AIN– is set differently from AIN+. As mentioned earlier, the dc voltages at the analog input pins can drift when one pin or the other is floating. The test with clamp pulse control further proves this statement. The dc drift appears as a voltage spike when a pulse is applied to the Clamp pin, and this is observed by oscilloscope as shown in Figure 3.

The spike periodically appears at AIN+ at clamp pulse frequency, and its amplitude increases as the dc voltage difference between the analog input pins increases. The test data shows that when Clampin is connected to a 1-V

Figure 3. Spikes can appear at AIN+ with dc voltage on AIN–



supply and AIN– is connected to a 0.5-V supply, the dc measurement at AIN+ is 1 V during the clamp pulse logic high and low. The ac measurement at AIN+ is a positive spike at about 20 mV and appears when the clamp pulse transitions from low to high. When AIN– is connected to a 1.5-V supply and Clampin is still connected to a 1-V supply, the dc measurement at AIN+ is 1 V. The ac measurement at AIN+ is a negative spike at about 30 mV and appears when the clamp pulse transitions from low to high. When AIN– is connected to a 1-V supply, the same as the dc voltage at AIN+, the spike disappears and the 1-V dc voltage at AIN+ is smooth and stable.

Further testing shows that the spike gets smaller when the duty cycle of the clamp pulse goes higher. Adding a capacitor C3 at the Clampout pin will significantly limit the spike.

THS1041 ac performance with clamp pulse control

The spike at analog input AIN+ can degrade the ac performance of the THS1041 (see Figures 4 and 5 and Table 5). Figures 4 and 5 are FFT plots of the THS1041 with clamp pulse control and different dc voltage conditions on the analog input pins. The FFT plots are generated from a Labview FFT program based on the data captured from the THS1041 EVM by an HP1600 logic analyzer. The test signal at the analog input of the EVM is a 2.2-MHz sine wave with an amplitude of –20 dBFS (20 dB below the ADC's full scale). It is generated from an HP8644 sine-wave generator and received by the SE input of the THS1041 through an onboard transformer. (Detailed settings of the EVM board for this test are described later in this article.) A pulse generator triggered by the HP8644 is running the THS1041 input clock at 40 MHz. The clamp pulse is generated from a pulse generator with a frequency of 15.6 kHz and a 50% duty cycle.

In time domain the spike appears periodically at clamp pulse frequency as shown in Figure 3. In frequency domain the spike appears at 15.6 kHz (the low end of the frequency axis) on the FFT. When the dc voltage difference at the analog input pins is 0.5 V (AIN+ is 1 V and AIN– is 0.5 V), the spike at 15.6 kHz is –67 dBFS, the largest spike in the

FFT (see Figure 4). This spike is much higher than any harmonic on the FFT and contributes to the spurious-free dynamic range (SFDR) with a low value. When the dc voltage difference is zero (AIN+ and AIN- are 1 V), the spike at the same frequency is -82 dBFS, a 15-dB improvement (see Figure 5). This spike is lower than the

second and third harmonics and lower than the total harmonic distortion (THD).

Figures 4 and 5 show that with the dc voltage difference between AIN+ and AIN- increasing to a certain degree, the SFDR decreases and could be significantly worse than the THD if the input analog signal was small. This would

Figure 4. FFT of THS1041 in clamp mode with 0.5-VDC difference between analog input pins

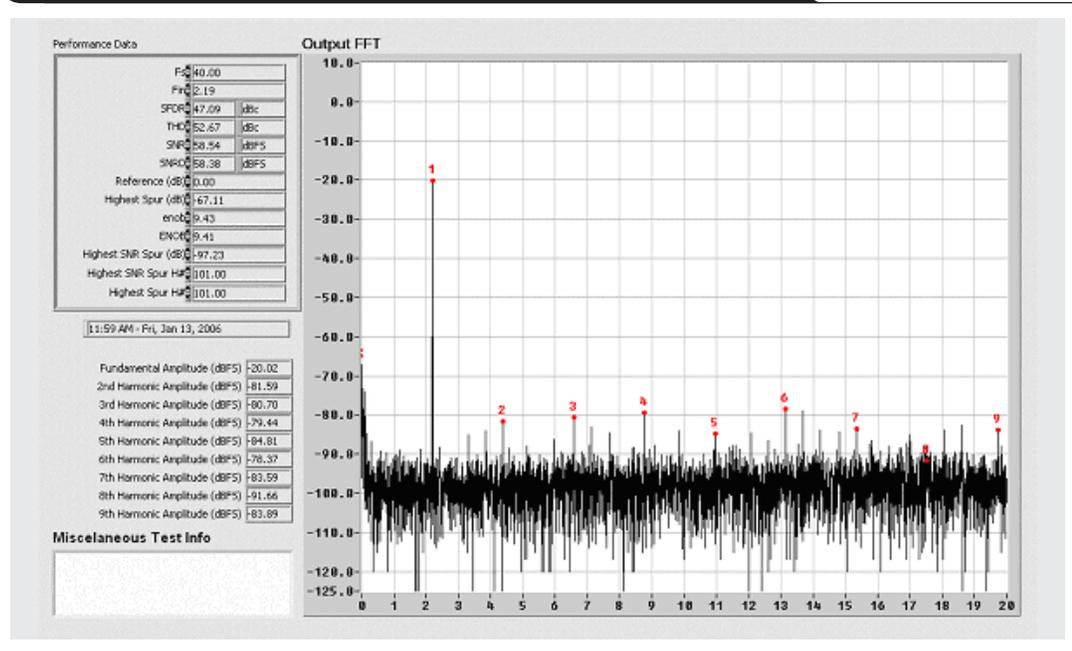
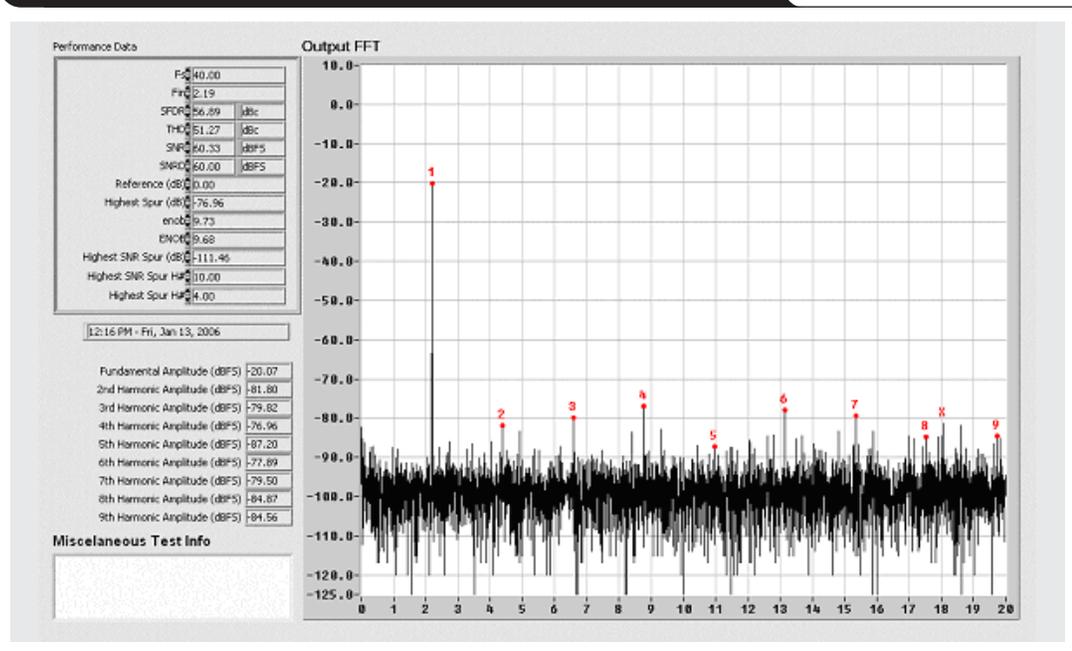


Figure 5. FFT of THS1041 in clamp mode with 0-VDC difference between analog input pins



be especially true if the decoupling capacitance C3 at Clampout (see Figure 2) was not large enough. Based on these test results, a further test was conducted with a different decoupling capacitance at Clampout. With an analog input amplitude of -21 dBFS (21 dB below the 2-V full-scale input of the THS1041), a C3 value of $0.4 \mu\text{F}$, and a dc voltage difference between AIN+ and AIN– of 0.5 V, the SFDR is about 16 dB worse than the THD. At the same value of C3, the SFDR is 3 dB worse than the THD when the dc voltage difference between AIN+ and AIN– is decreased to 0 V. If C3 is increased to $1.4 \mu\text{F}$, the overall ac performance—including the SFDR, THD, and signal-to-noise ratio (SNR)—improves significantly. In this case the SFDR is about 5 dB better than the THD when the dc voltage difference between AIN+ and AIN– is zero, and about 6 dB worse than the THD when the dc voltage difference is 0.5 V. The test data is shown in Table 5.

Table 5. THS1041 ac performance with different C3 values and different dc voltages at AIN– (clamp pulse is on and analog input is -21 dBFS)

AIN+ (V)	AIN– (V)	SFDR Relative to THD (C3 = $0.4 \mu\text{F}$) (dB)	SFDR Relative to THD (C3 = $1.4 \mu\text{F}$) (dB)
1	0.5	–16	–6
1	1	–3	5
1	1.5	–17	–5

The test data shows that the dc voltage differences between AIN+ and AIN– cause not only a spike at the analog input but also early output saturation, therefore decreasing the maximum analog input amplitude. For example, when the dc voltage difference between AIN+ and AIN– is 0.5 V with AIN+ at 1 V, the maximum analog input amplitude has to be 20 dB below full scale to avoid output saturation. When the dc voltage difference is 0.3 V with AIN+ at 1 V, the maximum analog input amplitude is 3.5 dB below full scale. So the dc voltage at AIN+ and AIN– should be the same in order to maintain the best ac performance and the specified maximum input amplitude.

The test data also shows that with the loss of maximum analog input amplitude, the THS1041 seems able to tolerate small dc voltage differences between AIN+ and AIN– to maintain the specified ac performance (see Table 6). In this test, the analog input sine wave is 2.2 MHz with 1.4 V peak to peak, 3.5 dB below the full scale of the THS1041. The sampling rate is 40 MHz, the clamp pulse is 16 kHz with a 6% duty cycle, and the dc voltage difference at the analog

Table 6. THS1041 ac performance with SE input, clamp pulse control, and dc voltage difference of 0.3 V at analog input

AIN+ dc Voltage (V)	AIN– dc Voltage (V)	SNR (dBFS)	SFDR (dBc)	THD (dBc)	Input Amp (dBFS)
1	0.7	59	70	64	–3.5

input is 0.3 V (AIN+ is 1 V and AIN– is 0.7 V). In this case, the ac performance is still within the specification, with SNR at 59 dBFS, SFDR at 70 dBc, and THD at 64 dBc.

Test setup conditions

This ac performance test was based on the THS1041 EVM board. The EVM schematic is shown in Reference 2. The basic SE configuration of the EVM is similar to that of Figure 2. C2 is $0.6 \mu\text{F}$, C3 is $1.4 \mu\text{F}$, and the dc source at AIN– is well decoupled from a 3.3-V supply. On the EVM board, pin 1 of T1 (transformer) is open for SE input, and J2 is the analog input. The jumpers for pins 1 to 2 are on at W1 and W2, the jumper for pins 1 to 2 is off at SJP6, and the jumpers for pins 1 to 2 are on at SJP2 and SJP1.

Conclusion

To maintain the maximum input range and best ac performance of the THS1041, the common-mode voltages added to analog inputs AIN+ and AIN– should meet the requirement in the datasheet, and the dc voltage added to AIN– should be the same as the dc voltage at AIN+ with an SE input configuration. Adding different dc voltages to AIN+ and AIN– can cause a spike at the analog input when the clamp function is on and a pulse signal is applied to Clamp. The higher the dc voltage difference between analog inputs AIN+ and AIN–, the larger the spike. The spike also gets worse if the duty cycle of the clamp pulse is decreased. This is because the dc voltages at AIN+ and AIN– drift toward each other after their external voltage sources are disconnected. In this case the charge or discharge occurs internally between the sampling capacitors in the ADC's sample-and-hold circuit during the hold phases. The dc voltage difference between AIN+ and AIN– also causes early output saturation and degrades the maximum analog input amplitude, so the difference should be limited. Increasing decoupling capacitance at Clampout will minimize the spike, increase dc voltage difference tolerance at the analog input, and improve overall THS1041 ac performance. This conclusion is based on the THS1041 bench test. The observation and test method in this article are also helpful for other high-speed ADCs.

References

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A 3-A, 1.2-V_{OUT} linear regulator with 80% efficiency and P_{LOST} < 1 W

By Jeff Falin (Email: j-falin1@ti.com)

HPA Portable Power Applications

Introduction

Using linear regulators for higher-current (>1-A), low-output voltage applications has been a challenge for many years due to the regulator's dropout requirements, related inefficiency, cumbersome output capacitor requirements for stability, and large inrush currents at startup. The Texas Instruments (TI) dual input rail TPS74x01 solves these problems.

Linear regulator topology review

The primary drawback of linear regulators for higher-current applications is their low efficiency, computed as V_{OUT}/V_{IN} . The power lost (P_{LOST}) in a linear regulator, computed as

$$1 - \frac{V_{OUT}}{V_{IN}} \times P_{IN} = (V_{IN} - V_{OUT}) \times I_{OUT},$$

must be dissipated by its package. The TO-263 or D2PAK package is the largest surface-mount package in which linear regulators are available. Without additional airflow, its maximum power dissipation capability is approximately 2.75 W (assuming it is soldered to a large copper plane for heat sinking). Many higher-current, "low-dropout" linear regulators with PMOS pass elements have minimum input voltages of 2.5 to 2.7 V, not only to power the internal

LDO drive circuitry but also to drive the PMOS FET hard enough to provide higher output currents.

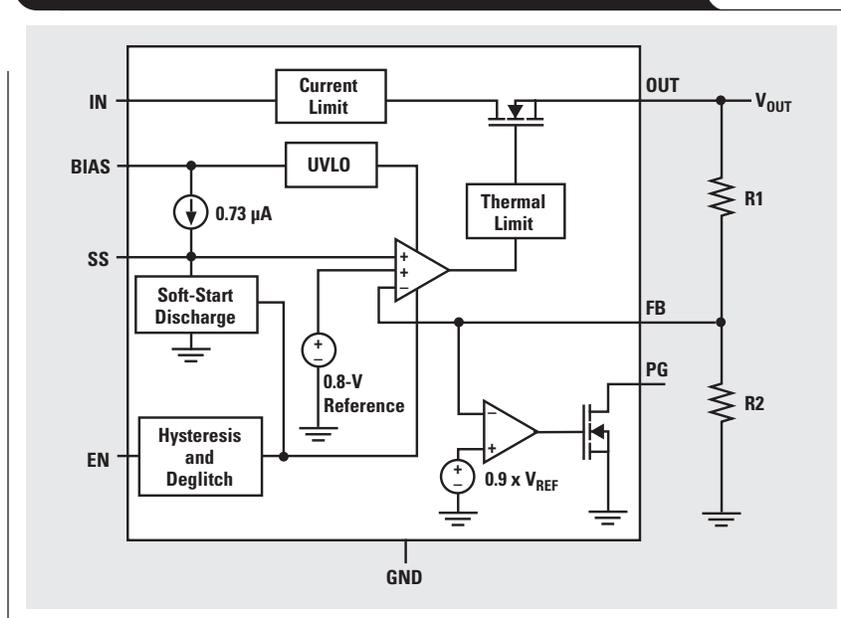
Therefore, using many PMOS-pass-element-based linear regulators for output voltages below 1.8 V and output currents above 2.5 A is cumbersome and costly due to the additional airflow and/or external heat sinking required to dissipate the heat generated by the regulator.

Since NMOS FETs have inherently lower $r_{DS(on)}$ than similarly current-rated PMOS FETs, an NMOS FET pass element needs less $V_{IN} - V_{OUT}$ drop to provide the same current. However, the source-follower configuration of the NMOS-based regulator requires that the gate of the FET be at least a threshold voltage drop (typically 1 V) above the output voltage. The regulator needs either an internal charge pump to provide a higher gate-drive voltage or, more simply, a second low-power input rail from an existing 5-V or 3.3-V bias supply. This is the reasoning behind the development of the dual-rail, NMOS-pass-element-based TPS74x01 family of linear regulators.

Dropout

As shown in Figure 1, the TPS74x01 regulators have two input voltages, one providing the low-current bias voltage to power the internal circuitry that controls the NMOS pass device and one as a second power input. Since all the

Figure 1. Block diagram of the TPS74201 and TPS74401 linear regulators



internal circuits run off the higher BIAS input, the device is capable of achieving regulation from a low-voltage input supply. In fact, the power input, IN, is limited only by the output voltage and dropout of the device.

There are two different specifications for dropout voltage with the TPS74x01. The first is referred to as V_{IN} dropout and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62 V above V_{OUT} . Such an application might be a low-ripple, 1.2-V, 3-A power rail for an FPGA transceiver where V_{IN} and V_{BIAS} are provided by 1.5-V and 3.3-V switching supplies, respectively. In this configuration, the 3 × 3-mm QFN package, which is capable of dissipating 1.9 W at 55°C, needs to dissipate only

$$(1.5 \text{ V} - 1.2 \text{ V}) \times 3 \text{ A} = 0.9 \text{ W},$$

thereby achieving 1.2 V/1.5 V = 80% efficiency.

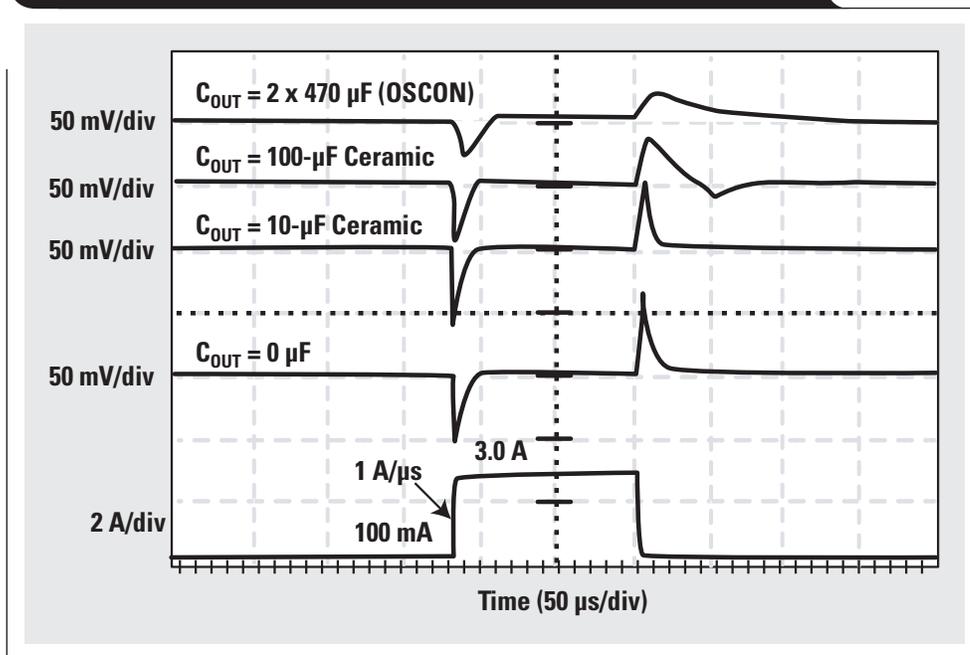
The second specification is referred to as V_{BIAS} dropout and is for users who wish to tie the IN and BIAS pins together. This allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be 1.4 V above V_{OUT} . For example, the TPS74201 can provide a 3.3-V, 1.0-A soft-starting supply (discussed later) from a 5-V rail with 3.3 V/5 V = 66% efficiency and can dissipate

$$(5 \text{ V} - 3.3 \text{ V}) \times 1.0 \text{ A} = 1.7 \text{ W}.$$

Stability and transient response

Until recently, linear regulator loop stability presented a challenge to analog IC designers because one of the control-loop poles, created by the output capacitor and the impedance at the load, varies in frequency location based on the output current. Regulators with the NMOS pass element in source-follower configuration have always been slightly easier to compensate because their output impedances are lower than similarly rated PMOS regulators in common-source configurations. This means that the NMOS regulator's moving pole is higher in frequency than the comparably rated PMOS counterpart and so is further away from the internal error amplifier's pole(s). Older methods of ensuring stability were either to roll off the control-loop response at low frequency, thereby killing transient response, or to counteract the moving pole with a zero created by an output capacitor with a certain amount of equivalent series

Figure 2. Load transient response with various output capacitors



resistance (ESR). Using a patented feedback control topology, the TPS74x01 family, configured with $V_{BIAS} = 3.3 \text{ V}$, $V_{IN} = 1.8 \text{ V}$ and $V_{OUT} = 1.5 \text{ V}$, achieves fast transient response times (see Figure 2) with no output capacitors but is still stable with larger capacitors having ESR. The absence of output voltage ringing after the load transient shows that the regulator is very stable with no output capacitance.

Since the TPS74x01 family is stable with no output capacitor but has such fast transient response, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of many FPGAs and DSPs. This reduces total solution cost by eliminating the need to have multiple bulk capacitors for the power rail.

Soft start and sequencing

Many older linear regulators start up fast because the feedback loop senses the low output voltage and turns on the pass FET hard. For some applications, fast startup is required; however, such fast turn-on causes large inrush currents, up to the current-limit rating of the device, to charge output capacitors. These large currents may pull down the input power bus and cause system-level problems. To achieve a linear and monotonic soft start that reduces peak inrush current during startup and minimizes startup transients seen by the input power bus, the TPS74201 and TPS74401 error amplifiers track the voltage ramp of the external soft-start capacitor until its voltage exceeds the internal reference. The soft-start ramp time is dependent on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}). It can be calculated with

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}}$$

Note that since the soft start is voltage-controlled, the startup is not dependent on the output load.

Instead of an SS pin, the TPS74301 version has a TRACK pin. As summarized in Figure 3, with the center tap of a resistor divider from an external supply connected to TRACK, the TPS74301's output voltage will track the external supply until the TRACK voltage reaches 0.8 V. This feature can be used to implement simultaneous or ratiometric sequencing. It is useful for minimizing the stress on ESD structures that are present between the Core and I/O power pins of many processors and/or for managing integrated power-on reset circuitry. All members of the TPS74x01 family facilitate implementation of sequential sequencing by tying the integrated PG signal to the EN pin of a following supply.

Conclusion

With a dual input rail and low dropout voltage, the TPS74x01 family has made linear regulators more appealing than switching regulators, reducing board size and cost and providing comparable efficiency for powering many lower-voltage, higher-output-current power rails. The family's additional features—including controllable soft starting, tracking, and integrated PG—manage start-up problems that have plagued linear regulators in the past. Add in

the fast transient response, which minimizes the total number of output capacitors, and you have a nearly ideal dc/dc converter.

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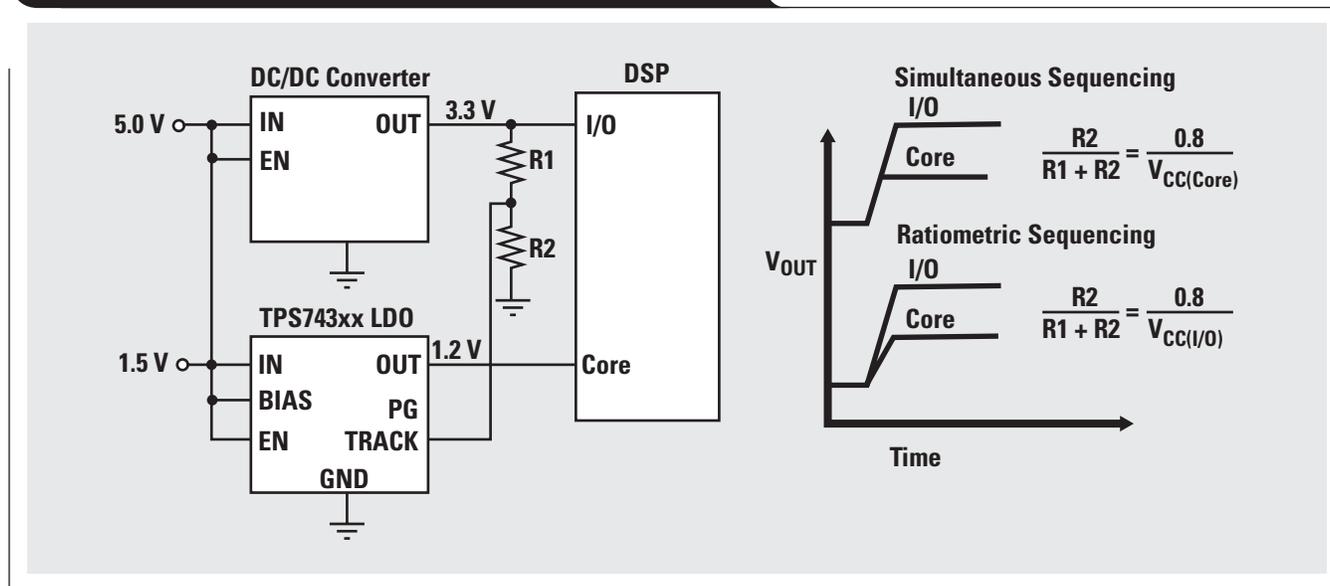
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace "litnumber" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "1.5-A LDO with Programmable Soft-Start," TPS74201 Datasheetsbvs064
2. "1.5A Ultra-Low Dropout Linear Regulator with Programmable Sequencing," TPS74301 Datasheetsbvs065
3. "3.0A Ultra-Low Dropout Linear Regulator," TPS74401 Datasheetsbvs066

Related Web sites

power.ti.com
www.ti.com/sc/device/partnumber
 Replace *partnumber* with TPS74201, TPS74301, or TPS74401

Figure 3. Various sequencing methods using the TRACK pin



bq25012 single-chip, Li-ion charger and dc/dc converter for Bluetooth® headsets

By **Lingyin Zhao** (Email: lzhaot@ti.com)

Application Engineer, Portable Power Management

Introduction

Highly integrated charger and dc/dc converter ICs have become more and more desirable as portable power management technology continues to advance. These ICs not only support size reduction of portable devices but also incorporate more functionality and enhance performance in diagnostics, monitoring, control, and protection.

As an example, a typical Bluetooth headset needs a rechargeable battery (and thus a battery charger) and a 1.8-V dc/dc converter to power the core chip. With small size, light weight, and low cost being the major concerns, the bq25012 is an ideal solution for this application. A single-chip 3.5 × 4.5-mm QFN package incorporates a linear charger with dual inputs for both the ac adapter and the USB, and a dc/dc converter with integrated FETs saves board space and reduces system design time. Figure 1 shows a typical application circuit with a 1.8-V, 100-mA power converter and a 500-mA linear battery charger using the bq25012.

Single-cell, Li-ion battery charger

The bq25012 offers an integrated power MOSFET and charge controller with programmable charge current up to 500 mA for single-cell, Li-ion battery applications. It

charges the battery and powers the system from either the ac adapter or the USB with autonomous power-source selection. When the V_{CC} supply is removed, the bq2501x automatically enters sleep mode with reverse blocking protection to extend the battery runtime.

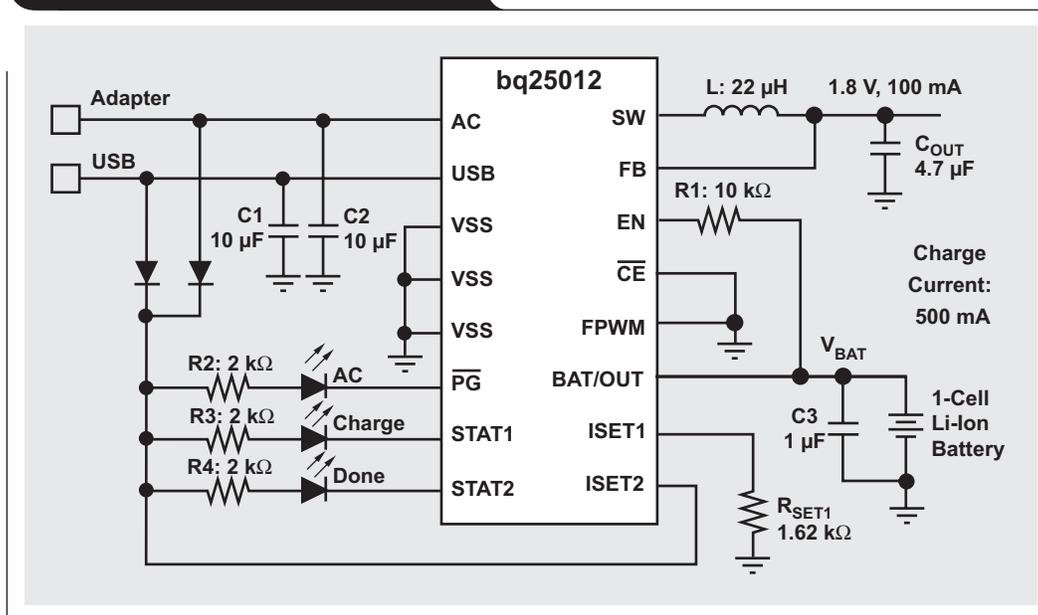
The bq25012 charges the battery in three phases with high-accuracy current and voltage regulation: precharge, constant current, and constant voltage. Charging is terminated based on minimum current. An internal charge timer provides an additional safety feature for charge termination. The bq2501x automatically recharges the battery if the battery voltage falls below an internal voltage threshold, which is 100 mV below the voltage regulation point.

The STAT1 and STAT2 open-drain outputs indicate various charger and battery conditions, while the \overline{PG} pin indicates whether the ac adapter is present. The digital input (\overline{CE}) is used to enable and disable the charging process.

High-efficiency dc/dc converter

The high-efficiency, synchronous switching dc/dc converter with integrated power MOSFETs is capable of supplying up to 150 mA. The bq25012 has fixed dc/dc converter output voltage at 1.8 V, while the bq25010 has adjustable output voltage from 0.7 to 4.2 V. They use the battery voltage, V_{BAT} , as their input. The synchronous pulse width modulation (PWM)

Figure 1. bq25012 application circuit



controller operates at 1 MHz, minimizing the size of the filter inductor and capacitor. The undervoltage lockout circuit prevents the converter from turning on the switch or rectifier MOSFET at low input voltages or under undefined conditions.

During PWM operation, the converter uses a unique, fast-response voltage-mode-controller scheme with input voltage feedforward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. As the load current decreases, the converter enters power-save, or pulse frequency modulation (PFM), mode. In this mode the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. However, in cases when PFM is not desirable, driving the forced PWM pin high overrides power-save mode and forces the dc/dc converter to remain in the PWM mode.

Figure 2 shows measured dc/dc converter efficiency when the bq25012 EVM is used.

Design example

Requirements

Adapter voltage: 5 V

Battery pack: Single Li-ion, 1800 mAh

Battery regulation voltage: 4.2 V

Fast-charge current: 500 mA

Precharge and termination current: 50 mA

dc/dc converter output voltage: 1.8 V/100 mA

Determine the inductor L

Given 40% ripple current, the inductance when

$V_{IN} = V_{BAT_max}$ and $V_{IN} = V_{BAT_min}$ is

$$L = \frac{V_{BAT_max} - V_{OUT}}{\Delta I_L} \times \frac{V_{OUT}}{V_{BAT_max}} \times \frac{1}{f_S} = 25.7 \mu\text{H}.$$

Select $L = 22 \mu\text{H}$.

The inductor saturation current should be larger than the peak current to prevent inductor saturation. Select the Taiyo Yuden LBC2016T220M inductor (22 μH , 165 mA, 0806).

Determine the output capacitor C_{OUT}

To achieve optimum loop stability, the resonant frequency f_0 , composed of the inductor and output capacitor of the dc/dc converter, is approximately 16 kHz.

$$C_{OUT} = \frac{1}{(2\pi f_0)^2 L} = 4.5 \times 10^{-6} \text{ (farads)}$$

Select a 4.7- μF , 6.3-V, 0603 ceramic capacitor.

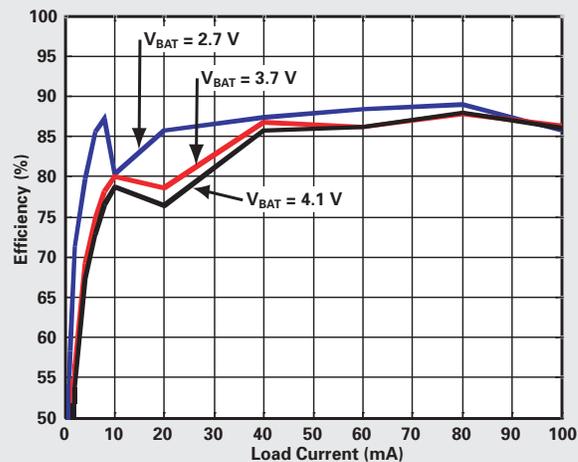
Determine current setting resistor R_{SET1}

With $V_{SET} = 2.5 \text{ V}$ and $K_{SET} = 320 \text{ V/A}$,

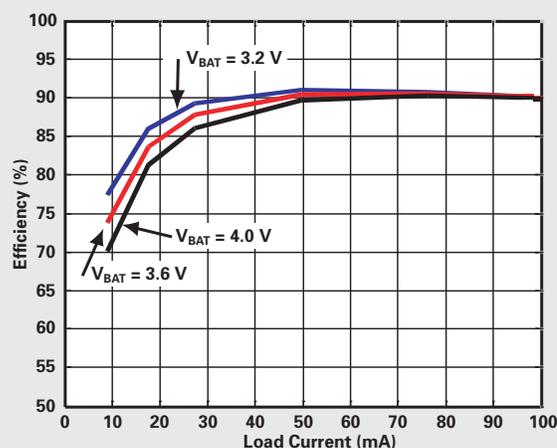
$$R_{SET1} = \frac{V_{SET} K_{SET}}{I_{Fast-charge}} = \frac{2.5 \times 320}{0.5} = 1.6 \text{ k}\Omega.$$

Select 1%, 1.62-k Ω resistors.

Figure 2. Efficiency vs. I_{OUT}



(a) Power-save mode ($V_{OUT} = 1.8 \text{ V}$, $T = 27^\circ\text{C}$)



(b) Forced PWM ($V_{OUT} = 1.8 \text{ V}$, $T = 22^\circ\text{C}$)

Determine USB charge current

The ISET2 pin determines the charge current for the USB port (high = 500 mA, low = 100 mA, high-Z = disable USB charge).

Conclusion

The bq25012 fully integrates a single-cell Li-ion battery linear charger up to 500 mA and a high-efficiency, 1-MHz, synchronous switching step-down dc/dc converter. The small size, high efficiency, and easy design make this a simple and versatile IC to use for many portable power applications such as Bluetooth headsets and MP3 players.

Related Web sites

power.ti.com

www.ti.com/sc/device/bq25010

www.ti.com/sc/device/bq25012

Fully integrated TPS6300x buck-boost converter extends Li-ion battery life

By Bill Johns (Email: w-johns2@ti.com)

HPA Portable Power Applications

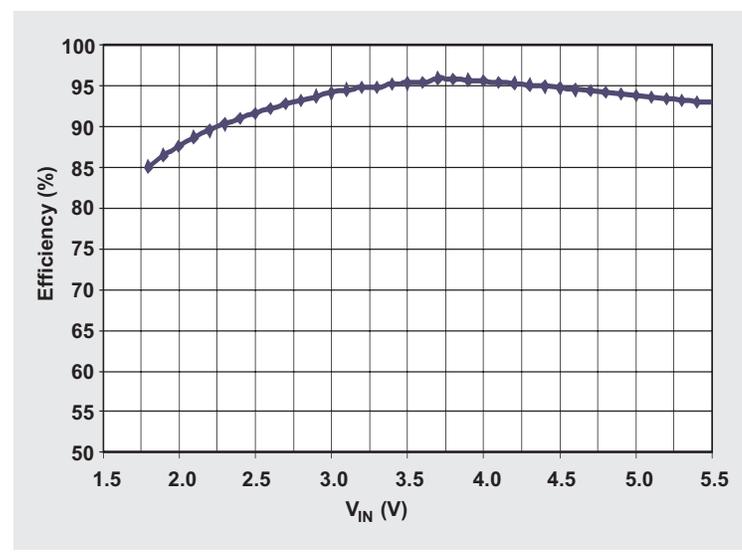
Introduction

For portable power applications to take advantage of the small size and high energy density of modern battery technology, they must operate efficiently over the full battery-discharge voltage range. This presents a design challenge for Li-ion-powered systems requiring a 3.3-V bus. While standard buck converters excel at efficiently converting a 4.2- to 3.0-V Li-ion battery to lower output voltages such as 1.8 V, and standard boost converters efficiently convert a Li-ion battery to higher output voltages such as 5 V, neither provides an optimal solution for generating the ever-present 3.3-V bus. Topologies such as the SEPIC and traditional buck-boost utilize the full battery capacity but suffer from drawbacks such as low efficiency, high cost, increased board area, and high part count. The TPS6300x, available in three configurations, can solve many of these problems. The TPS63000 has an adjustable output from 1.2 V to 5.5 V. The TPS63001 and TPS63002 outputs are fixed at 3.3 V and 5.0 V, respectively. All are available in the space-saving 10-pin QFN (DRC) package.

TPS63001

The Texas Instruments TPS63001 efficiently converts the Li-ion input to a 3.3-V bus with minimized part count, small board area, and reduced cost. It integrates both

Figure 1. TPS63001 efficiency at 1.8 to 5.5 V with 320-mA load ($V_{OUT} = 3.3$ V)

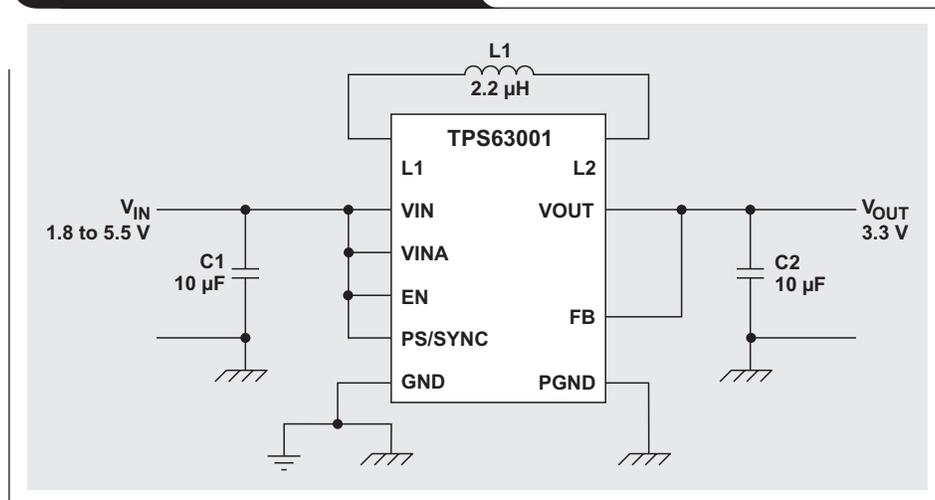


buck and boost functions into a single 3×3 -mm QFN package, including switching FETs, compensation, and protection features. Only three external parts are required for operation: input and output capacitors and an inductor. The converter operates with a peak efficiency of 96% (see Figure 1). With a peak output current of 800 mA, it delivers

enough current to power most portable loads. A wide input voltage range of 1.8 to 5.5 V allows operation with many popular power sources such as dual- and triple-cell alkaline and NiMH batteries as well as 3.3- and 5-V buses.

Figure 2 shows a typical 3.3-V supply that could be powered by a single Li-ion battery. A switching frequency of 1.5 MHz allows the use of a small 2.2- μ H inductor and small 0603-sized ceramic input and output capacitors. High efficiency combined with a low

Figure 2. Typical application circuit



external part count reduces the total solution size to only 6 × 6 mm (see Figure 3).

Advanced control topology maximizes efficiency

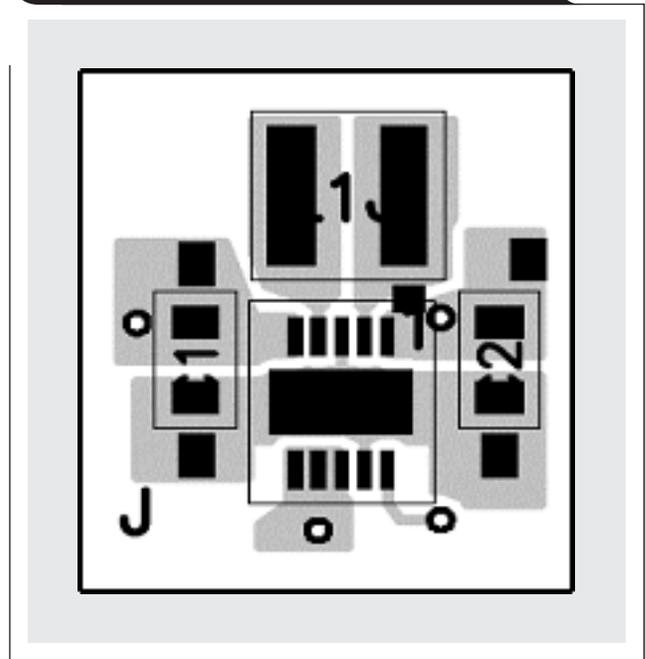
The TPS6300x is based on the standard H-bridge buck-boost power stage shown in Figure 4. It contains both buck and boost switching-FETs configurations that are connected to a single inductor. Unlike a standard buck-boost mode that continuously switches all four FETs simultaneously, the TPS6300x utilizes a proprietary modulator design that switches only two FETs at a time. This control scheme significantly reduces unnecessary switching losses. The TPS6300x also reduces power loss by operating in the more efficient buck or boost mode rather than the traditional buck-boost mode.

As the Li-ion battery discharges down to and below 3.3 V, a buck-boost converter must transition from buck mode to boost mode. Many buck-boost control schemes exhibit efficiency drops, power-supply jitter, or unstable output voltage at this transition point. The TPS6300x transitions seamlessly between buck and boost modes on a pulse-by-pulse basis as necessary. This provides constant PWM switching over the buck and boost range with no overlap or dead time between the two modes.

Additional features

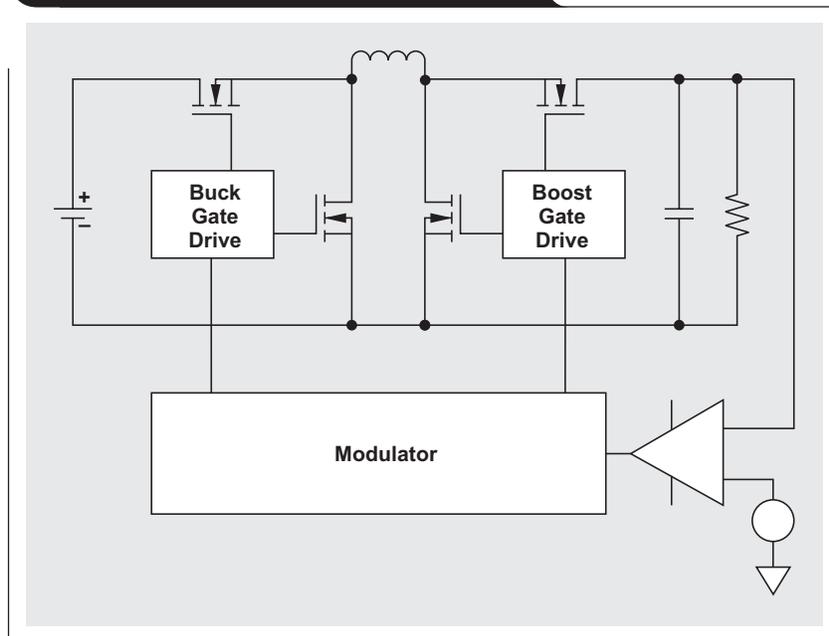
The TPS6300x contains additional integrated features that enhance its usability in portable applications that have, for example, an extremely low quiescent current (less than 50 μA), a user-selectable power-save (PS) mode that maintains efficiency at light loads, or external synchronization to help minimize system noise.

Figure 3. Typical layout in a 6 × 6-mm area



Average-current-mode control topology provides fast transient response and low output ripple in both buck and boost modes. Output regulation tolerance is ±1% over the input and load ranges. Internal compensation is optimized for an external inductor of 2.2 to 4.7 μH with an output capacitor between 10 and 22 μF.

Figure 4. Block diagram of power section



Short-circuit protection provides a foldback current limit that reduces the output current limit from its maximum value of 1.7 A to 800 mA when the output voltage falls by 3%.

This reduces power dissipation on the device during an output overload condition. When the overload has cleared, normal operation resumes. One advantage of this approach is the ability to charge large-output capacitors such as super capacitors.

PS-mode features maintain very high efficiency, even at light loads below 300 mA. In the PS mode, switching occurs only long enough to raise the output voltage slightly above the output-voltage set point. Switching then stops until the output voltage falls below the set point again. This “on then off” switching provides excellent efficiency at light loads.

Other applications

The TPS6300x also operates in a current-regulation mode to drive a white-light-emitting diode (WLED). This is accomplished by replacing the output voltage divider network

with a resistor in the return path of the WLED. Since the typical forward voltage drop of a WLED is 4.2 to 3.5 V, powering it from a Li-ion cell presents a problem to most power-supply topologies because the supply is required to both buck and boost its output voltage. The TPS6300x's buck-boost functionality solves this problem and easily delivers 500 mA of current for a torch or flash application.

Conclusion

The TPS6300x is an ideal solution for converting a Li-ion battery to a 3.3-V bus. Its features such as high efficiency, small board area, low cost, and seamless transition from buck mode to boost mode make it an easy choice for the design engineer needing a high-performance design with quick turnaround.

Related Web sites

power.ti.com

www.ti.com/sc/device/TPS63000

Detection of RS-485 signal loss

By Kevin Gingerich (Email: k-gingerich@ti.com)

High-Performance Linear/Interface

Introduction

Fault isolation and safety shutdown protocols are critical in many industrial, telecommunication, automotive, and data processing systems. While built-in test routines may provide fault isolation when the system is offline, real-time fault detection requires continuous monitoring of signals. These systems often use RS-485 to share data between sensors, actuators, single-board computers, or communication processors.

RS-485 signals are differential, using two signal wires to transmit data, and detection of valid signal levels requires a differential window comparator. Designing this circuit function is complicated by the wide common-mode range of RS-485 signals and, in many cases, the availability of only positive supply rails.

This article shows how a differential window comparator can be constructed with the passive-failsafe feature* of two SN65HVD3088E RS-485 transceivers and an AND

*See Reference 1 for more on this feature.

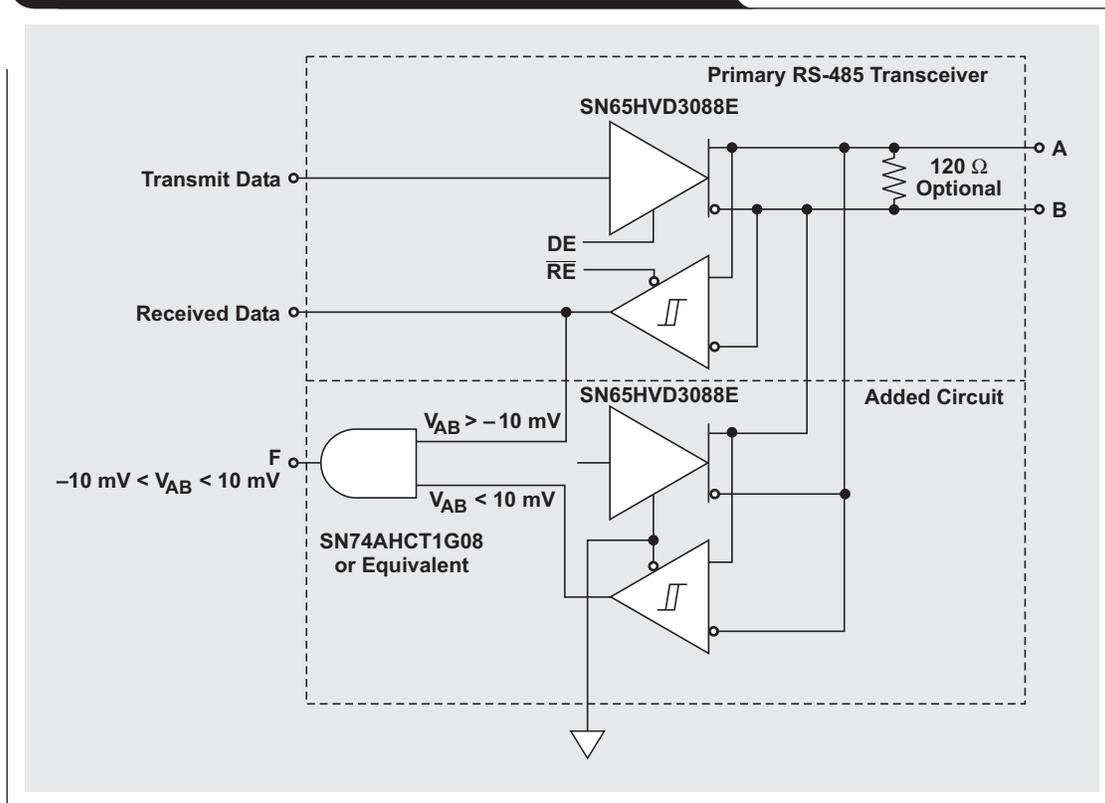
gate. It also provides theory of operation, the basic circuit schematic, test results, and other design considerations.

Theory of operation

The differential input threshold is the voltage between the non-inverting and inverting RS-485 signals above which the bus state is high and below which the bus state is low. The differential input voltage threshold of standard receivers is between -200 mV and 200 mV . The differential input voltage threshold of the SN65HVD3088E is between -200 mV and -10 mV . This gives a known (high-level) receiver output state with zero volts (no input signal) and is called *passive failsafe*. It does not distinguish between a valid high input and no signal.

A single SN65HVD3088E can determine if the differential input voltage is less than -200 mV or above -10 mV . Reversing the input polarity of a second SN65HVD3088E can determine if the differential input voltage is below 10 mV or above 200 mV and is the basis for constructing the differential window comparator shown in Figure 1.

Figure 1. RS-485 transceiver with loss-of-signal indicator



The upper-receiver output in Figure 1 is true (high) if the differential input voltage, V_{AB} , is greater than -10 mV. Since the inputs of the lower receiver are reversed, the output is true (high) if $-V_{AB} > -10$ mV or, dividing both sides of the inequality by negative one, $V_{AB} < 10$ mV. If both receiver outputs are true, then the differential bus voltage is between -10 mV and 10 mV and is not a valid input. This fault is indicated by the AND gate F output using inputs of the two receiver outputs.

Test results

Figures 2 and 3 show the F and V_{AB} low-to-no and high-to-no signal transitions and the desired fault indication.

Figure 2. Loss of valid low-level signal

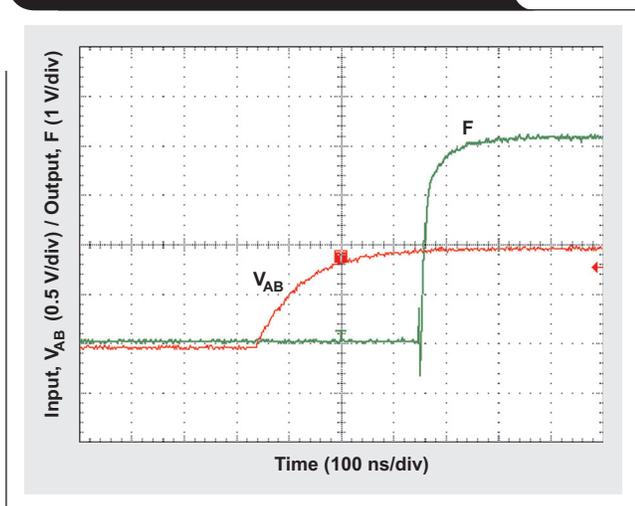
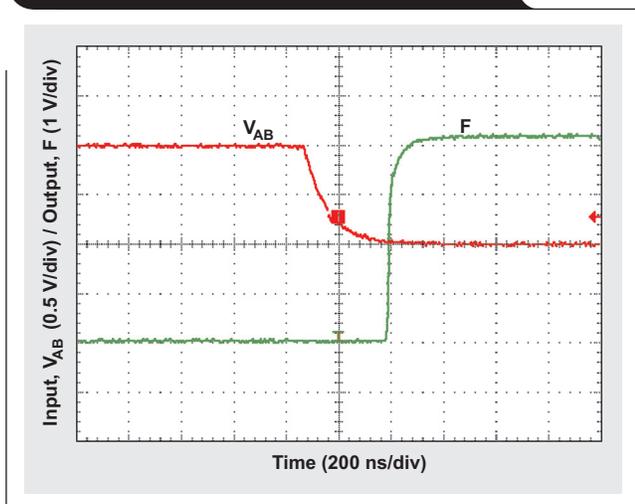


Figure 3. Loss of valid high-level signal



Other design considerations

While this example circuit uses the SN65HVD3088E, any RS-485 receiver with the passive failsafe feature may be used (Texas Instruments offers over thirty such products). A similar approach may be applied to unidirectional (simplex) connections. The parallel connection of the two transceivers will halve the unit loading and double the stray capacitance presented to the bus. This may limit the number and spacing of devices on a bus segment (see References 2 and 3).

If the system timing budget allows, filtering of F may prevent false fault indications from differential noise or from very slowly changing input signals. Filtering may be done by adding gating or by choosing a very slow AND gate.

Conclusion

A differential window comparator can be constructed by adding a passive-failsafe RS-485 receiver and one AND gate to another passive-failsafe receiver. The circuit then provides a loss-of-signal indication from an RS-485 data bus. This fault flag may then be used for system fault isolation or safety shutdown protocols.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace "litnumber" with the **TI Lit. #** for the materials listed below.

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1. Kevin Gingerich, "Failsafe in RS-485 data buses," <i>Analog Applications Journal</i> (3Q 2004)	slyt080
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Index of Articles

Title	Issue	Page	Lit. No.
Data Acquisition			
Aspects of data acquisition system design	August 1999	1	SLYT191
Low-power data acquisition sub-system using the TI TLV1572	August 1999	4	SLYT192
Evaluating operational amplifiers as input amplifiers for A-to-D converters	August 1999	7	SLYT193
Precision voltage references	November 1999	1	SLYT183
Techniques for sampling high-speed graphics with lower-speed A/D converters	November 1999	5	SLYT184
A methodology of interfacing serial A-to-D converters to DSPs	February 2000	1	SLYT175
The operation of the SAR-ADC based on charge redistribution	February 2000	10	SLYT176
The design and performance of a precision voltage reference circuit for 14-bit and 16-bit A-to-D and D-to-A converters	May 2000	1	SLYT168
Introduction to phase-locked loop system modeling	May 2000	5	SLYT169
New DSP development environment includes data converter plug-ins	August 2000	1	SLYT158
Higher data throughput for DSP analog-to-digital converters	August 2000	5	SLYT159
Efficiently interfacing serial data converters to high-speed DSPs	August 2000	10	SLYT160
Smallest DSP-compatible ADC provides simplest DSP interface	November 2000	1	SLYT148
Hardware auto-identification and software auto-configuration for the TLV320AIC10 DSP Codec — a “plug-and-play” algorithm	November 2000	8	SLYT149
Using quad and octal ADCs in SPI mode	November 2000	15	SLYT150
Building a simple data acquisition system using the TMS320C31 DSP	February 2001	1	SLYT136
Using SPI synchronous communication with data converters — interfacing the MSP430F149 and TLV5616	February 2001	7	SLYT137
A/D and D/A conversion of PC graphics and component video signals, Part 1: Hardware	February 2001	11	SLYT138
A/D and D/A conversion of PC graphics and component video signals, Part 2: Software and control	July 2001	5	SLYT129
Intelligent sensor system maximizes battery life: Interfacing the MSP430F123 Flash MCU, ADS7822, and TPS60311	1Q, 2002	5	SLYT123
SHDSL AFE1230 application	2Q, 2002	5	SLYT114
Synchronizing non-FIFO variations of the THS1206	2Q, 2002	12	SLYT115
Adjusting the A/D voltage reference to provide gain	3Q, 2002	5	SLYT109
MSC1210 debugging strategies for high-precision smart sensors	3Q, 2002	7	SLYT110
Using direct data transfer to maximize data acquisition throughput	3Q, 2002	14	SLYT111
Interfacing op amps and analog-to-digital converters	4Q, 2002	5	SLYT104
ADS82x ADC with non-uniform sampling clock	4Q, 2003	5	SLYT089
Calculating noise figure and third-order intercept in ADCs	4Q, 2003	11	SLYT090
Evaluation criteria for ADSL analog front end	4Q, 2003	16	SLYT091
Two-channel, 500-kSPS operation of the ADS8361	1Q, 2004	5	SLYT082
ADS809 analog-to-digital converter with large input pulse signal	1Q, 2004	8	SLYT083
Streamlining the mixed-signal path with the signal-chain-on-chip MSP430F169	3Q, 2004	5	SLYT078
Supply voltage measurement and ADC PSRR improvement in MSC12xx devices	1Q, 2005	5	SLYT073
14-bit, 125-MSPS ADS5500 evaluation	1Q, 2005	13	SLYT074
Clocking high-speed data converters	1Q, 2005	20	SLYT075
Implementation of 12-bit delta-sigma DAC with MSC12xx controller	1Q, 2005	27	SLYT076
Using resistive touch screens for human/machine interface	3Q, 2005	5	SLYT209A
Simple DSP interface for ADS784x/834x ADCs	3Q, 2005	10	SLYT210
Operating multiple oversampling data converters	4Q, 2005	5	SLYT222
Low-power, high-intercept interface to the ADS5424 14-bit, 105-MSPS converter for undersampling applications	4Q, 2005	10	SLYT223
Understanding and comparing datasheets for high-speed ADCs	1Q, 2006	5	SLYT231
Matching the noise performance of the operational amplifier to the ADC	2Q, 2006	5	SLYT237
Using the ADS8361 with the MSP430 USI port	3Q, 2006	5	SLYT244
Clamp function of high-speed ADC THS1041	4Q, 2006	5	SLYT253

Title	Issue	Page	Lit. No.
Power Management			
Stability analysis of low-dropout linear regulators with a PMOS pass element	August 1999	10	SLYT194
Extended output voltage adjustment (0 V to 3.5 V) using the TI TPS5210	August 1999	13	SLYT195
Migrating from the TI TL770x to the TI TLC770x	August 1999	14	SLYT196
TI TPS5602 for powering TI's DSP	November 1999	8	SLYT185
Synchronous buck regulator design using the TI TPS5211 high-frequency hysteretic controller	November 1999	10	SLYT186
Understanding the stable range of equivalent series resistance of an LDO regulator	November 1999	14	SLYT187
Power supply solutions for TI DSPs using synchronous buck converters	February 2000	12	SLYT177
Powering Celeron-type microprocessors using TI's TPS5210 and TPS5211 controllers	February 2000	20	SLYT178
Simple design of an ultra-low-ripple DC/DC boost converter with TPS60100 charge pump	May 2000	11	SLYT170
Low-cost, minimum-size solution for powering future-generation Celeron™-type processors with peak currents up to 26 A	May 2000	14	SLYT171
Advantages of using PMOS-type low-dropout linear regulators in battery applications	August 2000	16	SLYT161
Optimal output filter design for microprocessor or DSP power supply	August 2000	22	SLYT162
Understanding the load-transient response of LDOs	November 2000	19	SLYT151
Comparison of different power supplies for portable DSP solutions working from a single-cell battery	November 2000	24	SLYT152
Optimal design for an interleaved synchronous buck converter under high-slew-rate, load-current transient conditions	February 2001	15	SLYT139
-48-V/+48-V hot-swap applications	February 2001	20	SLYT140
Power supply solution for DDR bus termination	July 2001	9	SLYT130
Runtime power control for DSPs using the TPS62000 buck converter	July 2001	15	SLYT131
Power control design key to realizing InfiniBand™ benefits	1Q, 2002	10	SLYT124
Comparing magnetic and piezoelectric transformer approaches in CCFL applications	1Q, 2002	12	SLYT125
Why use a wall adapter for ac input power?	1Q, 2002	18	SLYT126
SWIFT™ Designer power supply design program	2Q, 2002	15	SLYT116
Optimizing the switching frequency of ADSL power supplies	2Q, 2002	23	SLYT117
Powering electronics from the USB port	2Q, 2002	28	SLYT118
Using the UCC3580-1 controller for highly efficient 3.3-V/100-W isolated supply design	4Q, 2002	8	SLYT105
Power conservation options with dynamic voltage scaling in portable DSP designs	4Q, 2002	12	SLYT106
Understanding piezoelectric transformers in CCFL backlight applications	4Q, 2002	18	SLYT107
Load-sharing techniques: Paralleling power modules with overcurrent protection	1Q, 2003	5	SLYT100
Using the TPS61042 white-light LED driver as a boost converter	1Q, 2003	7	SLYT101
Auto-Track™ voltage sequencing simplifies simultaneous power-up and power-down	3Q, 2003	5	SLYT095
Soft-start circuits for LDO linear regulators	3Q, 2003	10	SLYT096
UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 1	3Q, 2003	13	SLYT097
UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 2	4Q, 2003	21	SLYT092
LED-driver considerations	1Q, 2004	14	SLYT084
Tips for successful power-up of today's high-performance FPGAs	3Q, 2004	11	SLYT079
A better bootstrap/bias supply circuit	1Q, 2005	33	SLYT077
Understanding noise in linear regulators	2Q, 2005	5	SLYT201
Understanding power supply ripple rejection in linear regulators	2Q, 2005	8	SLYT202
Miniature solutions for voltage isolation	3Q, 2005	13	SLYT211
New power modules improve surface-mount manufacturability	3Q, 2005	18	SLYT212
Li-ion switching charger integrates power FETs	4Q, 2005	19	SLYT224
TLC5940 dot correction compensates for variations in LED brightness	4Q, 2005	21	SLYT225
Powering today's multi-rail FPGAs and DSPs, Part 1	1Q, 2006	9	SLYT232
TPS79918 RF LDO supports migration to StrataFlash® Embedded Memory (P30)	1Q, 2006	14	SLYT233
Practical considerations when designing a power supply with the TPS6211x	1Q, 2006	17	SLYT234
TLC5940 PWM dimming provides superior color quality in LED video displays	2Q, 2006	10	SLYT238
Wide-input dc/dc modules offer maximum design flexibility	2Q, 2006	13	SLYT239
Powering today's multi-rail FPGAs and DSPs, Part 2	2Q, 2006	18	SLYT240
TPS61059 powers white-light LED as photoflash or movie light	3Q, 2006	8	SLYT245
TPS65552A powers portable photoflash	3Q, 2006	10	SLYT246
Single-chip bq2403x power-path manager charges battery while powering system	3Q, 2006	12	SLYT247
Complete battery-pack design for one- or two-cell portable applications	3Q, 2006	14	SLYT248

Title	Issue	Page	Lit. No.
Power Management (Continued)			
A 3-A, 1.2-V _{OUT} linear regulator with 80% efficiency and P _{LOST} < 1 W	4Q, 2006	10	SLYT254
bq25012 single-chip, Li-ion charger and dc/dc converter for Bluetooth® headsets	4Q, 2006	13	SLYT255
Fully integrated TPS6300x buck-boost converter extends Li-ion battery life	4Q, 2006	15	SLYT256
Interface (Data Transmission)			
TIA/EIA-568A Category 5 cables in low-voltage differential signaling (LVDS)	August 1999	16	SLYT197
Keep an eye on the LVDS input levels	November 1999	17	SLYT188
Skew definition and jitter analysis	February 2000	29	SLYT179
LVDS receivers solve problems in non-LVDS applications	February 2000	33	SLYT180
LVDS: The ribbon cable connection	May 2000	19	SLYT172
Performance of LVDS with different cables	August 2000	30	SLYT163
A statistical survey of common-mode noise	November 2000	30	SLYT153
The Active Fail-Safe feature of the SN65LVDS32A	November 2000	35	SLYT154
The SN65LVDS33/34 as an ECL-to-LVTTL converter	July 2001	19	SLYT132
Power consumption of LVPECL and LVDS	1Q, 2002	23	SLYT127
Estimating available application power for Power-over-Ethernet applications	1Q, 2004	18	SLYT085
The RS-485 unit load and maximum number of bus connections	1Q, 2004	21	SLYT086
Failsafe in RS-485 data buses	3Q, 2004	16	SLYT080
Maximizing signal integrity with M-LVDS backplanes	2Q, 2005	11	SLYT203
Device spacing on RS-485 buses	2Q, 2006	25	SLYT241
Improved CAN network security with TI's SN65HVD1050 transceiver	3Q, 2006	17	SLYT249
Detection of RS-485 signal loss	4Q, 2006	18	SLYT257
Amplifiers: Audio			
Reducing the output filter of a Class-D amplifier	August 1999	19	SLYT198
Power supply decoupling and audio signal filtering for the Class-D audio power amplifier	August 1999	24	SLYT199
PCB layout for the TPA005D1x and TPA032D0x Class-D APAs	February 2000	39	SLYT182
An audio circuit collection, Part 1	November 2000	39	SLYT155
1.6- to 3.6-volt BTL speaker driver reference design	February 2001	23	SLYT141
Notebook computer upgrade path for audio power amplifiers	February 2001	27	SLYT142
An audio circuit collection, Part 2	February 2001	41	SLYT145
An audio circuit collection, Part 3	July 2001	34	SLYT134
Audio power amplifier measurements	July 2001	40	SLYT135
Audio power amplifier measurements, Part 2	1Q, 2002	26	SLYT128
Amplifiers: Op Amps			
Single-supply op amp design	November 1999	20	SLYT189
Reducing crosstalk of an op amp on a PCB	November 1999	23	SLYT190
Matching operational amplifier bandwidth with applications	February 2000	36	SLYT181
Sensor to ADC — analog interface design	May 2000	22	SLYT173
Using a decompensated op amp for improved performance	May 2000	26	SLYT174
Design of op amp sine wave oscillators	August 2000	33	SLYT164
Fully differential amplifiers	August 2000	38	SLYT165
The PCB is a component of op amp design	August 2000	42	SLYT166
Reducing PCB design costs: From schematic capture to PCB layout	August 2000	48	SLYT167
Thermistor temperature transducer-to-ADC application	November 2000	44	SLYT156
Analysis of fully differential amplifiers	November 2000	48	SLYT157
Fully differential amplifiers applications: Line termination, driving high-speed ADCs, and differential transmission lines	February 2001	32	SLYT143
Pressure transducer-to-ADC application	February 2001	38	SLYT144
Frequency response errors in voltage feedback op amps	February 2001	48	SLYT146
Designing for low distortion with high-speed op amps	July 2001	25	SLYT133
Fully differential amplifier design in high-speed data acquisition systems	2Q, 2002	35	SLYT119
Worst-case design of op amp circuits	2Q, 2002	42	SLYT120
Using high-speed op amps for high-performance RF design, Part 1	2Q, 2002	46	SLYT121
Using high-speed op amps for high-performance RF design, Part 2	3Q, 2002	21	SLYT112
FilterPro™ low-pass design tool	3Q, 2002	24	SLYT113
Active output impedance for ADSL line drivers	4Q, 2002	24	SLYT108

Title	Issue	Page	Lit. No.
Amplifiers: Op Amps (Continued)			
RF and IF amplifiers with op amps	1Q, 2003	9	SLYT102
Analyzing feedback loops containing secondary amplifiers	1Q, 2003	14	SLYT103
Video switcher using high-speed op amps	3Q, 2003	20	SLYT098
Expanding the usability of current-feedback amplifiers	3Q, 2003	23	SLYT099
Calculating noise figure in op amps	4Q, 2003	31	SLYT094
Op amp stability and input capacitance	1Q, 2004	24	SLYT087
Integrated logarithmic amplifiers for industrial applications	1Q, 2004	28	SLYT088
Active filters using current-feedback amplifiers	3Q, 2004	21	SLYT081
Auto-zero amplifiers ease the design of high-precision circuits	2Q, 2005	19	SLYT204
So many amplifiers to choose from: Matching amplifiers to applications	3Q, 2005	24	SLYT213
Instrumentation amplifiers find your needle in the haystack	4Q, 2005	25	SLYT226
High-speed notch filters	1Q, 2006	19	SLYT235
Low-cost current-shunt monitor IC revives moving-coil meter design	2Q, 2006	27	SLYT242
General Interest			
Synthesis and characterization of nickel manganite from different carboxylate precursors for thermistor sensors	February 2001	52	SLYT147
Analog design tools	2Q, 2002	50	SLYT122

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