Clocking the RF ADC: Should you worry about jitter or phase noise?

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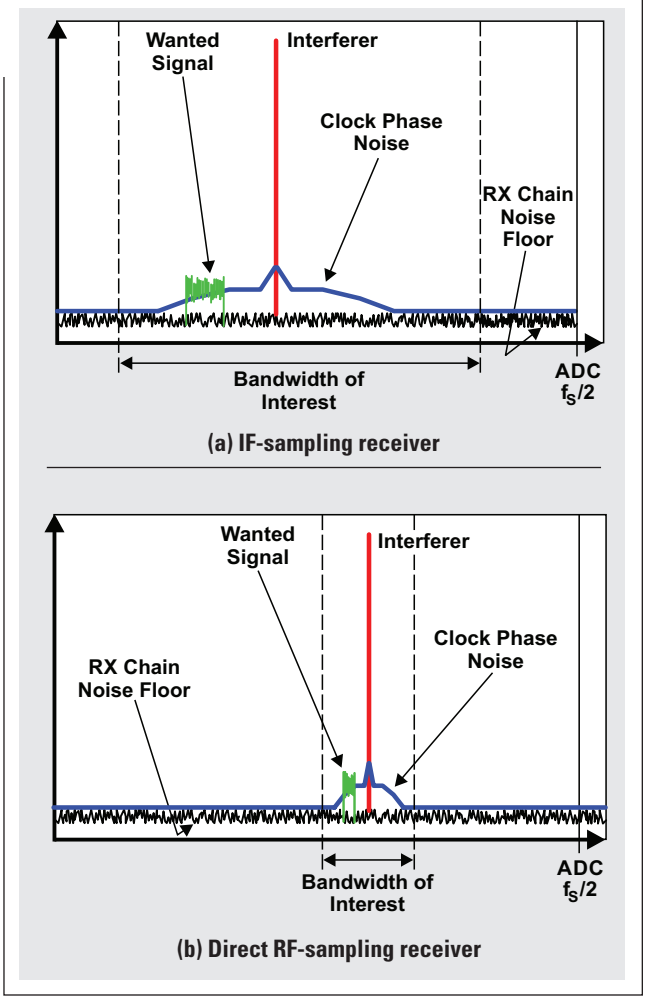
Introduction

A critical specification of a receiver is the blocker specification. It determines the weakest signal power level that can be successfully detected in the presence of an in-band interferer/blocker. To determine the receiver performance during a blocking event, system designers have to analyze various noise sources of the receiver, including the clock noise contribution of the data converter .

In a traditional heterodyne receiver, the noise contribution of the data-converter clock is typically derived in the time domain using integrated jitter numbers. In a direct RF-sampling architecture (Figure 1), the actual signal bandwidth may be much smaller than the Nyquist zone of the analog-to-digital converter (ADC). Rather than integrating the phase-noise contribution of the clock across the entire Nyquist zone, it may make more sense to work directly with frequency offset-dependent phase noise in the frequency domain. Even though the time-domain approach is simpler, it may result in an unrealistic and impractical clock-noise requirement.

Since recent introduction of high-performance, direct RF-sampling converters, such as the ADC12J4000 and ADC32RF45, customers frequently ask about external phase-noise requirements for the ADC sampling clock. The answer depends on the customer's requirements for receiver performance, as well as several additional factors that impact the clock noise of data converters. These include ADC aperture jitter, clock amplitude or slew rate, signal input frequency and input-signal amplitude, to name a few. This article shows how to derive the noise contribution in the frequency domain and compares it to a traditional calculation approach of time-domain jitter.

Figure 1. Clock phase noise contribution



ADC noise analysis in the frequency domain

The data-converter noise contribution in the frequency domain can be analyzed using the following five steps. Simplified diagrams normalized to the input signal frequency are added for better illustration.

1. Obtain the external-clock phase noise (PN_E) and ADC aperture jitter (PN_A) in the frequency domain in dBc/Hz. The frequency bin sizes and steps need to be identical. The clock phase-noise data is typically given in a log-type format. If the ADC aperture jitter is not assumed flat across frequency, some data interpolation may be necessary to match the phase-noise data format. As discussed earlier, the ADC aperture jitter is clock-amplitude dependent, which needs to be considered as well.

2. PN_C is the combined external-clock phase noise and the ADC aperture jitter that is calculated with Equation 1 and shown in Figure 2. The top red curve shows the shift that adjusts it for signal-amplitude back-off as calculated in step 3.

$$PN_C = 20\log\left[\sqrt{\left(10^{\frac{PN_E}{20}}\right)^2 + \left(10^{\frac{PN_A}{20}}\right)^2}\right] \text{ dBc/Hz} \quad (1)$$

3. Equation 2 accounts for the signal input-frequency shifting of the combined clock noise.

$$PN_{f_{IN}} = PN_C + 20\log\left(\frac{f_{IN}}{f_S}\right) \quad (2)$$

where f_{IN} is the signal input frequency and f_S is the ADC sampling rate. As the signal input frequency increases, the signal-to-noise (SNR) degradation due to clock noise also increases.

4. It is also important to account for the amplitude of the input signal. Reducing the signal amplitude in respect to the ADC full-scale directly reduces the clock noise contribution. For example, a 3-dB back-off (A_{IN} = –3 dBFS) reduces the noise power in each frequency bin by 3 dB.
5. The final step is to combine the shifted clock noise with the inherent thermal noise of the data converter. This results in the expected total noise contribution from the ADC for specific frequency offsets from the input signal as illustrated in Figure 3.

The final ADC noise in Figure 3 explains several use cases. For example, for high input frequencies in under-sampling scenarios (where f_S = 3 GSPS, f_{IN} = 1.8 GHz), the clock noise contribution is increased. This pushes the close-in phase noise from the clock above the ADC's thermal noise floor.

Figure 2. Data converter noise after combining ADC aperture jitter with the external clock phase noise

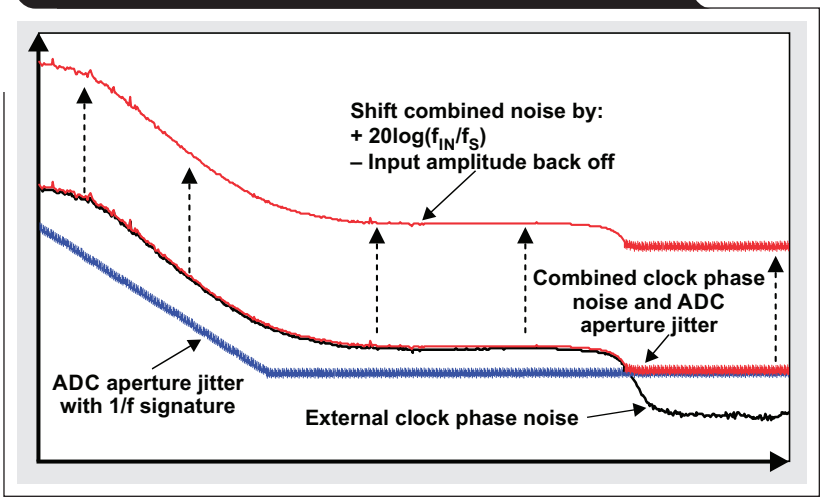


Figure 3. Total ADC noise after adding the data-converter thermal noise

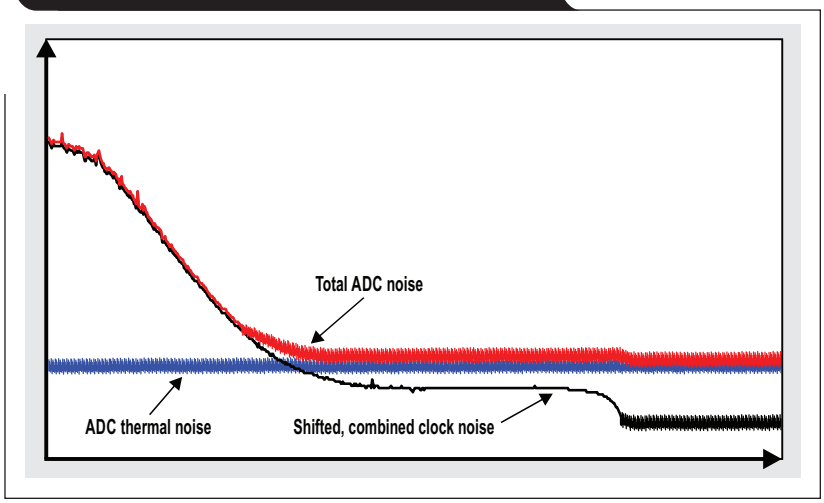
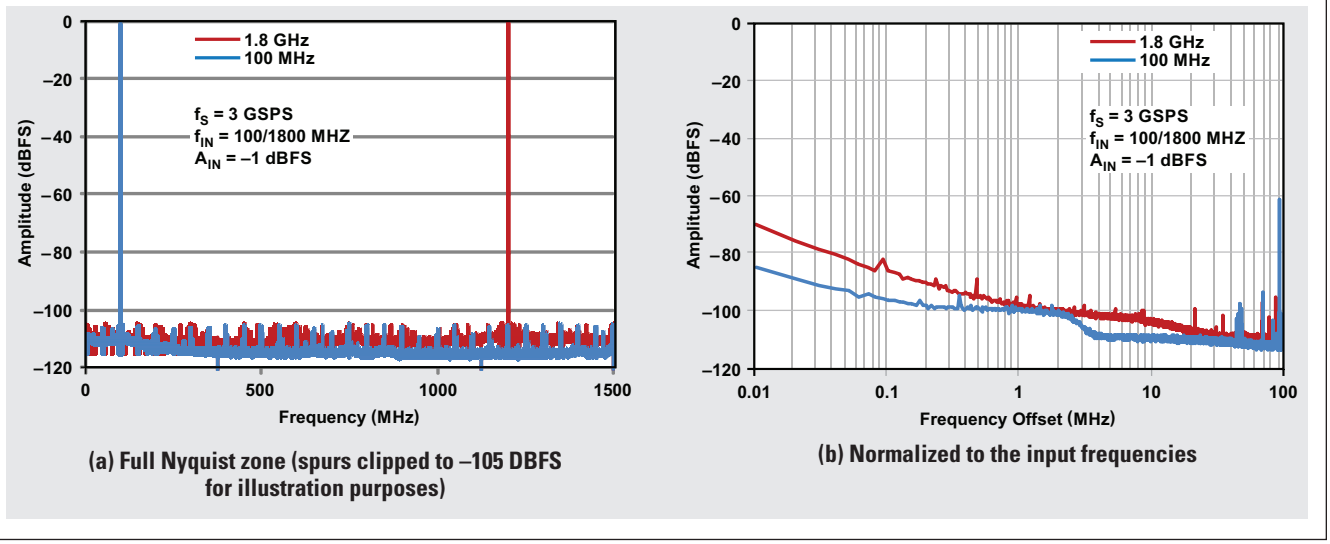


Figure 4. Fast Fourier transform (FFT) noise comparison



(a) Full Nyquist zone (spurs clipped to –105 DBFS for illustration purposes)

(b) Normalized to the input frequencies

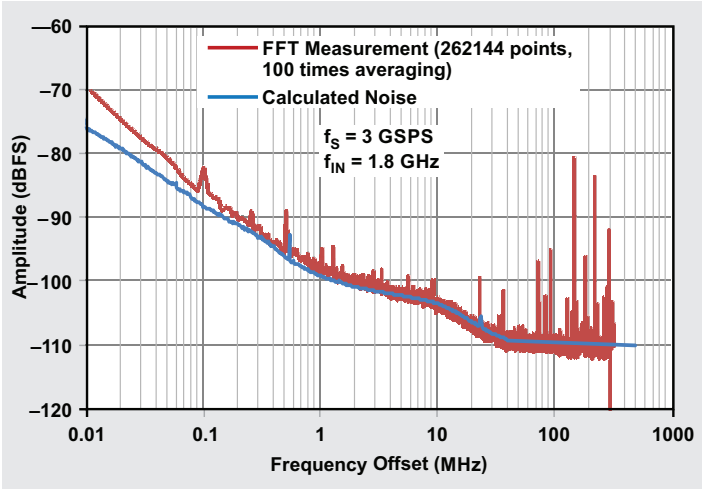
As a result, the ADC experiences SNR degradation because of clock jitter, which is clearly visible in Figure 4. In Figure 4a, the red curve with a 1.8-GHz input signal shows larger close-in noise, as well as a distant noise floor compared to the 100-MHz curve. Both are due to the ADC aperture jitter increasing in magnitude because of higher input frequency.

Figure 4b shows the phase-noise signature (frequency corner ≈ 3 MHz) of the input signal itself in the blue curve. While it does not experience any amplitude shift, it disappears in the clock noise in the 1.8-GHz scenario.

Calculation versus measurement

How well can the data-converter noise be predicted with this frequency-domain analysis? The noise calculation was performed for the previous measurement using the aperture-jitter information of the ADC32RF45, along with the phase-noise information of both the clock and input signal generators. The results in Figure 5 show a very close match where other degradations, such as power-supply noise and temperature effects, were not included. In this way, the system designer can estimate the ADC clock-noise contribution at a specific frequency offset.

Figure 5. Noise comparison between FFT measurement and calculated data converter noise



Time domain versus frequency domain?

System engineers are used to operating in the time domain with the simple jitter equation of $SNR_{Jitter} = 20\log(2\pi f_{IN} \times t_{Jitter})$. Table 1 compares the frequency-domain approach illustrated in this article against the traditional time-domain method.

Table 1. Analysis comparison of clock-noise contribution in ADCs

Step	Time-domain analysis	Frequency-domain analysis
1	Obtain jitter by integrating the external clock phase noise over desired bandwidth: $t_E = \frac{\sqrt{2\int PN_E}}{2\pi f_S}$ (3) where PN_E = External clock phase noise, and f_S = ADC sampling rate	Obtain external clock-phase noise in dBc/Hz. Convert ADC aperture jitter into phase noise in dBc/Hz with integration bandwidth of double the ADC sampling rate. Can be assumed flat across Nyquist zone unless specific information about 1/f behavior is available, as on the ADC32RF45.
2	Combine external with ADC internal aperture jitter: $t_J = \sqrt{t_E^2 + t_A^2}$ (4) Assuming the ADC aperture is in fact also noise integrated over a bandwidth $t_J = \frac{1}{2\pi f_S} \times \sqrt{\left(\sqrt{2\int PN_E}\right)^2 + \left(\sqrt{2\int PN_A}\right)^2}$ (5)	Combine external clock phase noise with ADC internal aperture phase noise. This is calculated per frequency bin. $PN_C = 20\log\sqrt{\left(10^{\frac{PN_E}{20}}\right)^2 + \left(10^{\frac{PN_A}{20}}\right)^2}$ (9)
3	Calculate SNR degradation due to jitter and input frequency: $PN_{Thermal} = SNR_{Thermal} + 10\log(f_S/2)$ (6) Adding previous term: $SNR_{Jitter} = 20\log\left[\frac{f_{IN}}{f_S} \times \sqrt{\left(\sqrt{2\int PN_E}\right)^2 + \left(\sqrt{2\int PN_A}\right)^2}\right]$ (7)	Shift combined phase noise by input frequency: $PN_{f_{IN}} = PN_C + 20\log\left(\frac{f_{IN}}{f_S}\right)$ (10)
4	Adjust for signal input amplitude: Subtract ADC back-off (in dB) from the SNR_{Jitter} value.	Adjust for signal input amplitude: Subtract input signal back-off from the phase-noise amplitude for each individual frequency bin.
5	Combine result from Step 4 with ADC thermal noise: $SNR = 20\log\left[\sqrt{\left(10^{\frac{SNR_{Jitter}}{20}}\right)^2 + \left(10^{\frac{SNR_{Thermal}}{20}}\right)^2}\right]$ (8)	Combine result from Step 4 with ADC thermal noise: $Noise_{bin} = 20\log\sqrt{\left(10^{\frac{PN_{f_{IN}}}{20}}\right)^2 + \left(10^{\frac{PN_{Thermal}}{20}}\right)^2}$ (11) where $PN_{Thermal} = SNR_{Thermal} + 10\log(f_S/2)$
6	(Intentionally left blank)	Compare with actual measured FFT data. Scale noise per bin with FFT bin size: $Noise_{FFT} = Noise_{bin} + 10\log(binsize)$ (12)

Conclusion

Evaluating the noise contribution from an RF-sampling data converter gives the system designer a very powerful tool when analyzing system-interferer specifications. The side-by-side comparison shows that both time- and frequency-domain methods are using the same information. However, the frequency-domain analysis preserves crucial application-specific information for frequency offset and may be much better suited for working with modern, high-performance RF-sampling converters such as the ADC32RF45.

Related Web sites

Product information:
ADC12J4000
ADC32RF45

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