Stretching a single-phase design with a buck controller to support high currents

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Introduction

This article is about pushing the design boundaries of a single-phase buck controller to allow higher current levels than what the parametric tables in the product folders suggest. The key advantage is a lower-cost solution because it avoids the use of two inductors and more expensive two-phase controllers.

Buck-controller parametric tables or selection guides typically give a maximum current; in most cases, it's 20 A to 25 A. Where does this range come from? Is the current really limited to 25 A?

In essence, the answer boils down to thermals. There are various parameter knobs in designing a buck controller that can be used to help push the boundaries to higher current levels. In referring to knobs, it means various design parameters that can be changed. Some knobs have a big impact on thermals, while others, if turned in a mutually beneficial direction to the design criteria, can help minimize temperature rise. In a buck-controller design, a good metal-oxide semiconductor field-effect transistor (MOSFET) and controller pair helps, but many other knobs play a key role in achieving the holistic target of currents higher than 25 A.

With buck converters, there are a limited number of knobs to turn, and there is always a manufacturer-specified maximum output current based on curves for the safe operating area (SOA) that are derived from thermal limits.

With the platform for buck controllers, depending on how the various knobs are used, the boundaries can be pushed. The efficiency of a buck converter is just a number unless it is put into perspective with thermals.

Figure 1 shows the various knobs that can be changed to achieve design goals. To elaborate, here's what's tunable with the knobs shown in Figure 1:

- Frequency, f_{SW}: The switching frequency of the controller. The higher the frequency, the greater the switching losses.
- $R_{DS(on)}$: The drain-to-source on-resistance affects conduction losses. Duty cycle also plays a factor in determining whether the high-side (HS) or synchronous FET plays a bigger role in the losses.
- HS FET rise time: The slew rate of the turn-on of the HS FET. A faster rise time reduces switching losses, but the trade-off could be switch-node spikes and ringing.
- LDCR: The inductor DC resistance directly contributes to conduction losses.
- Q_{gd}: The gate drain charge. This is an important parameter that relates to switching loss. Q_{gd} is inversely proportional to $R_{DS(on)}$.
- Q_{gs}: The gate source charge. This is also an important parameter that relates to switching loss.
- V_{Miller}: The Miller plateau voltage of the FET, which affects the rise time of the HS FET.

Figure 1. Various knobs that affect losses and efficiency in a buck controller
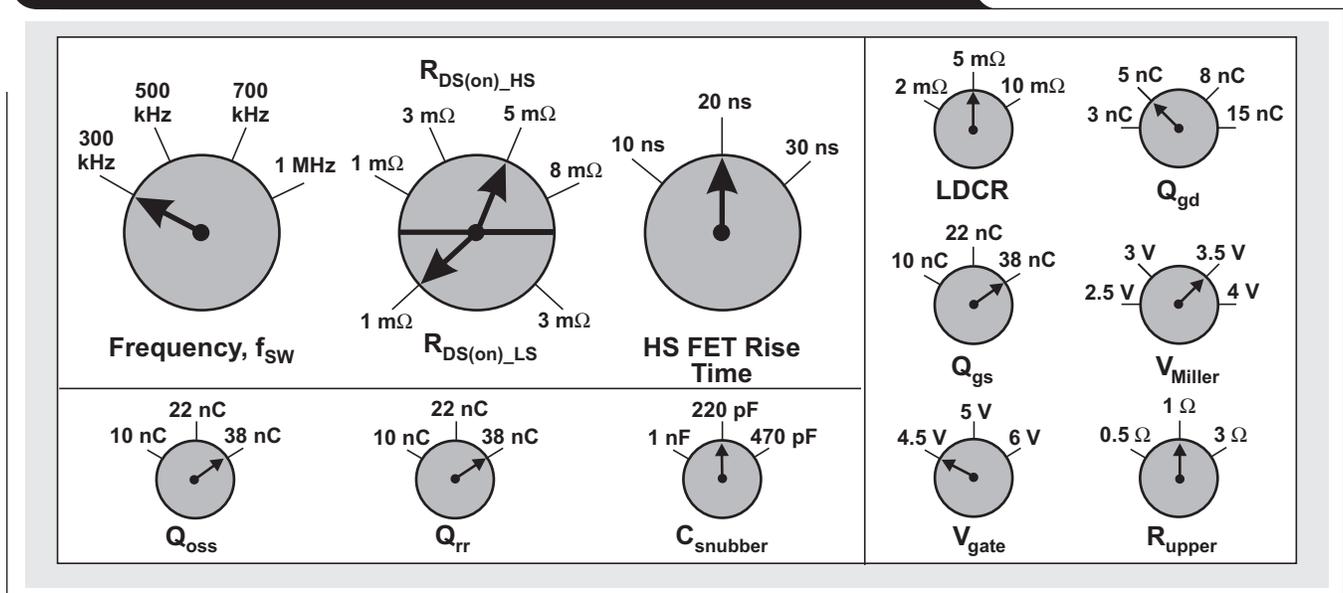
- V_{gate}: The gate voltage provided by the controller. The higher the voltage, the more efficiency.
- R_{upper} (R_{pullup}): The HS-driver ON-resistance. Lower numbers mean faster rise times and fewer switching losses.
- $C_{snubber}$: The snubber capacitance along with the resistor at switch node. $C_{snubber}$ effectively controls ringing or peak switch voltages with efficiency trade-offs.
- Q_{oss}: The output charge affecting switching losses. Some MOSFET data sheets only give C_{oss}. To obtain Q_{oss}, use the formula $Q_{oss} = C_{oss} \times V_{DS}$.
- Q_{rr}: The body diode reverse-recovery charge of the MOSFET.

So in essence, the selected controller, FET and inductor will determine the maximum current capability of a single-phase design. How exactly can the maximum current be derived? The answer is the loss in each component, as shown in Figure 2. Once the losses are known, the temperature rise can be calculated by using the respective junction-to-ambient thermal resistance (θ_{JA}) numbers, which lead to the health meter shown in Figure 3. The goal is to keep the Temp Rise + $T_{A(max)}$ << $T_{J(max)}$ for semiconductor devices. In a typical system, $T_{A(max)}$ and $T_J(max)$ are fixed parameters, so the key parameter that can be controlled is Temp Rise.

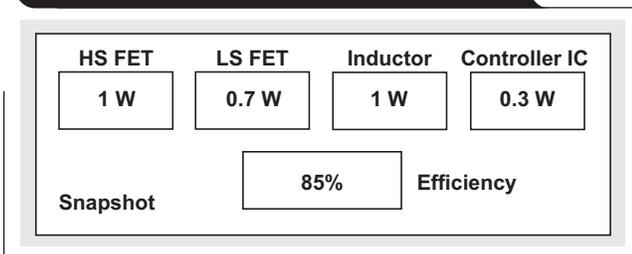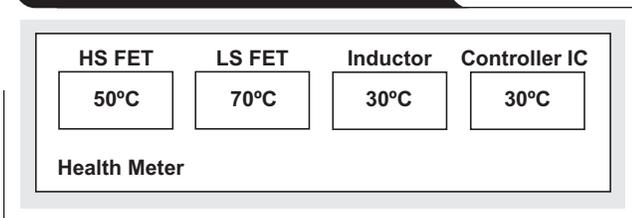Figure 2. Snapshot of the losses in key components and overall efficiency

Figure 3. Temperature rise of the key components

The following descriptions are for two practical examples: A 35-A design for a 1.2-V output and a 50-A design for a 10-V output. The input voltage is 12 V.

Example No. 1: V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 35 A

For this example, a controller, FET, and inductor were selected and the LM27402 was chosen for the controller. Table 1 and Figures 4 and 5 were used to evaluate possible FETs to get an idea of any potential problems and some generic curves, where I_{OUT} = 35 A, f_{SW} = 300 kHz and L = 0.47 µH.

Table 1. FETs under consideration

FETs	$R_{DS(on)}$ mΩ	Q_g (nC)	Q_{gd} (nC)	Q_{oss} (nC)	R_g (Ω)	V_{Miller} (V)
CSD17573Q5B	1.19	49	11.9	21	0.9	2.3
CSD17311Q5	1.80	24	5.2	47	1.2	2.1
CSD17301Q5A	2.30	19	4.3	35	1.3	2.3
CSD17306Q5A	3.30	11.8	2.4	23	1	2.1
CSD17310Q5A	5.90	8.9	2.1	8.6	0.9	2.2

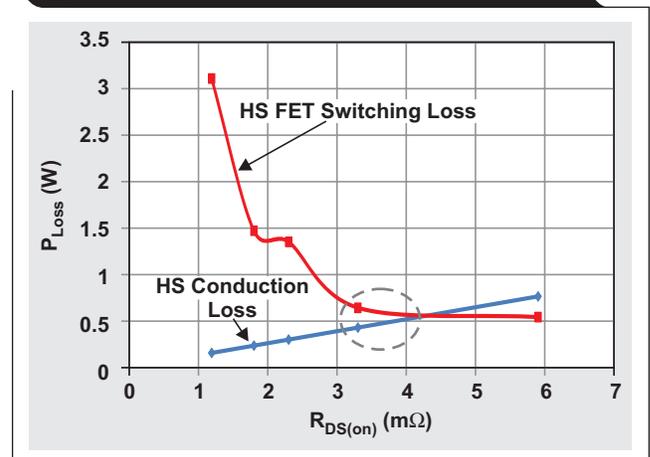Figure 4. HS FET conduction and switching losses for the FETs listed in Table 1
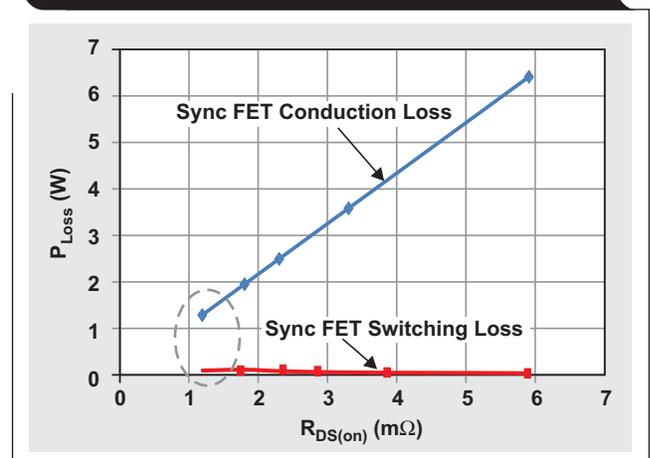

Figure 5. Low-side (LS) FET conduction and switching losses for the FETs listed in Table 1

Designers typically use the intersection of conduction and switching losses and pick a FET with an $R_{DS(on)}$ in this range. In this first example, the 3.3-mΩ CSD17306Q5A was chosen for the HS FET and the 1.19-mΩ CSD17573Q5B was chosen for the LS FET; call this configuration No. 1.

The switching plus conduction losses in the HS and LS FETs are 1.07 W and 1.41 W, respectively. The θ_{JA} numbers for the FETs will provide the temperature rise:

- HS FET temperature rise: 1.07 W $\times$ 49°C/W = 52°C
- LS FET temperature rise: 1.41 W $\times$ 50°C/W = 70°C (conduction loss = 1.3 W, switching loss = 0.11 W)

One thing to keep in mind is that θ_{JA} numbers are from the data sheet; in actual designs, these numbers may be lower depending on the size of the board, the number of layers, the copper thickness and the number of vias.

Assuming a maximum ambient temperature of 75°C, this design could be used since $T_J < T_{J(max)}$ (150°C), but it would be better to have more margin for the LS FET. One way to obtain more margin is to use another FET in parallel, which cuts conduction losses in half and doubles switching losses.

Configuration No. 2 uses one 3.3-mΩ CSD17306Q5A HS FET and two 0.595-mΩ CSD17573Q5B LS FETs. The conduction loss for the LS FET is now 0.65 W compared to 1.3 W earlier and the switching loss is 0.21 W compared to 0.11 W earlier.

- LS FET temperature rise: 0.86 W x 50°C/W = 43°C

By following proper design methodologies, a 35-A or 40-A single-phase design is possible, even though the data sheet or parametric table for the LM27402 gave the maximum current as 25 A.

What other parameters of the controller integrated circuit (IC) influence the efficiency? The biggest parameter is the switching frequency, as shown in Figure 6 and applied to configuration No. 2. Operating at lower frequencies keeps losses down. The HS FET has a steep slope compared to the LS FET.

Figure 6. Switching losses for HS and LS FETs versus frequency
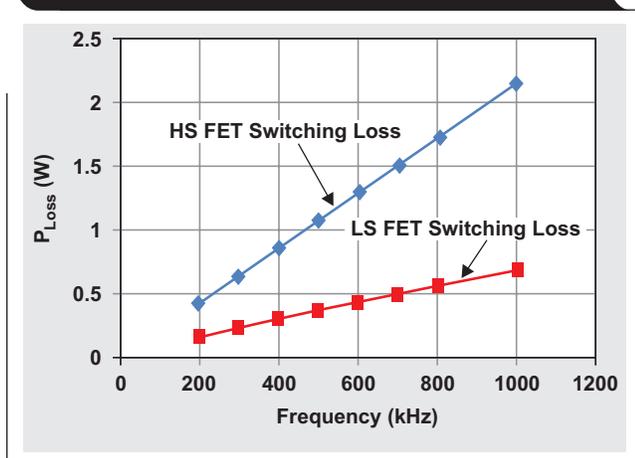
The following are four other important parameters to consider in a controller.

Internal regulator current limit
This is an often overlooked specification that creeps into the red zone when operating at high switching frequencies and with parallel FETs. The current drawn from the internal regulator can be calculated as shown in Equation 1.

$$I_{Regulator} = (Q_{g\_HS} + Q_{g\_LS}) \times f_{SW} \qquad (1)$$

where Q_{g_HS} and Q_{g_LS} are the total gate charges for the high-side and low-side FETs, respectively, from the origin to the point at which the gate voltage is equal to the driver voltage.

Table 2 shows the current drawn for various frequencies in Configuration No. 2. The V_{DD} current limit specification for the LM27402 is 106 mA (typical), so to be conservative, assume it is reduced by 20% for establishing a limit to stay under, which is 85 mA. Controllers that can support high currents have a high current limit for the regulator. Examples include the TPS53819A (152 mA) and TPS40400 (100 mA).

Table 2. Regulator current versus frequency

	Two LS FETs	Three LS FETs
Frequency (kHz)	$I_{Regulator}$ (mA)	$I_{Regulator}$ (mA)
200	22	32
300	33	48
400	44	64
500	55	80
700	77	112
1000	110	159

Internal regulator voltage
A higher level for the internal regulator voltage enables the best $R_{DS(on)}$ performance for the FETs. It also affects the transition time and hence the switching losses. Equation 2 calculates the gate voltage available to drive a FET.

$$V_{gate\_available} = V_{gate} - V_{GS}(Miller\,plateau) \qquad (2)$$

where V_{gate} is the gate-driver output voltage and V_{GS} is the Miller plateau voltage.

Equation 3 calculates the current available to drive the FET.

$$I_{gate} = \frac{V_{gate\_available}}{R_{drive} + R_{gate}} \qquad (3)$$

where R_{drive} is the driver pull-up resistance and R_{gate} is the FET gate resistance.

Equation 4 calculates the transition time required for the current to ramp up.

$$t_{trans} = \frac{Q_{gd\_Miller}}{I_{gate}} \qquad (4)$$

where Q_{gd_Miller} is the charge injected into the FET gate during the time the device is in the Miller plateau.

Equation 5 calculates transition losses that occur during the transition time (t_{trans}).

$$P_{trans\_losses} = 2 \quad V_{IN} \quad I_{OUT} \quad t_{trans} \quad f_{SW} \qquad (5)$$

where V_{IN} and V_{OUT} are the input and output voltages, and f_{SW} is the switching frequency.

HS FET gate pull-up resistor

A lower value for the HS FET pull-up resistor (as calculated in Equation 3) translates to higher gate current and faster transition times, leading to fewer switching losses. Controllers geared toward high-current capability such as the LM27402, LM27403, TPS40400 or TPS53819A have a pull-up resistance of 1.5 Ω or less. Some data sheets or selection guides emphasize the rating for gate-drive peak current; this can be misleading as the peak-current numbers do not show up in calculating transition times as shown in Equation 4.

Duty-cycle considerations

It's a good idea to check the minimum or maximum duty cycle that the controller supports and whether it meets design requirements.

Example No. 2: V_{IN} = 12 V, V_{OUT} = 10 V, I_{OUT} = 50 A

To start off, a controller is required that supports an 83% duty cycle. The LM27403 fits the bill. Given the high duty cycle, the HS FET needs to be a low $R_{DS(on)}$ choice. Unfortunately, a low-$R_{DS(on)}$ FET means a typically higher Q_{gd}, leading to higher switching losses. The availability of good FETs helps minimize the impact. In this case, the TPHR9003NL was chosen, which has a low gate charge. The high duty cycle requires special attention to the HS FET losses and, in this case, considering the high current and duty cycle, two FETs were used in parallel and a 200-kHz switching frequency minimizes the impact of using FETs in parallel. Using two TPHR9003NL HS FETs and one TPHR9003NL LS FET provided these conduction and switching losses:

- HS FETs: conduction loss = 1.16 W,
  switching loss = 3.7 W, and
  total loss = 4.85 W
- LS FET: conduction loss = 0.48 W,
  switching loss = 0.071 W, and
  total loss = 0.55 W

Since there are two HS FETs in parallel, the losses are divided into two for the purposes of calculating temperature rise:

- HS FET temperature rise: 2.425 W × 44.6°C/W = 108°C
- LS FET temperature rise: 0.55 W × 44.6°C/W = 25°C

Given that the maximum junction temperature for the FET is 150°C, the maximum ambient operating temperature is around 40°C. To extend the range for the operating ambient temperature, it was essential to use forced-air

cooling and/or heat sinking for the HS FETs. Forced-air cooling reduces the θ_{JA} and helped limit the temperature rise of the HS FETs to around 50°C. The efficiency of the design is 97.88%, an example of why efficiency numbers can be misleading; even with such high efficiency, the losses of the HS FET lead to a temperature rise that necessitated the use of forced air cooling.

It may seem that increasing the number of FETs used in parallel would help, and while it does help reduce conduction losses, adding more capacitors in parallel increases switching losses. For example, if three TPHR9003NL HS FETs were used, the losses would be:

- HS_FETs: conduction loss = 0.77 W,
  switching loss = 5.53 W, and
  total loss = 6.3 W.

The power loss for each FET is 2.1 W. Although this is an improvement over 2.425 W when using two FETs, it would be better to reduce θ_{JA} by using forced air cooling for a reliable design over a wide temperature range. A lower driver pull-up resistance (R_{drive}) would also help bring down the switching losses.

Conclusion

High-current single-phase designs are possible and can be designed reliably over and beyond the suggested parametric table values when:

- Proper design considerations are followed and the FET's switching frequency and various other knobs shown in Figure 1 are chosen carefully.
- Inductors are selected to keep the ripple current ratio below a 0.4 to 0.5 range.
- The direct-current resistance is selected such that the temperature rise of the inductor at the rated current is below 40°C.

References

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3. Arvind Raj, "Calculating Efficiency," Texas Instruments Application Report (SLVA390), February 2010.

Related Web sites

Product information:
**LM27402, LM27403, TPS53819A, TPS40400
CSD17306Q5A, CSD17573Q5B**

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