AN-335 Digital PLL Synthesis

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Digital PLL Synthesis

National Semiconductor
Application Note 335
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I. System Concepts

INTRODUCTION

Digital tuning systems are fast replacing the conventional mechanical systems in AM/FM and television receivers. The desirability of the digital approach is mainly due to the following features:

- Precise tuning of station frequencies
- Exact digital frequency display
- Keyboard entry of desired frequency
- Virtually unlimited station memory
- Up/down scanning through the band
- Station ''search'' (stop on next active station)
- Power on to the last station
- Easy option for time-of-day clock

In addition, recent developments in large scale integrated circuit technology and new varactor diodes for the AM band have made the cost-benefit picture for digital tuning very attractive. System partitioning is extremely important in optimizing this cost-benefit picture, as will be discussed.

SYSTEM DESCRIPTION

A simplified block diagram of a typical digitally tuned receiver is shown in *Figure 1*. Notice this receiver could be one for AM, FM, marine radio, or television; it makes no difference. The frequency synthesizer block generates the local oscillator frequency for the receiver, just as a conventional mechanical tuner would. However, the phase-locked-loop (PLL) acts as an integral frequency multiplier of an accurate crystal controlled reference frequency while the mechanical type provides a continuously variable frequency output with no reference. Some method of controlling the value of the multiplier for channel tuning must be provided. The other RF, IF, and audio/video circuitry will be the same as in the mechanical tuning method.

There are many different ways to partition the frequency synthesizer system to perform the digital tuning function.

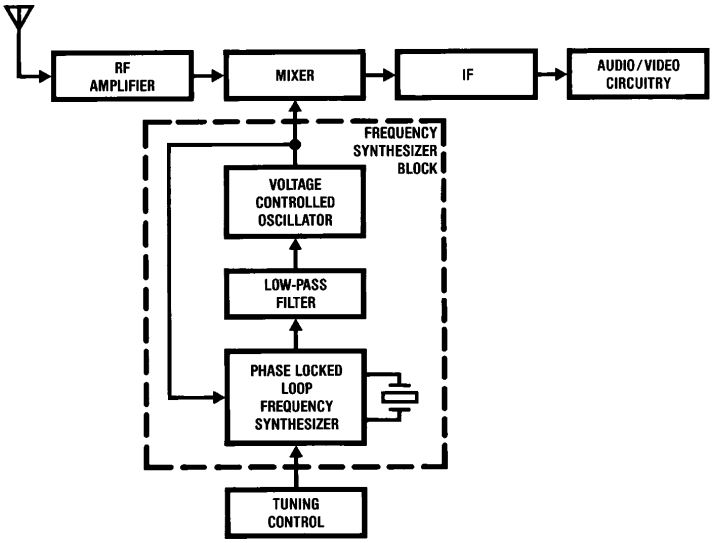

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FIGURE 1. Block Diagram of a Digitally Tuned Receiver

PROGRAMMABLE CONTROLLER FUNCTION

The most cost-effective application of different IC process technologies is shown in *Figure 2*. The controller is separate from the PLL. The controller can be as simple as a mask programmable microcontroller* or as complicated as a high-powered microprocessor system. It can be done most economically with NMOS technology because of the logic density possible and the small size of the RAM/ROM memory cells. It could also be CMOS for extremely low power consumption in standby mode.

BASIC PHASE-LOCKED-LOOP FUNCTION

The DS8906/7/8 series of PLLs utilize a dual-modulus frequency synthesis technique. The reasons for this and the PLL itself will now be discussed.

Figure 3 is a diagram of the most simple phase-locked-loop. A particular reference frequency is generated by a crystal oscillator and some fixed divider, and this goes into one side of a digital phase comparator. A voltage controlled oscillator (VCO) feeds directly into the other input of the phase comparator. The output of the phase comparator is an error signal which is filtered and fed back to the VCO as a DC control voltage.

In lock, the phase error must be zero, so f_{IN} equals f_{REF}. This system provides only one output frequency, that being equal to the reference frequency.

Figure 4 is basically the same but now a programmable divide-by-N counter is between the VCO and the phase comparator. The input to the phase comparator (f_{IN}) now becomes the output frequency of the VCO (f_{OUT}) divided by N, where N is the division code loaded into the programmable counter. This means f_{OUT}/N must equal f_{REF}. Thus, the VCO output frequency becomes $N \times f_{REF}$, and f_{OUT} can now be changed in integral steps of f_{REF} by merely changing N.

*Such as National's COP™ family.

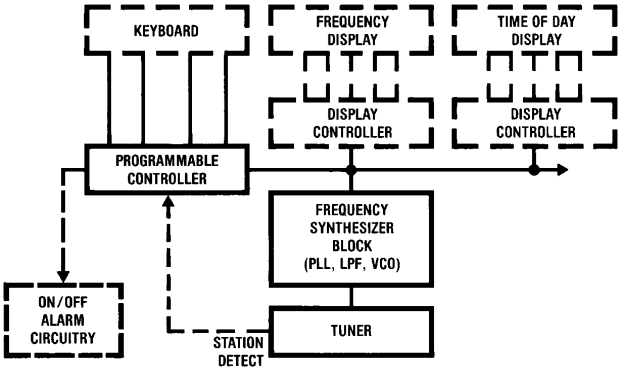

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FIGURE 2. System Block Diagram

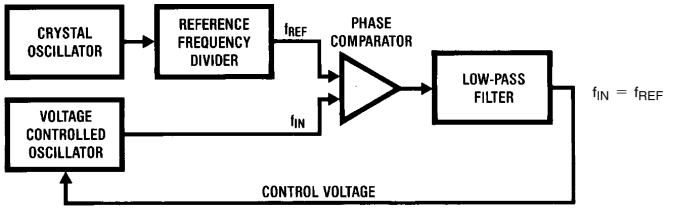

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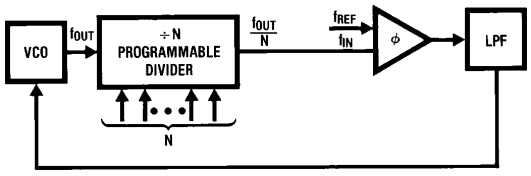
FIGURE 3. Basic Phase-Locked-Loop



$f_{IN} = f_{REF}$

$f_{IN} = \frac{f_{OUT}}{N}$

$\frac{f_{OUT}}{N} = f_{REF}$

$f_{OUT} = N \times f_{REF} \rightarrow f_{STEP}$
$= f_{REF}$

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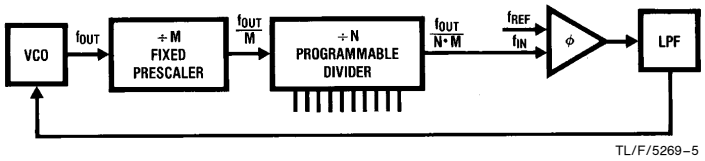
FIGURE 4. Basic PLL Frequency Synthesizer

In applications where the output frequency desired exceeds the maximum clock frequency of available programmable dividers, a common solution is to add a prescaler preceding the programmable divider, as shown in *Figure 5*. In this case $f_{OUT} = N (M \times f_{REF})$ and so the output frequency step size becomes $M \times f_{REF}$. So, while this technique allows higher frequency operation, it does so at the expense of either increased channel spacing for a given reference frequency, or decreased reference frequency if a specific channel spacing is required. This latter limitation is often undesirable as it can cause increased lock-on time, decreased scanning rates, and sidebands at undesirable frequencies.

Figure 6 shows the basic dual-modulus scheme. Here, a dual-modulus prescaler is substituted for the fixed prescaler and the modulus is controlled by programmable counters. The advantage to this approach is that the step size is again equal to the reference frequency while the prescaling still allows the programmable counters to operate at lower frequencies. As in the fixed prescale technique, only the prescaler needs to be high speed. The DS8906/7/8 prescale by 7/8 for AM and in a similar fashion by 63/64 in FM.



$f_{IN} = f_{REF}$

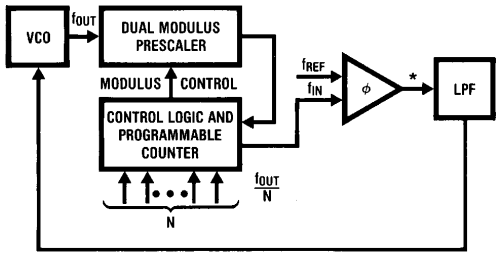
$f_{IN} = \frac{f_{OUT}}{N \times M}$

$\frac{f_{OUT}}{N \times M} = f_{REF}$

$f_{OUT} = (N \times M) f_{REF}$

$f_{OUT} = N (M \times f_{REF}) \rightarrow f_{STEP} = M \times f_{REF}$

FIGURE 5. PLL Frequency Synthesizer with Fixed Prescaler



$f_{IN} = \frac{f_{OUT}}{N} = f_{REF}$

$f_{OUT} = N \times f_{REF} \rightarrow f_{STEP} = f_{REF}$

*if $f_{REF} = f_{IN}$, then "tuned"
if $f_{REF} \neq f_{IN}$, then "not tuned"

FIGURE 6. Basic Dual-Modulus Frequency Synthesizer

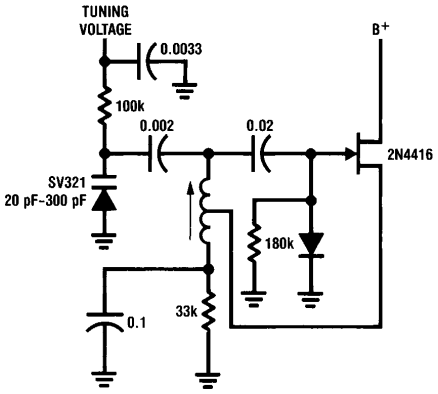
II. Application Hints

VOLTAGE CONTROLLED OSCILLATORS

In all radio and television applications, the voltage controlled oscillator (VCO) is a varactor tuned, LC type of circuit. The LC circuit is used over the various RC current controlled circuits because of their superior noise characteristics. *Figure 7* shows a collection of popular VCOs used in radio and television tuners. The AM VCO is a Hartley design chosen for wide tuning range. Commonly used varactors will show a capacitance change of 350 pF at 1V to 20 pF at 8V, which if used in a low capacitance oscillator circuit, can produce a tuning range approaching 3 to 1.

In the higher frequency ranges, above 50 MHz, Colpitts oscillators are used because stray circuit capacitance will be in parallel with desired feedback capacitance and not cause undesirable spurious resonances that might occur with the tapped coil Hartley design. The FM VCO shown is a grounded base design with feedback from collector to emitter. A UHF television oscillator is also shown. It too is a grounded base oscillator, but using a transmission line as the resonant element instead of a coil. The transmission line and tuning capacitors are arranged in π network which offers improved noise characteristics over a parallel tuned circuit. This circuit will tune over almost an octave.

Hartley Oscillator



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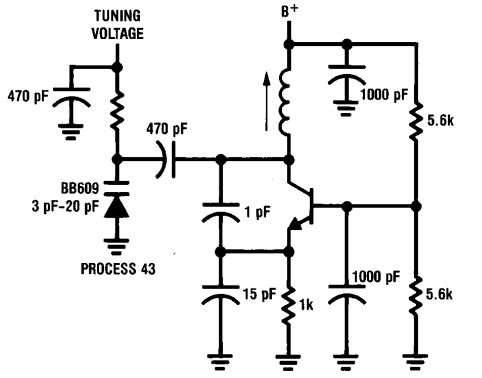
50 kHz ~ 15 MHz VCO
Tuning range ≅ 3:1

Colpitts Oscillator



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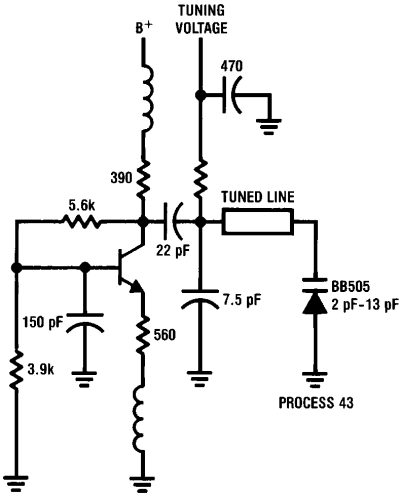
50 MHz ~ 300 MHz VCO
Tuning range ≅ 2:1

Colpitts Oscillator



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500 MHz ~ 1000 MHz VCO
Tuning range ≅ 1.8:1

FIGURE 7. Typical VCO Circuits (Typical Values Shown)

PLL LOOP FILTER CALCULATIONS

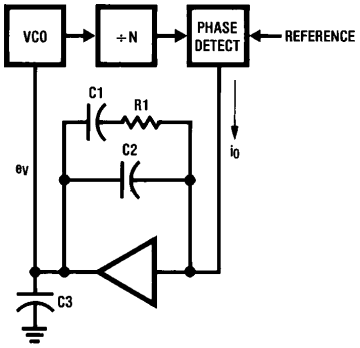
Andrzej Przedpelski, in two articles published in Electronic Design (#19, Sept. 13, 1978 and #10, May 10, 1978) explains how to calculate the three time constants associated with a third order type 2 loop which is typically used with the DS8906/7/8 series. *Figure 8* explains his method and shows a sample calculation. His articles illustrate how to calculate three time constants, and plot open loop gain and phase, and closed loop noise response.

It should be noted that VCO gain, K_V, is in terms of radians per second per volt, and phase detector gain, K_D, is in terms of amps per radian. The phase detector gain for the DS8906/7/8 series is $\pm I_{OUT}$ divided by 4π.

Figure 9 illustrates an example calculation of time constants, and a plot of open loop gain and phase based on the preceding analysis.

REFERENCES

1. Manassewitsch V., *"Frequency Synthesizers"* (Wiley, New York, 1976)
2. Rohde, A. L., *"Digital PLL Frequency Synthesizers"* (Prentice Hall, Englewood Cliffs, 1983)
3. Egan, W. F., *"Frequency Synthesis By Phase Lock"* (Wiley, New York, 1981)



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$T1 = R1C1$

$T1 = R1C2$

$$\frac{e_V}{I_O} = \frac{1+ST1}{SC1\,(1+ST2)}$$

$$G(S) = \frac{K_D K_V}{NS^2C1}\left(\frac{1+ST1}{1+ST2}\right)$$

$$T2 = \frac{1-\tan\phi\cos\phi}{\omega_O\cos\phi}$$

$$T1 = \frac{1}{\omega_O{}^2T2}$$

$$C1 = \frac{K_D K_V}{N\omega_O{}^2}\left(\frac{-\omega_O T1-1}{\omega_O T2+1}\right)$$

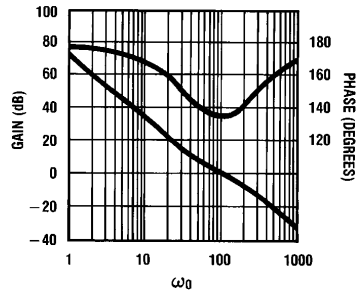
where θ = desired phase margin

ω_O = loop natural frequency

$\approx$ closed loop bandwidth

Note: DS8909 op amp required C3 $\approx$ 1000 pF for compensation.

FIGURE 8. Third Order Type 2 Loop



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VHF loop, running at 100 MHz, ref = 10 kHz

$K_V = 2.5$ MHz/V = 15.7 Mrad/sec/V

$$K_D = \frac{400\ \mu A}{4\pi} = 31.8\ \mu A/\text{radian}$$

$$N = \frac{100\text{ MHz}}{10\text{ kHz}} = 10{,}000,\ \omega_O = 2\pi \times 100\text{ Hz}$$

$\theta = 45°$ (desired phase margin)

$T2 = 6.6 \times 10^{-4}$ sec

$T1 = 3.84 \times 10^{-3}$ sec

$C1 = 0.3\ \mu F$

so $R1 = T1/C1 = 13\ k\Omega$

$C2 = T2/R1 = 0.05\ \mu F$

FIGURE 9. Example of Gain and Phase Calculation

DUAL-MODULUS COUNTING RANGE LIMITATIONS

- Minimum count limitations
- Maximum count limitations

The DS8906/7/8 series PLLs utilize a dual-modulus counting scheme internally based on a 63/64 prescale modulus in FM mode in order that all of the U.S. FM frequency assignments could be reached using a 25 kHz reference. The counter modulus N = 64A + B where B is the 6 least significant bits of N and A is the 7th and greater significant bits of N.

$$N = 64A + B$$
$$N = 64A + \overline{63} - B \quad (B = 63 - \overline{B})$$
$$1 + N = 64A + 63 + 1 - 64\overline{B} + 63\overline{B}$$
$$1 + N = 64(A + 1 - \overline{B}) + 63\overline{B}$$

The last equation is in the final form used internally by the DS8906/7/8. The equation indicates that, if N is loaded into the device, it will solve for N + 1.

The minimum continuous N modulus (code) the equation dictates should occur when A = $\overline{B}$. $\overline{B}$ maximum = 63 implies A = $\overline{62}$, B = 63 should be an illegal N + 1 code (N + 1 = 3969). However, because this is just inside the lower FM band limits, extra circuitry was added to enable this particular code's operation. The actual minimum N + 1 code for these PLLs thus becomes the case when A = 61, $\overline{B}$ = 61, N + 1 minimum = 3907. There are legitimate N + 1 codes below this 3907 value, however, they are not continuous. (i.e., Starting at 3907 and counting down, one additional code is in error every 63 codes. Thereafter, these erroneous codes are the cases where A < $\overline{B}$.) The sequence of illegal codes is shown in *Figure 10*.

Loaded Value of N	A	$\overline{B}$	Status	Actual Locked N + 1 Value
3906	61	61	OK	3907
3905	61	62	illegal	3907
3904	61	63	illegal	3907
3903	60	0	OK	3904
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3843	60	60	OK	3844
3842	60	61	illegal	3844
3841	60	62	illegal	3844
3840	60	63	illegal	3844
3839	59	0	OK	3840
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3780	59	59	OK	3781
3779	59	60	illegal	3781
3778	59	61	illegal	3781
3777	59	62	illegal	3781
3776	59	63	illegal	3781
3775	58	0	OK	3776
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3717	58	58	OK	3718
3716	58	59	illegal	3718
3715	58	59	illegal	3718
3714	58	60	illegal	3718
3713	58	61	illegal	3718
3712	58	63	illegal	3718
3711	57	0	OK	3712
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•

FIGURE 10. FM Mode Dual-Modulus Counting Below the Minimum Continuous N Code of 3906

Maximum code limits for these dual-modulus PLLs are determined by the N code bit length. The DS8906 and DS8908 have a 14-bit N counter allowing 16,383 counts. The DS8907 has a 13-bit N node length, allowing a maximum N count of 8,191. See *Figure 11* for table operating ranges of the DS8906, DS8907 and DS8908 PLLs.

CONCLUSION

The major application for the DS8906/7/8 PLLs are synthesizers for AM-FM radios, and have been widely accepted in the marketplace. *Figure 12* shows the block diagram of such a radio. In this application the following performance relating to the PLL tuning system is realized.

PLL Loop Bandwidth	300 Hz
Reference Frequency Sidebands	>60 dB
Signal-to-Noise Ratio	
AM: 30% modulation	>50 dB
FM: 22.5 kHz deviation	>55 dB
Switching Speed (one channel)	<1.5 ms

Product	Input	Ref (Hz)	f_{IN} (Hz)	
			Min*	Max
DS8906	AM	500	24.5k	8.193M
	FM	12.5k	48.8375M	120M
DS8907	AM	10k	490k	15M
	FM	25k	97.675M	120M
DS8908	AM	1k	49k	15M
		9k	441k	15M
		10k	490k	15M
		20k	980k	15M
	FM	1k	3.907M	15M
		9k	35.163M	120M
		10k	39.07M	120M
		20k	78.14M	120M

*The minimum frequency shown is obtained when the minimum continuous N code is utilized and it assumes the edge rates >20V/μs.

FIGURE 11. Product Operating Frequency Range

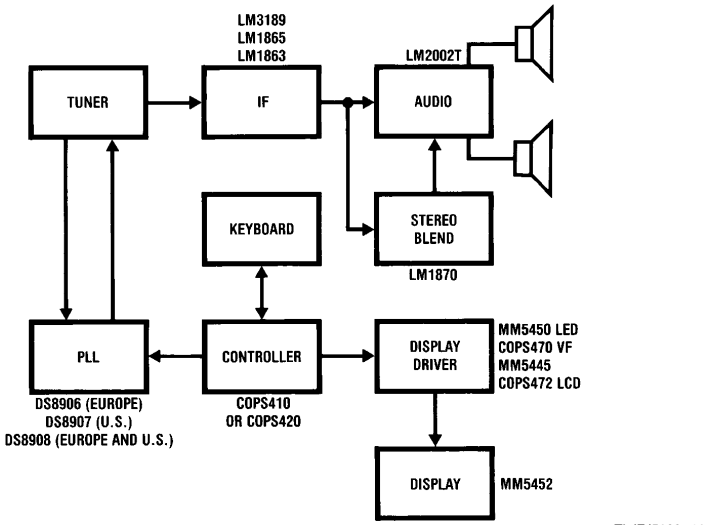

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FIGURE 12. AM-FM Digitally Tuned Radio System

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