A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8V Down (Part Two of Two)

Literature Number: SNAA104

Technology Edge

Note: This is Part Two of Two (Continued from June 2001 Edition)

A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8V Down to 2.2V (Robert C. Taft and Maria Rosaria Tursi, Data Conversion Systems)

Abstract-A 100-MS/s 8-b CMOS analog-to-digital converter (ADC) designed for very low supply voltage and power dissipation is presented. This single-ended-input ADC is based on the unified two-step subranging architecture, which processes the coarse and fine decisions in identical signal paths to maximize their matching. However, to minimize power and area, the coarse-to-fine overlap correction has been aggressively reduced to only one LSB. The ADC incorporates five established design techniques to maximize performance: bottom-plate sampling, distributed sampling, auto-zeroing, interpolation, and interleaving. Very low voltage operation required for a general purpose ADC was obtained with four additional and new circuit techniques. These are a dual-gain first-stage amplifier, differential T-gate boosting, a supply independent delay generator, and a digital delay-locked-loop controlled output driver. For a clock rate of 100 MS/s, 7.0 (7.3) effective bits for a 50 MHz (10 MHz) input are maintained from 3.8 V down to 2.2 V. At 2.2 V, this 100-MS/s converter dissipates 75 mW plus 9 mW for the reference ladder. For a typical supply of 2.7 V, it consumes just 1 mW per MS/s over the 10-160-MS/s clock frequency range. Differential nonlinearity below 0.5 LSB is maintained from 2.7 V down to 2.2 V, and it degrades only slightly to 0.8 LSB at 3.8-V supply. The converter is implemented in a 0.35-mm CMOS process, with double-poly capacitors and no low-threshold devices.

Index Terms-Analog-to-digital converters, CMOS analog integrated circuits, Nyquist converters, subranging A/D converters, switched capacitor circuits, two-step A/D converters.

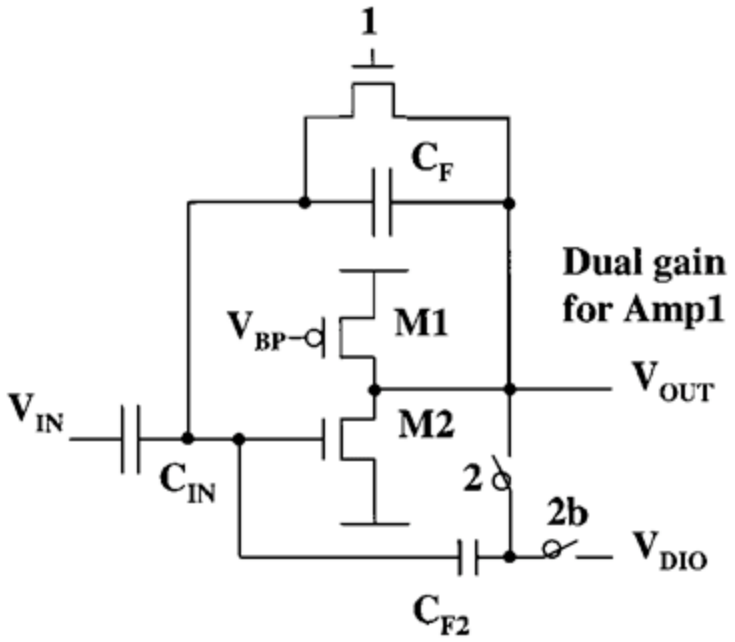

Fig. 5. Amp 1, a common-source nMOS , M2, with a pMOS current load, M1. Shown is feedback capacitor C_F in addition to input capacitor, C_{IN}. During phase 2, C_{F2} is used to reduce the gain of the amplifier, to enhance its linearity and bandwidth.

V. DUAL-GAIN AMP1

Interpolation between largely varying input voltages at the input of amp 2 stress the linearity requirements of amp 1 during the coarse amplify in phase 2. Thus, errors can exceed one LSB for the matching of the coarse- and fine-compare results, especially at low supply. Since this exceeds the error budget, the lin-earity of amp 1 and amp 2 during coarse amplify was improved. Making amp 1 dual-gain by switching in a second feedback capacitor during phase 2, as shown in Fig. 5, greatly alleviates this constraint. The lower gain during coarse amplify results in not only better linearity, but also higher bandwidth and faster settling. During fine amplify, the higher gain of amp 1 is beneficial in reducing all offset errors of amp 2, amp 3, and the comparator. As long as the coarse-compare is within one LSB of the correct answer, the fine-compare fully determines the performance of the converter. Thus, since the fine amplifiers have a lower bandwidth and need accurate results, the settling time for the fine-amplify phase needed to be extended.

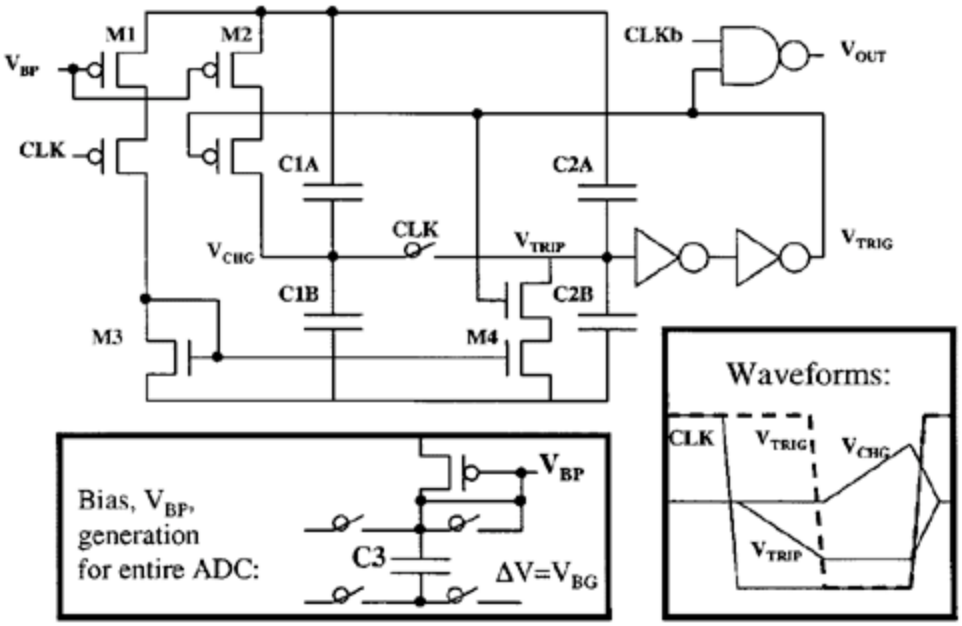

Fig. 6. Process, temperature, and supply independent delay generator used to generate a clock 1/4 period, to extend the length of phase 4. Key waveforms are plotted, and an approximate description of the bias generator for V_{BP} is given.

VI. NON-DLL CLOCK-PERIOD DIVIDER

The fine amplify phase 4 is extended at the expense of phase 3, since the comparators regenerate very quickly. Even for the worst case, the comparators need only one-half of the clock high time for phase 3. A delay generator to halve the clock high time, preferably without the complexity of a delay-locked loop (DLL), was required. It needed to be not only process and supply insensitive, but also have the ability to adjust to large variations in ADC clock frequency. In Fig. 6, a very simple and robust period divider is shown along with the key waveforms required to create half a clock s low time (CLK is inverted as implemented). All capacitors are of equal value, and are connected between the supply rails for supply rejection. M4 discharges C2 when CLK goes low until it reaches the inverter trip point. At this point, V_{TRIG}, the signal used to halve the CLK low time, is generated. For the remainder of CLK s low time, M2 charges up C1, with a charge transfer occurring from C1 to C2 when CLK goes high. This charge transfer returns C2 to its original voltage in preparation for the next CLK low. The delay is independent of the inverter trip point, depending only on the ratio of M1 to M2. With M1 and M2 equal, the CLK low time is halved.

The circuit has two vulnerabilities. First, if M1 exceeds three times the strength of M2, V_{TRIG} will not lock and this will create large jitter. For all other ratios the circuit locks quickly and remains stable. Second, the voltage V_{TRIP} could saturate due to variations in bias level V_{BP}. This second problem is avoided by design, since the bias for the entire ADC is generated by a bandgap voltage applied across a capacitor matching the one used in the delay cell. The approximate schematic is given at the bottom of Fig. 6. Additional benefits of using this "switching" current generator are an ADC that reduces its quiescent power when operated below its maximum conversion rate and a more tightly controlled current. Over process, temperature, and voltage variations, resistors in CMOS processes generally have more variation in value than capacitors.

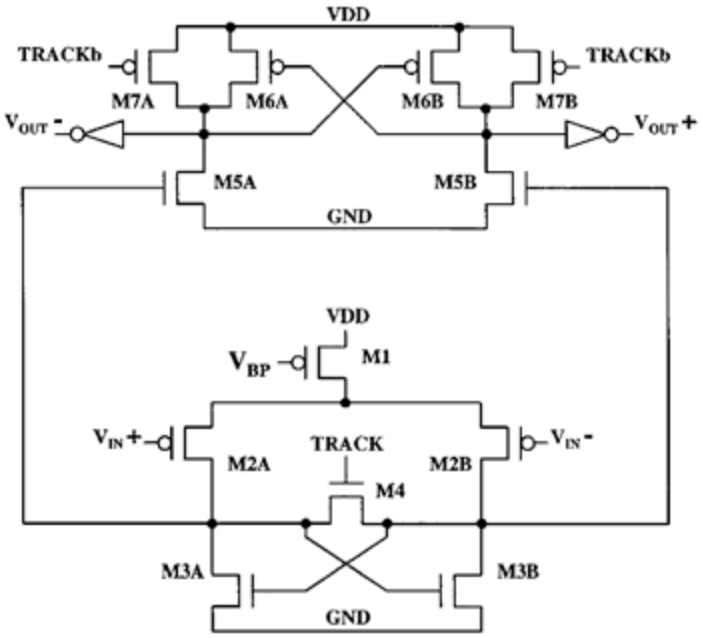

Fig. 7. The low-voltage low-offset comparator consists of two stages, the quiescent regenerator (below) and the dynamic level shifter (above).

VII. LOW-VOLTAGE LOW-OFFSET COMPARATOR

One advantage of the 1.5-b-per-stage pipe architecture previously described in the introduction is that the comparator need not be very accurate. Later conversions can compensate for comparator offset errors made earlier in the pipe. For this and all flash-like converters, however, no such recovery exists, and a low-offset comparator is crucial. Fig. 7 shows a two-stage comparator, consisting of a quiescent regenerator followed by a dynamic level shifter. It is based on that of [8] and [9], but is lower voltage because the two-stage approach reduces the amount of device stacking. In addition, unlike in [8] and [9], clock signals TRACK and TRACKb can be simultaneous, reducing the complexity of the clock generation. Although the input and reference ladder are single-ended, the analog channel is actually pseudodifferential, with a reference channel consisting of amp 1, amp 2, and amp 3, which is not shown in Fig. 4. The input to the reference channel is a quiet ground, and the output of amp 3 is applied to the negative input of the regenerator, with the signal channel applied to the positive input. Input pair M2A and M2B, and cross-coupled M3A and M3B are large to minimize the offset of the regenerator. Further, M4 is small to reduce the dynamic offset errors resulting from an uneven TRACK clock coupling into both halves of the regenerator. Although the bias current set by V_{BP} limits the slew-rate of the regenerator stage, only a small amount of regeneration is required to activate the level shifter, which rapidly generates CMOS logic levels.

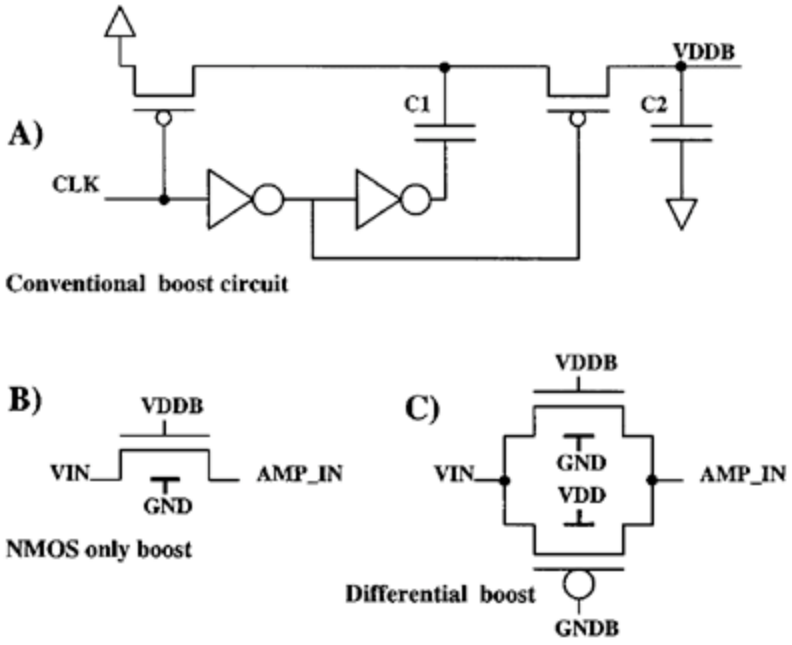

Fig. 8. (a) Conventional boost circuit. (b) nMOS-only T-gate. (c) Differential T-gate boosting with double back-bias effect used for this ADC.

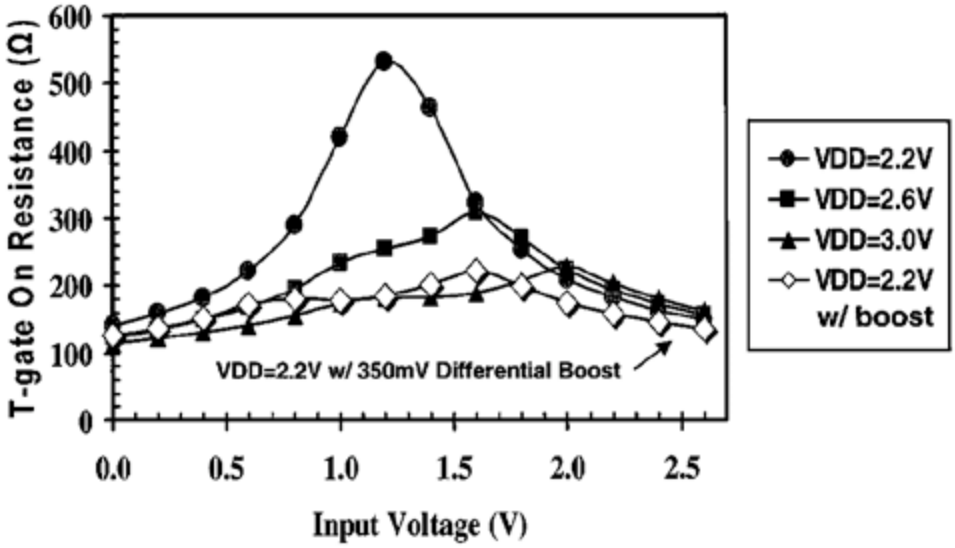

Fig. 9. Simulated T-gate on-resistance versus V_{IN} for three supply voltages, 2.2, 2.6, and 3.0V. Note that the inclusion of a 350-mV differential boost for V_{DD}=2.2V reduces the maximum R_{ON} and absolute R_{ON} variation more effectively than an 800-mV increase in supply voltage.

VIII. DIFFERENTIAL T-GATE BOOSTING

Fig. 8(a) shows a conventional boost generator, which can be used with an nMOS-only T-gate, Fig.

8(b). The nMOS-only transmission gate has been used with a dynamic boost voltage to obtain a constant V_{GS}. This minimizes the variation of the input resistance, minimizing the distortion at high input frequencies.

The problem with the nMOS-only approach is the increased voltage stress, since the maximum supply and operating supply are converging for aggressive CMOS technologies. For an input voltage range which can lie anywhere between the supply rails, the nMOS-only approach is limited. Furthermore, the dynamic boost circuit is not well suited for distributed sampling.

The new approach is shown in Fig. 8(c). It uses a very small 350-mV differential boost voltages VDDB and GNDB. This requires a second, complementary boost circuit, as shown in Fig. 8(a), to generate the -350 mV below-ground boost voltage GNDB. Note that this approach minimizes the technology stress, since no transistor has both VDDB and GNDB applied to it. In addition, it has the added benefit of the body effect of the T-gate transistors, e.g., for the T-gate pMOS, a lower hard supply on the n-well results in a lower V_{BS}, therefore a lower V_{TH}. The same applies to the T-gate nMOS. Thus, at V_{DD} = 2.2V, the reduction in T-gate on-resistance obtained with only the addition of 350-mV differential voltage stress is equivalent to increasing the supply voltage 800 mV without the use of differential T-gate boosting; see Fig. 9.

Because of the low controlled differential boost voltages of +/-350 mV, no special precaution or circuitry was required for routing these levels to the V_{IN} T-gates. Therefore, these same boosted logic levels were used for all critical T-gates, including those in the analog MUX. This allowed the use of smaller T-gates for the same pass resistance, and therefore a substantial reduction in parasitic device capacitance.

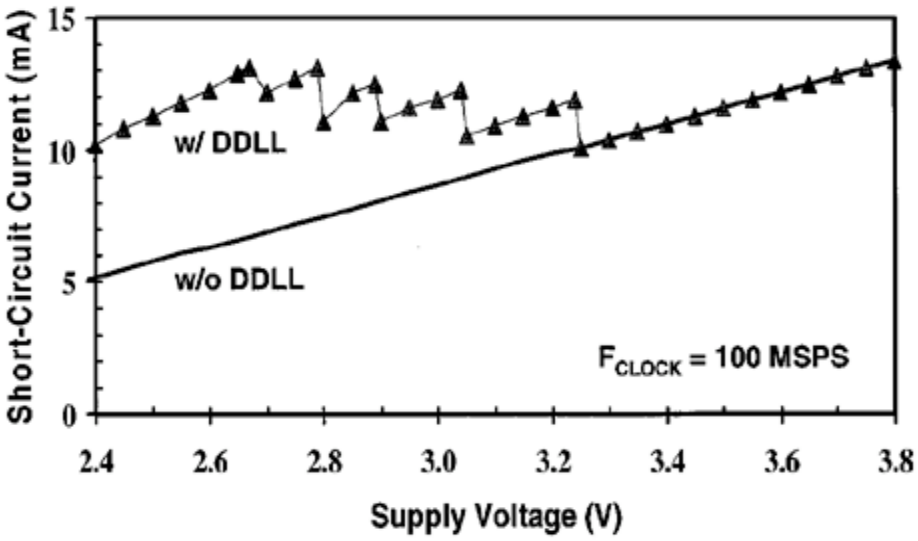

Fig. 10. Short-circuit output driver current versus supply with and without the digital delay lock-loop (DDLL) control active.

IX. DIGITAL DELAY-LOCK-LOOP OUTPUT DRIVER

The variations in process and supply voltage present special challenges for the ADCs digital output driver design. At 100 MHz, capture of the ADCs digital output is not trivial. The output drivers must be strong enough to drive reasonable board loads (10 pF) in slow corners. In fast corners, however, they must be sufficiently weak to minimize digital noise from coupling back into the analog circuit. Sophisticated approaches using current source output drivers were rejected in this design because of the large required layout area. The approach here was to vary the output driver

strength from 3 to 11 parallel fingers, set by a DLL with a replica scaled output driver and an internal load capacitor of 2 pF. The resulting reduction in output driver strength variation at 100 MHz is nearly 3 , as seen by plotting short-circuit current versus supply voltage, see Fig. 10. Note that not all transitions between m = 3 and 11 are seen, due to the need to lock the circuit on specific m values.

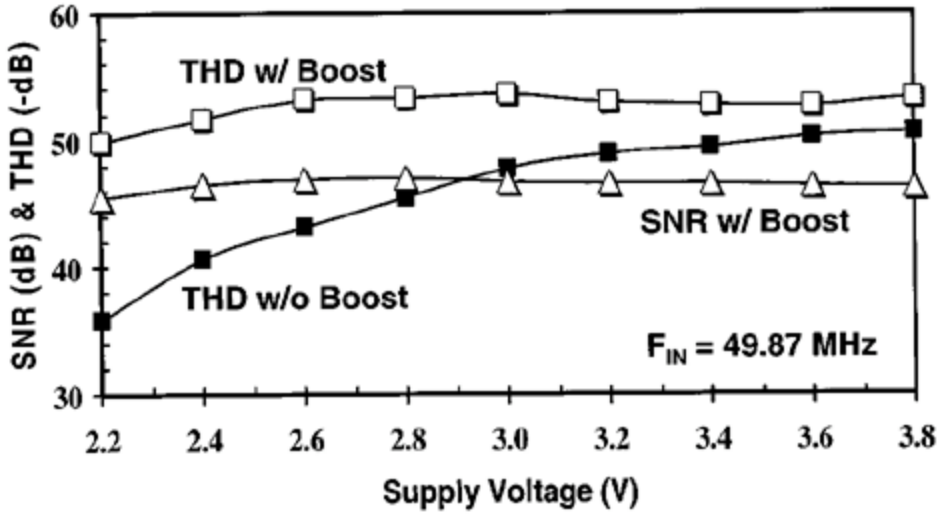

Fig. 11. Total harmonic distortion and signal-to-noise ratio at Nyquist versus supply voltage. As a comparison, the measured THD without using boosted supplies has been plotted.

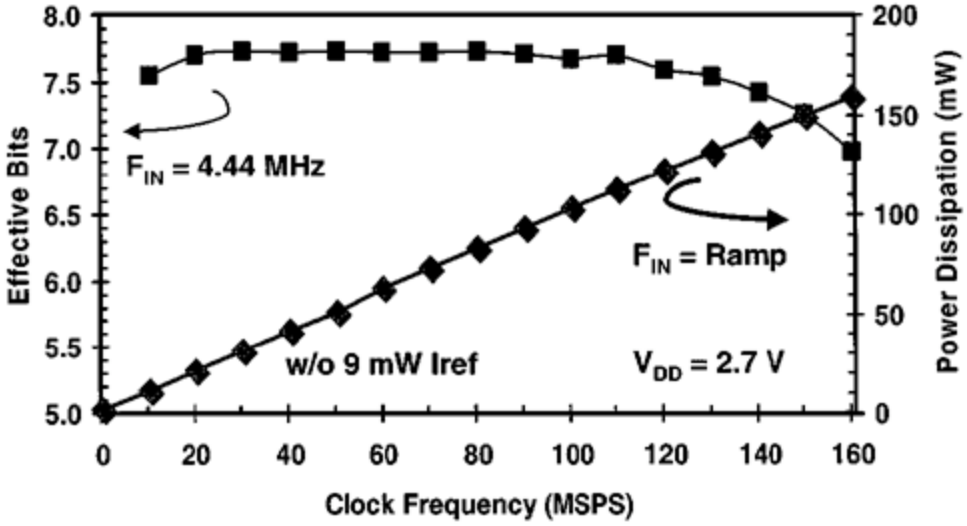

Fig. 12. Signal-to-noise and distortion (SINAD) expressed in effective bits, and total power dissipation for a ramp input, both versus clock frequency. The resistor reference power was omitted to show that the ADCs combined digital and analog power is proportional to F_{CLK}, at 1 mW/MHz. At F_{CLK} = 160MS/s, 7.0 effective bits are still maintained.

X. EXPERIMENTAL RESULTS

Fig. 11 shows the total harmonic distortion (THD) and signal-to-noise ratio (SNR) at Nyquist versus supply voltage, from 3.8 V down to 2.2 V. A V_{DD} of 3.8 V just exceeds the maximum operating supply, especially with the addition of the 350-mV boost. However, it demonstrates the robustness of the circuit blocks. The effectiveness of the differential boost circuit is demonstrated by plotting the measured THD with the boost voltages replaced by the supplies. The effect of the switching bandgap current generator on power dissipation versus clock frequency is shown in Fig. 12. The power, at 1 mW per MS/s, is for a ramp input, and therefore does not include significant output driver current. This latter component is dominated by the capacitive load of the test board. Shown also is the signal-to-noise and distortion (SINAD) versus clock frequency for a video 4.44MHz - 0.5dBFS input. For converter rates of 10-160 MS/s, 7.0 effective bits are maintained.

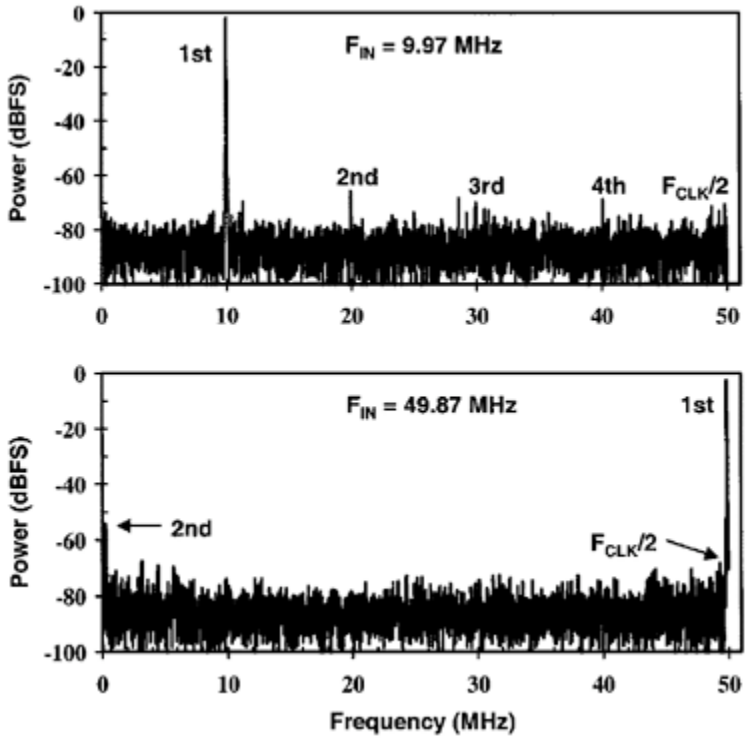

Fig. 13. FFT spectrum at 100 MS/s and 2.7 V, for F_{IN} = 9.97 MHz (above) and F_{IN} = 49.87 MHz (below). The spectrum is clean, and shows nearly no $F_{CLK}/2$ component or F_{IN} with F_{CLK} mixing even at Nyquist.

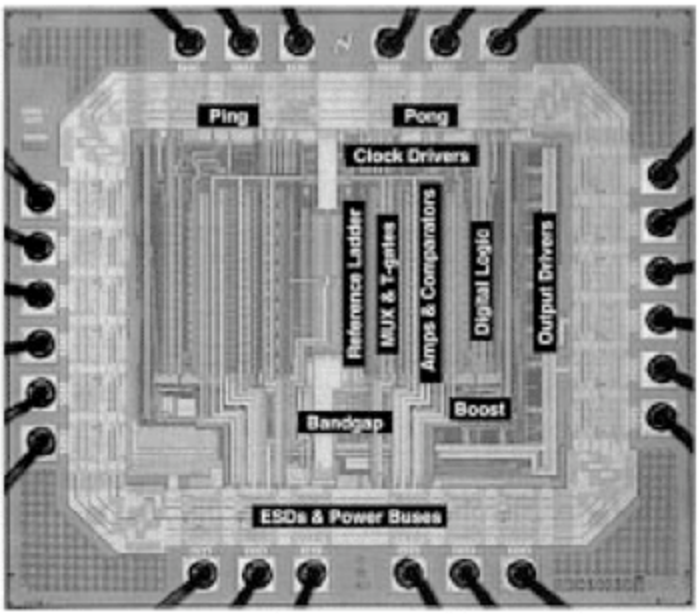

Fig. 14. Die photograph showing the location of key circuit blocks. Note the symmetry about the central polysilicon reference ladder, shared by both interleaved analog channels.

Spectrums for two different input frequencies, 10 and 50 MHz, are shown in Fig. 13. In both cases, no $F_{CLK}/2$ components or with mixing is seen. This results from the good gain, offset, and timing matching of the two interleaved channels. For the 10-MHz spectrum, note the excellent third harmonic distortion of 67 dB, which plays an important role in communications. The second harmonic dominates due to the use a single-ended front end. A die photograph showing the location of key circuit blocks is shown in Fig. 14. The polysilicon reference ladder, in the center, is shared by both interleaved analog channels, indicated as "Ping" and "Pong." The digital circuits for the one LSB of MSB-to-LSB mismatch correction are indicated. Shown also are the boost capacitors used to the 350-mV differential boost, and the output drivers complete with their digital DLL control unit.

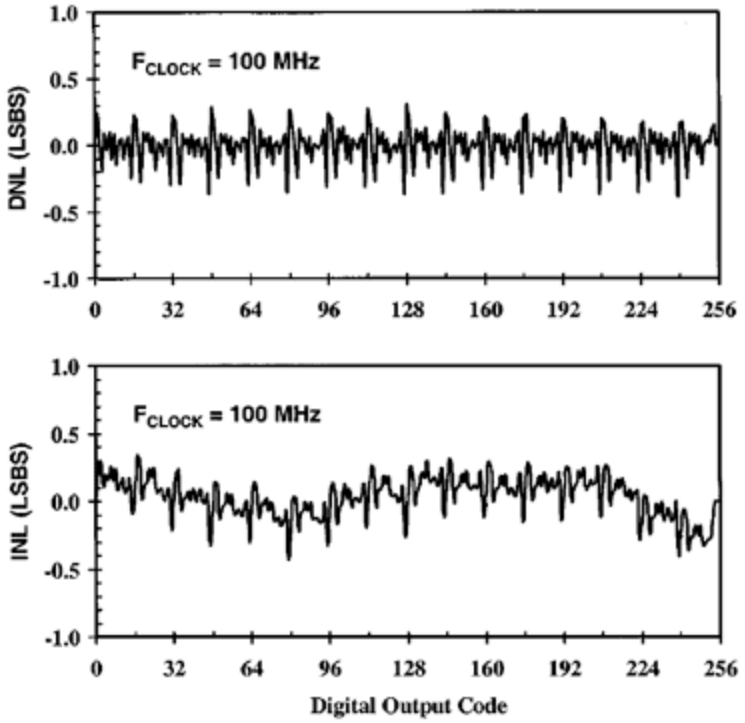

Fig. 15. Differential nonlinearity (above) and integral nonlinearity (below) at 2.7 V. The subranging architecture results in a small modulo 2 ^ (N/2) = 16 signature, due to the cyclical use of the 2 ^ (N/2) comparators to evaluate all 2 ^ N codes.

TABLE I
ADC PERFORMANCE VERSUS SUPPLY VOLTAGE FROM 2.2 V UP TO 3.8 V

VDD	2.2 V	2.7 V	3.8 V
ADC Clock (MSPS)	100	100	100
Power w/o Ref. (mW)	75.2	108.9	167.6
Ladder Power (mW)	9.1	9.1	9.1
Max DNL (LSB)	-0.43/+0.40	-0.39/+0.30	-0.51/+0.80
Max INL (LSB)	-0.60/+0.41	-0.43/+0.34	-0.58/+0.59
THD (dB) @Fin=10MHz	-51.1	-56.7	-56.7
SNR (dB)	47.4	48.2	46.7
Eff._Bits	7.3	7.6	7.4
THD (dB) @Fin=50MHz	-49.4	-55.8	-52.5
SNR (dB)	45.2	45.9	46.4
Eff._Bits	7.0	7.3	7.3
Latency (cycles)	2.5	2.5	2.5
Ladder Reference; V_{RB} to V_{RT} (V)	0.3 to 1.9	0.3 to 1.9	0.3 to 1.9
Active area	0.9 sq. mm		
Die Area	2.6 sq. mm		
Technology	Lpoly=0.4um CMOS (2-poly,3-metal) NO low Vt devices		

Fig. 15 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) errors, again at 2.7

V. Both the maximum DNL and INL are about +/-0.4 LSB. Although the intent was to maintain parametric performance over a wide range of supply voltages, the ADC was optimized for a 2.7-V supply. Not all circuit blocks improve with increasing supply voltage. This is particularly true for DNL, where the contribution of charge-switch injection variation during the sampling phase cannot be auto-zeroed. The larger the supply, the larger the gate voltage above threshold for the sampling nMOS of Figs. 3 and 4, and the larger the injected charge and injected charge variation during sampling. This DNL effect is seen in Table I, which summarizes the ADC parametric results for three supply voltages. The converter actually maintains a DNL of +/-0.5 LSB down to 2.0 V, at which point its power consumption is only 60 mW.

ACKNOWLEDGMENT

The authors wish to thank A. Glenny, D. Archer, B. Brandt, D. Boisvert, J. Lutsky, F. Bowman, J. Margolycz, and R. Cullen for technical assistance and discussions. The authors are very grateful to S. Dacy for proofreading and correcting early drafts. They are also very grateful for the technical support of DCS and the NSME, and for the management support of P. Holloway and P. Tucci.

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