

ADC12EU050

Continuous-Time Sigma-Delta A/D Converters



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Continuous-Time Sigma-Delta A/D Converters

— By Scott Kulchyski, Engineer, Ph. D.

A/D Converters (ADCs) perform two basic, fundamental operations: discretization in time and discretization in amplitude. The two functions are shown conceptually in *Figure 1*, though the actual ADC may not be structure as such [1].

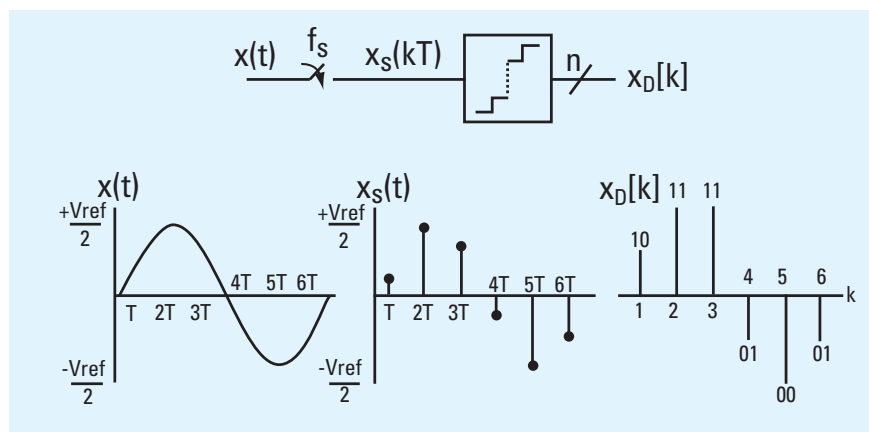


Figure 1: Analog-to-Digital Conversion

The first operation of the ADC is to discretize in time, or sample, the continually time-varying input analog signal. The input signal is typically sampled at uniformly spaced times at a frequency of f_s , and the samples are thus separated by a period $T_s = 1/f_s$. Once the input signal is sampled, the resultant signal exists only as impulses at the sampling interval, kT_s . However, this sampled signal is still able to assume an infinite range of values, and therefore cannot be represented precisely in a digital form.

The second function of the ADC is to discretize the sampled signal in amplitude. That is, the ADC approximates the amplitude of each sample with one of a finite number of possible values. Because the output of the ADC can take on only a finite number of possible values, the amplitude of each sample can be represented by a digital code whose bit length determines the total number of possible converter outputs. The finite number of output values in

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a converter introduces error into the digital representation of the analog input. This so-called quantization error limits the resolution of the converter.

Continuous-Time Sigma-Delta (CT $\Sigma\Delta$) ADCs

National's ADC12EU050 is the industry's first production-ready CT $\Sigma\Delta$ ADC. The ADC12EU050 offers performance improvement both because of the inherent advantages of CT $\Sigma\Delta$ technology versus sampled-input ADCs, such as pipeline and traditional, Discrete-Time (DT) $\Sigma\Delta$ ADCs, and also because of additional circuitry that National has integrated on-chip.

Lower Power

The most significant benefit of the CT $\Sigma\Delta$ architecture is its low power consumption relative to sampled-input ADCs in the high-resolution, sub-100 MSPS application space. A common way to compare the performance of ADCs is an energy Figure Of Merit (FOM) which typically measures the ratio of the overall power of the ADC to the resolution and bandwidth of its output. Aided by the inherent efficiency advantage of CT $\Sigma\Delta$ technology, the ADC12EU050 provides excellent performance at extremely low power, yielding an outstanding FOM.

The power advantage of a CT $\Sigma\Delta$ implementation arises because of the internal circuitry. In any sampled-input Switched-Capacitor (SC) circuit – including both pipeline and DT $\Sigma\Delta$ ADCs – the internal amplifiers must settle to within some target resolution each period. This places significant speed constraints on the internal amplifiers, increasing the power consumption [2] and limiting the maximum achievable sampling rate.

In a CT $\Sigma\Delta$ with CT feedback, because the amplifier output never attempts to switch its output voltage instantaneously, there is no output settling required and, hence the amplifier speed constraints are relaxed [2]. Although an exact comparison is difficult, the SC nature of a sampled-input ADC does necessitate higher-speed amplifiers than does a CT $\Sigma\Delta$ implementation, leading to higher power consumption

for a pipeline or DT $\Sigma\Delta$ ADC in general. The lack of a need for high-speed settling in CT $\Sigma\Delta$ ADCs is also the reason they are able to achieve higher sampling rates than traditional DT $\Sigma\Delta$ ADCs in a given technology.

Low power, high energy efficiency operation is obviously important for any system but portable devices especially benefit since reduced power extends battery life and reduces heat dissipation, which is particularly important for handheld applications including handheld ultrasound systems. The 1.2-V power supply of the ADC12EU050 also enables single-battery powered operation.

Anti-Aliasing Filtering

The CT $\Sigma\Delta$ ADC architecture eliminates the need for stringent input filtering because of its inherent anti-aliasing filtering. In the ADC12EU050, many of the performance characteristics of the Anti-Aliasing Filter (AAF) are set in the digital domain, allowing for a very high level of passband flatness and steep roll-off (high effective order).

The anti-aliasing performance of the CT $\Sigma\Delta$ is a result of its implementation as both a $\Sigma\Delta$ modulator and a CT circuit. In a Nyquist-rate ADC, such as a pipeline ADC, a high-order external AAF must be employed before the ADC to prevent signals around multiples of the output sampling rate from aliasing down in-band. Often a pipeline ADC is oversampled to reduce the range of frequencies that may alias down in-band, thereby lowering demands on an external AAF. However, such oversampling wastes the Nyquist bandwidth and increases the demands on subsequent digital circuitry, increasing system power. In contrast, the over-sampling and subsequent decimation filtering of the modulator output in a $\Sigma\Delta$ ADC (either CT or DT) results in a very sharp roll-off lowpass filter with a cutoff frequency at half the ADC output rate.

However, in addition to the inherent benefit of $\Sigma\Delta$ architectures, the CT offers an additional benefit, even over DT $\Sigma\Delta$ ADCs. Because the CT $\Sigma\Delta$ ADC samples at the output of the forward loop filter, the

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signal is first lowpass filtered by the loop before sampling, which attenuates signals around the modulator loop sampling rate (Mf_s) that can alias down in-band. Furthermore, because these aliased signals are then injected at the input of the internal quantizer, they are noise-shaped by the loop in the same manner quantization noise is shaped [1]. These two effects enable the CT $\Sigma\Delta$ to offer significant anti-aliasing filtering versus the DT $\Sigma\Delta$ in addition to the benefits offered by over-sampling and digital filtering versus a Nyquist-rate design. *Figure 2* summarizes the anti-aliasing performance of CT $\Sigma\Delta$ ADCs versus pipeline ADCs.

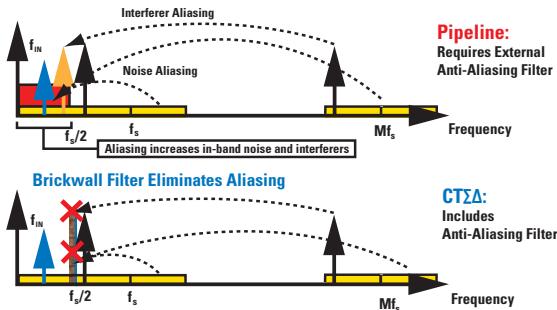


Figure 2. Anti-Aliasing Performance of CT $\Sigma\Delta$ and Pipeline ADCs

Quiet, Easy-to-Drive Input

The CT $\Sigma\Delta$ ADC also offers a much quieter input than a sampled-input ADC because of the CT nature of the internal circuitry. In a sampled-input ADC, such as a pipeline or traditional DT $\Sigma\Delta$ ADC, the input stage consists of a switched capacitor that is usually large to reduce the overall thermal noise of the ADC. Driving this large switching capacitor is difficult, especially in a DT $\Sigma\Delta$ whose internal modulator is sampling at several times the output data rate. In addition, the large switching noise from such inputs can couple into the system, reducing the overall system performance. The input voltages that can be applied to a switched-capacitor input are also limited because of the gate-source voltage of the input sampling switches. As opposed to a SC sampled input, CT $\Sigma\Delta$ technology instead presents a constant, resistive input, as illustrated in *Figure 3*.

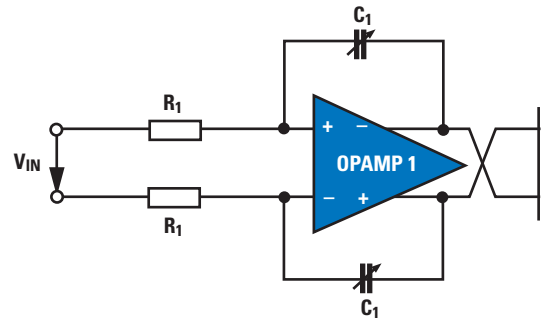


Figure 3. Model of the CT $\Sigma\Delta$ ADC Input

Because the input of a CT $\Sigma\Delta$ is not sampled, there are no switching capacitors and it is easier to drive the input, allowing for the use of cheaper, lower-power driving circuits. In addition, the lack of input switching noise will reduce noise coupling into the system, improving its overall performance. Finally, without any switches at the input to restrict the input voltage swing, the allowable input voltage range can be higher than for a SC sampled-input ADC; indeed, the input voltage can even exceed the supply rails.

Low-Jitter PLL Provides Accurate Sample Clock

A low-jitter sampling clock is crucial in all high-speed, high resolution data conversion systems to realize the full resolution of an ADC. The modulator over-sampling clock in National's ADC12EU050 drives the quantizer of the internal $\Sigma\Delta$ loop. This clock is provided by an on-chip clock conditioner, comprising a PLL and VCO. The high-performance PLL uses an on-chip LC-tuned circuit to create a high-Q resonator. This on-chip clock circuit multiplies up the frequency and provides low-jitter sampling edges to the modulator loop, allowing for the benefits of CT $\Sigma\Delta$ ADCs to be realized without requiring a high-performance, high-cost external clock source. The system designer needs simply to provide a moderate-quality, low-cost crystal at the desired output sampling rate (40 to 50 MSPS), and the ADC12EU050's on-chip clock circuitry takes care of the rest.

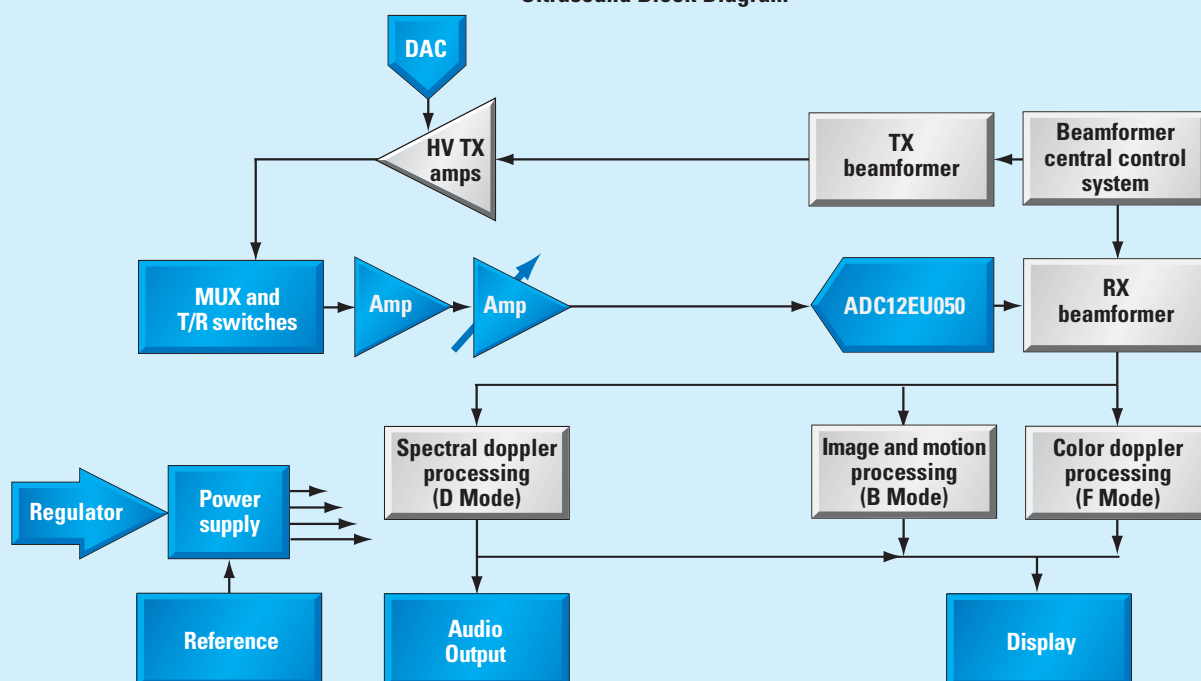
PowerWise® High-Speed Continuous-Time Sigma-Delta A/D Converter

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Sigma-Delta A/D Converter Provides Anti-Aliasing Filter and On-Chip PLL+VCO

Ultrasound Block Diagram



ADC12EU050 Features

- 8-channel, 12-bit, 40 to 50 MSPS ADC
- Ultra-low power consumption: 350 mW
- Consumes 44 mW/channel at 50 MSPS
- Alias-free sample bandwidth up to 25 MHz
- On-chip PLL+VCO
- 68 dB Signal-to-Noise and Distortion (SINAD)
- 70 dBFS Signal-to-Noise Ratio (SNR)
- Instant Overload Recovery (IOR)
- LLP-68 packaging

Applications

Medical imaging, industrial imaging, communication, test & measurement, and portable systems

For FREE samples, datasheets, and more, visit:

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A further advantage of the on-chip precision clock is that it can be routed to external circuits and used as a system reference clock for other time-critical blocks in the system, potentially eliminating the extra cost of a low-jitter source and saving both design effort and board area.

Instant Overload Recovery

Because the $\Sigma\Delta$ modulator is a feedback loop, it is susceptible to overloading in the presence of large input signals. In a typical $\Sigma\Delta$ modulator, such overloading may require the loop to be reset, losing data previously stored in the loop and causing a large glitch in the ADC output. Instead of resetting the loop, the modulator can be allowed to continue operation, allowing the overload condition to simply work its way out of the loop—but waiting to clear the overload condition can require several clock cycles, during which time the ADC output data is corrupted. The ADC12EU050 includes circuitry that recovers immediately from an overload condition. When this Instant Overload Recovery (IOR) circuitry is enabled, the ADC maintains signal integrity in the event of an input overload condition, allowing it to recover faster than even a pipeline ADC.

Technology Scaling

Finally, CT $\Sigma\Delta$ technology is capable of scaling well with future technologies, ensuring a lengthy presence in the ADC marketplace. Because the sampling operation in a CT $\Sigma\Delta$ occurs at the output of the loop filter, the performance impact due to errors in the sampling operation will be greatly reduced. In sampled-input ADCs such as pipeline or DT $\Sigma\Delta$ ADCs, the sampling occurs at the ADC input and therefore, any sampling errors are significant. It is for this reason that CT $\Sigma\Delta$ ADCs are more amenable to future, scaled CMOS processes. Non-idealities in the sampling circuit caused by reduced overdrive, leakage, or other effects in future processes will impact pipeline, DT $\Sigma\Delta$, and other sampled-input ADCs much more than CT $\Sigma\Delta$ ADCs.

National's New CT $\Sigma\Delta$ ADC

The PowerWise® ADC12EU050 12-bit, octal CT $\Sigma\Delta$ ADC offers an alias-free sample bandwidth of 20 to 25 MHz and a conversion rate of 40 MSPS to 50 MSPS. The device features 68 dB of signal-to-noise and distortion (SINAD) and a signal-to-noise ratio (SNR) of 70 dB full scale (dBFS). Operating from a 1.2V supply, it consumes 44 mW per channel at 50 MSPS for a total power consumption of only 350 mW, 30% lower than currently available competitive pipeline products.

The ADC12EU050 reduces interconnection complexity by using programmable serialized outputs, which offer industry-standard low-voltage differential signaling (LVDS) and scalable low voltage signaling (SLVS) modes. The ADC12EU050 operates over the -40°C to 85°C temperature range and is supplied in a 68-pin LLP® package.

Conclusion

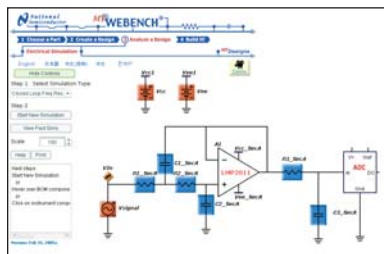
National's advanced ADC12EU050 ADC solution finally realizes the leap in performance that CT $\Sigma\Delta$ ADCs have promised for more than 40 years, successfully migrating the technology from the research lab to the production line. The power dissipation is 30% lower than for any of the competitive pipeline products and it offers 12-bit resolution at an output rate several times higher than the fastest currently available DT $\Sigma\Delta$ ADCs.

The CT $\Sigma\Delta$ technology on which the ADC12EU050 is based also offers significant inherent anti-aliasing filtering and provides a low-noise, easy-to-drive input stage. The ADC12EU050 includes an on-chip clock conditioner that eliminates the need for a high-performance, expensive clock. Finally, the ADC12EU050 avoids the hazards of input overload present in ADCs by offering a means for recovering immediately from an input overload event. ■

For more information on Continuous-Time Sigma-Delta A/D Converters, visit: www.national.com/adc

[1] S. D. Kulchyski, "Continuous-Time $\Sigma\Delta$ Modulation for High-Resolution, Broadband A/D Conversion," Ph.D. dissertation, Stanford University, March 2007.
[2] E. van der Zwan and E. C. Dijkmans, "A 0.2 mW CMOS $\Sigma\Delta$ modulator for speech coding with 80 dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1873-1880, December 1996.

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