Application Note

How to Use Adaptive Equalization for TDP1204 and TMDS1204

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ABSTRACT

The ability to adaptively equalize provides a robust solution for two communicating devices that need to equalize a signal in various channel conditions. The TDP1204 and TMDS1204 redrivers both implement adaptive equalization (AEQ). This application note provides procedures on how to use AEQ on the TDP1204 and TMDS1204 devices.

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Trademarks

1 Introduction

The ability to adaptively equalize a signal provides an ability to provide a system with a robust communications solution between a transmitting node and a receiving node. Many customer applications require a robust solution such as AEQ since the end users may require the ability to change cable length, temperature, data rates or other channel characteristics during communication events. Historically, the retimer devices implement AEQ algorithm, but retimers provide a less cost-effective solution than redrivers. Redriver products such as the TDP1204 and TMDS1204 offer AEQ functionality with a better cost efficiency. The TDP1204 and TMDS1204 are both redrivers that support AEQ functionality for HDMI™ 2.1 fixed rate link mode. The rest of the document discusses how to use the AEQ functionality for the TDP1204 and the TMDS1204 through an example using the TMDS1204EVM. Lastly, a few example tests were conducted to validate the AEQ algorithm functionality.

2 Test Setup

This procedure uses the test setup as shown in Figure 2-1. Note, the HDMI 2.1 cables should not be connected immediately, but should be connected as described in Section 3. For more information, see the *TMDS1204 EVM User's Guide* as this provides a schematic and an understanding of the functionality of the board before continuing to Section 3. Additionally, the proper software needs to be downloaded onto a personal laptop that includes Total Phase Control Center v4.3.0 and Total Phase USB Driver for I2C/SPI Adapter.

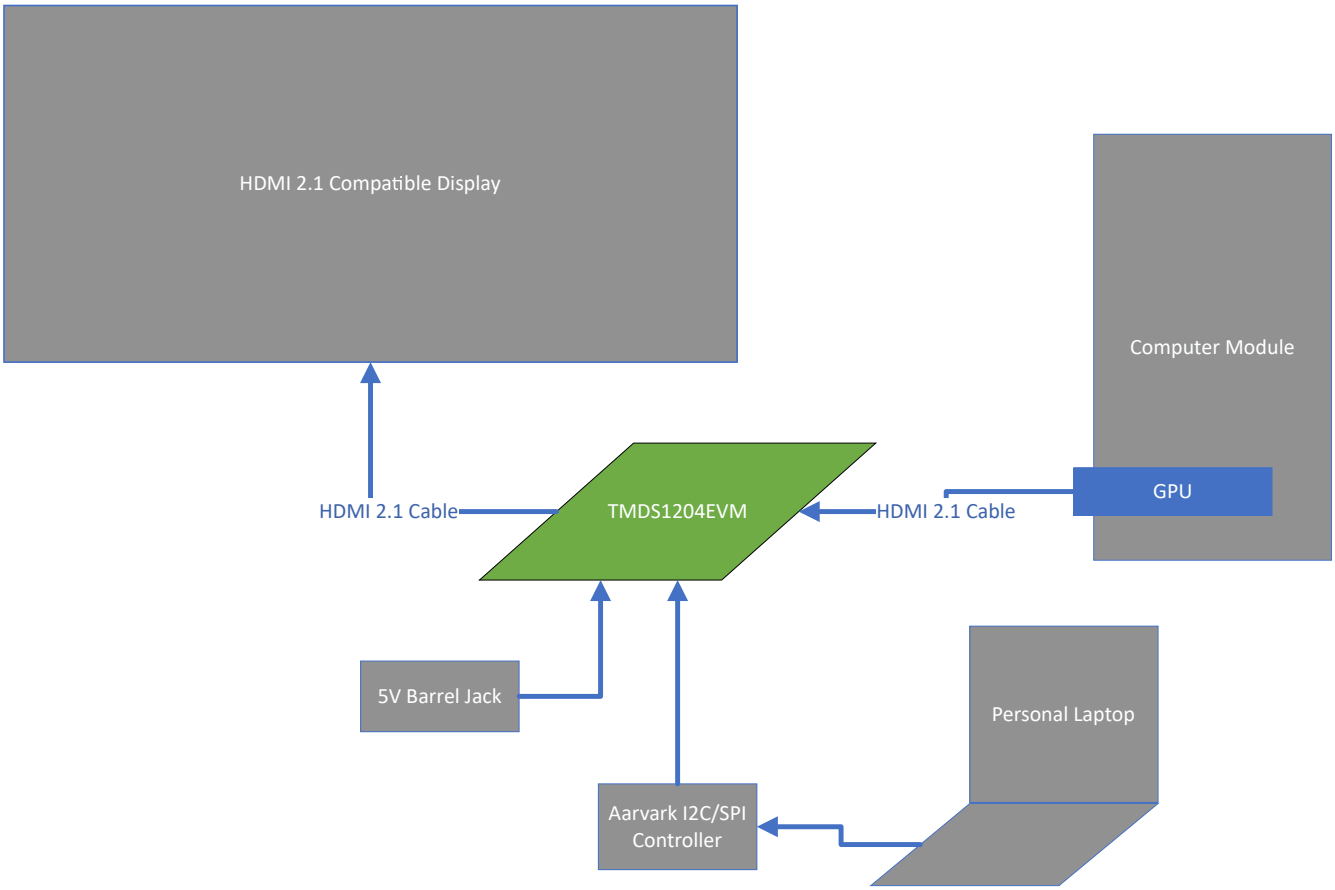

Figure 2-1. Test Setup Diagram

3 Test Procedure

Upon gathering all essential HW/SW, turn on the computer module and monitor to verify that both are working properly and configured to act as the HDMI 2.1 signal source and sink, respectively. Upon powering up the computer module and monitor, proceed to integrate the TMDS1204EVM into the test setup.

The following test procedure assumes that the TMDS1204EVM is in the external I2C configuration. However, the AEQ functionality can be used in both pin strap and I2C modes but for convenience of demonstration we use I2C mode in this procedure. To set the EVM to I2C mode, leave JMP 4 pins 4 and 6 unconnected. To integrate the EVM into the test setup and use AEQ functionality, do the following:

1. Insert the +5 V DC power source into the barrel jack. Turn on SW2.
2. Configure TMDS1204 using the I2C bus as described in the AEQ configuration section.
3. Insert an HDMI source using a standard HDMI cable into P1 (HDMI receptacle).
4. Insert an HDMI video sink into P2 (HDMI receptacle) using a standard HDMI cable.
5. Video output on HDMI sink should be observed.

3.1 AEQ Configuration

The TMDS1204 chip needs to be configured through the I2C bus to allow you to use AEQ functionality. You can access the I2C bus using J5. In this procedure, the Aardvark™ I2C/SPI adapter is plugged in directly to J5 and then a laptop to provide I2C read and write control capabilities. Afterwords, open the Total Phase Control Center v4.3.0 GUI and use the “Adapter” tab to connect to the EVM and use the Batch Mode to write to the TMDS1204 registers. The following code provides the Aardvark script that allows TMDS1204 to use AEQ functionality and configure the device. The script resets the AEQ before it is enabled by writing F3 to register offset 1Dh and then enables AEQ by writing 40 to register offset 1Eh.

```
<aardvark>
    <configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
    <i2c_bitrate khz="100"/>


======Rate snoop enabled, TXFFE snoop enabled. Enable SWAP======
<i2c_write addr="0x5E" count="1" radix="16">0A 88</i2c_write>/>

======3G and 6G TX slew rate control======
<i2c_write addr="0x5E" count="1" radix="16">0B 34</i2c_write>/>

======Clock and 8G10G10G TX slew rate control======
<i2c_write addr="0x5E" count="1" radix="16">0C 71</i2c_write>/>

======Linear, DC-coupled, 0dB DCG, TERM Auto, Disable CTLE bypass======
<i2c_write addr="0x5E" count="1" radix="16">0D A2</i2c_write>/>

======HDMI14, HDMI20, and HDMI21 CTLE Selection======
<i2c_write addr="0x5E" count="1" radix="16">0E 3F</i2c_write>/>

======Disable DDC Buffer======
<i2c_write addr="0x5E" count="1" radix="16">10 00</i2c_write>/>

======CLOCK VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">12 03</i2c_write>/>

======CLOCK EQ======
<i2c_write addr="0x5E" count="1" radix="16">13 01</i2c_write>/>

======D0 VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">14 03</i2c_write>/>

======D0 EQ======
<i2c_write addr="0x5E" count="1" radix="16">15 01</i2c_write>/>

======D1 VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">16 03</i2c_write>/>

======D1 EQ======
<i2c_write addr="0x5E" count="1" radix="16">17 01</i2c_write>/>

======D2 VOD and TXFFE======
<i2c_write addr="0x5E" count="1" radix="16">18 03</i2c_write>/>
```

```
======D2 EQ======
<i2c_write addr="0x5E" count="1" radix="16">19 01</i2c_write>/>

======AEQ Config======
<i2c_write addr="0x5E" count="1" radix="16">1D F3</i2c_write>/>

======AEQ Enable======
<i2c_write addr="0x5E" count="1" radix="16">1E 40</i2c_write>/>

======Clear x40 bit======
<i2c_write addr="0x5E" count="1" radix="16">20 00</i2c_write>/>

======Take out of PD.  HPD_OUT will get asserted high if HPD_IN is high======
<i2c_write addr="0x5E" count="1" radix="16">09 00</i2c_write>/>

</aardvark>
```

3.2 Verify AEQ Configuration

After writing to the registers, you should read back all registers to ensure that no errors occurred while writing to the device's registers. The following code shows an Aardvark script that allows you to read back the I2C registers of the TMDS1204 to verify AEQ functionality.

```
<aardvark>
    <configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
    <i2c_bitrate khz="100"/>

======Read TMDS x40 Status ======
<i2c_write addr="0x5E" count="0" radix="16">20</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>

======Read FRL Status ======
<i2c_write addr="0x5E" count="0" radix="16">31</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>

<i2c_write addr="0x5E" count="0" radix="16">35</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>

<i2c_write addr="0x5E" count="0" radix="16">41</i2c_write>/>
<i2c_read addr="0x5E" count="2" radix="16">00</i2c_read>/>


======Read AEQ Status ======
<i2c_write addr="0x5E" count="0" radix="16">50</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>

======Read AEQ Status ======
<i2c_write addr="0x5E" count="0" radix="16">51</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>

======Read EQ Levels ======
<i2c_write addr="0x5E" count="0" radix="16">15</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>
<i2c_write addr="0x5E" count="0" radix="16">17</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>
<i2c_write addr="0x5E" count="0" radix="16">19</i2c_write>/>
<i2c_read addr="0x5E" count="1" radix="16">00</i2c_read>/>


</aardvark>
```

After running this script in Batch Mode, you should see similar results as shown in the Table 3-1 in the Transaction Log at the bottom of the Aardvark GUI. Note, these results are expected results using an 8k4k display at 60 Hz as an example.

Table 3-1. Transaction Log Register Values

Register Offset	Data
0x20h	0x00h
0x31h	0x36h
0x35h	0x00h
0x41h	0x00h 0x00h
0x50h	0x83h
0x51h	0x39h
0x15h, 0x17h & 0x19h	0x01h

The key registers to determine if the device is operating as needed for AEQ functionality, for the example of an 8k2k display at 60 Hz, are discussed below.

- For register offset 0x20h, known as SCDC_TMDS_CONFIG, the expected read value is 0x00h which means that TMDS Bit Period to Clock Period Ratio is 1/10.
- For register offset 0x31h, known as SCDC_SINK_CONFIG, the expected read value is 0x36h, which means that device supports maximum FFE level and data rate supported is 12 Gbps on 4 lanes.
- For register offset 0x50h, known as AEQ_STATUS, the expected read value is 0x83h. When the first value is 0x8h this means that the AEQ algorithm is complete. The second value indicates the EQ level selected, which in this case is EQ level 3.

4 AEQ Functional Tests

Three tests were conducted using the procedure outlined in this document. These three tests with corresponding results are summarized in Table 4-1.

Table 4-1. AEQ Testing and Results

Test ID	Test Conditions	Results Summary
Enabled AEQ Test 1	Cable into P1: 10’ HDMI 2.1 Cable Cable out P2: 6’ HDMI 2.1 Cable	• AEQ selected the EQ value of 8 • Display Res. = 7680 x 4320 @ 60Hz • Bit Depth = 8 bit
Enabled AEQ Test 2	Cable into P1: 6’ HDMI 2.1 Cable Cable out P2: 10’ HDMI 2.1 Cable	• AEQ selected the EQ value of 4 • Display Res. = 7680 x 4320 @ 60Hz • Bit Depth = 8 bit
Disabled AEQ Test	Cable into P1: 10’ HDMI 2.1 Cable Cable out P2: 6’ HDMI 2.1 Cable	• Manual selection of EQ value of 7 through 10 • Some screen flickering observed at EQ values 7 and 10 • EQ values 8 and 9 appeared to produce the same screen quality as seen in AEQ Test 1

The test results show that using the TDMS1204 EVM with longer cables at the P1 port drives the AEQ algorithm to select a higher EQ value. Additionally, with the AEQ disabled, the manual selection shows that signal quality degrades when not selecting the EQ option determined by the AEQ algorithm.

5 Summary

The TMDS1204 and TDP1204 are HDMI 2.1 redrivers that support AEQ functionality that provides a cost-effective solution to applications that have dynamic channel characteristics. The procedure to use the AEQ functionality for both devices was given by using the example of the TMDS1204 EVM. This procedure can help to provide direction to other design when integrating the TMDS1204 or TDP1204 into other applications. Lastly, this document provided test results following the test procedure to show that AEQ functionality can correctly select the right EQ value to equalize the channel.

6 References

- *TMDS1204 EVM User's Guide*
- *TMDS1204 12-Gbps, DC or AC-Coupled to TMDS® and FRL HDMI™ Hybrid Redriver Data Sheet*
- *TDP1204 12-Gbps, DC/AC-Coupled to HDMI™ 2.1 Level Shifter Hybrid Redriver Data Sheet*

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