Application Note

DP83826 Troubleshooting Guide

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1 Trademarks

All trademarks are the property of their respective owners.

2 DP83826 Application Overview

The DP83826 offers low and deterministic latency, low power, and supports 10BASE-Te, 100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems. The device includes hardware bootstraps to achieve fast link-up time, fast link-drop detection modes, and dedicated reference CLKOUT to clock synchronize other modules on the systems.

Figure 2-1 is a high-level system block diagram of a typical DP83826 application.

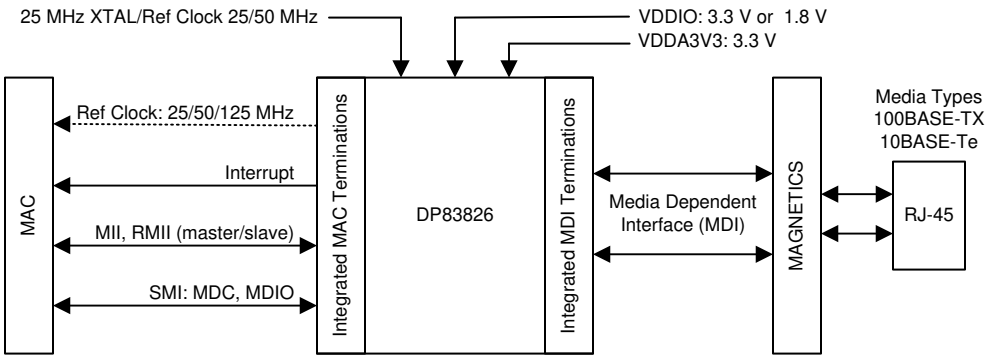

Figure 2-1. DP83826 Block Diagram

The DP83826 connects to an Ethernet MAC and to a media. The connection to the media is via a transformer and a connector.

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

3 Troubleshooting the Application

The following sections approach the debug from a high level, attempting to start with application characteristics that have a broad impact and then zeroing in on more focused aspects of the design.

3.1 Read and Check Register Values

Read the registers and verify the default values shown in the data sheet. Note that the initial values of some registers can vary based on strap options.

The expected register values for PHY operation and link in 10/100 Mbps with auto-negotiation enabled are shown below.

Table 3-1. DP83826 Register Value References

REGISTER ADDRESS	REGISTER VALUE	
	10 Mbps	100 Mbps
0x0000	3100	3100
0x0001	786D	786D
0x0002	2000	2000
0x0003	A130	A130
0x0004	0041	01E1
0x0005 (1)	41E1	41E1
0x0006	0007	0007
0x0007	2001	2001
0x0008	0000	0000
0x0009	0000	0000
0x000A	0100	0100
0x000B	0000	0000
0x000D	0000	0000
0x000E	0000	0000
0x000F	0000	0000
0x0010 (2)	4717 or 0017	4715 or 0715
0x0011	0108	0108
0x0012	7400	7400
0x0013	2800	2800
0x0014	0000	0000
0x0015	0000	0000
0x0016	0100	0100
0x0017	0041	0041
0x0018	0480	0480
0x0019	C000	CC00
0x001A	0000	0000
0X001B	007D	007D
0X001B	05EE	05EE
0X001C	0000	0000
0x001E	0002	0102

With the PHY linked in a given speed, use these values as a reference to identify any variance from the expected operation. Note that not all registers need to be the same, for example .

1. The value of Register 0x0005 depends on the link partner's capabilities.
2. The '4' or '0' difference in the MSB of Register 0x0010 is due to bit 14 MDI/MDIX Mode, doesn't affect anything. The significant difference is the '7' or '5' as the LSB, this tells you the Speed Status.

Example: After powering and linking the PHY in 10 Mbps, register 0x0010 is read at hex value 0017. Meaning Bits [4, 2, 1, 0] are high. These bits confirm: Auto-Negotiation is complete, Full-Duplex, 10 Mbps Mode, and valid link established.

Repeating this process for any values distinct from the expected values shown in the table will help diagnose the exact state of the PHY for any encountered issues.

3.2 Schematic and Layout Checklist

Reference and verify all of the noted schematic and layout recommendations in the following spreadsheet:

DP83826 Schematic and Layout Checklist

3.3 Component Checklist

Magnetics:

The following guidelines are the main specifications to reference for compatible magnetics:

Table 3-2. Recommended Transformers

MANUFACTURER	PART NUMBER
Pulse Electronics	HX1198FNL
	HX1188NL
	HX1188FNL

Table 3-3. Magnetic Isolation Requirements

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Insertion Loss	1-100 MHz	-1	dB
Return Loss	1-30 MHz	-16	dB
	30-60 MHz	-12	dB
	60-80 MHz	-10	dB
Differential to Common Mode Rejection Ratio	1-50 MHz	-30	dB
	50-150 MHz	-20	dB
Crosstalk	30 MHz	-35	dB
	60 MHz	-30	dB
Isolation	HPOT	1500	Vrms

If these exact requirements cannot be met, the following allowances can be made:

- Turns ratio
  - Ideally 2%, but 3% is tolerable.
- Inductance
  - High inductance is preferred. Usual numbers seen are around 350 µH.
- Insertion loss
  - As close to 0 dB as possible compared to specified value for each range stated in data sheet. If specification gives -1 dB as typical. finding a component with -1 dB, -0.9 dB, … is recommended.
- Return loss

– At or lower than the magnitude specified in data sheet. If specification gives -16 dB as typical, finding a component with -16 dB, -17 dB, … is recommended.

Crystal

The following guidelines are the main specifications to reference for compatible crystals:

Table 3-4. 25-MHz Crystal Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature	-100		100	ppm
Load Capacitance			15	40	pF
ESR				50	Ω

Table 3-5. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Rise / Fall Time	20% - 80%			5	ns
Symmetry	Duty Cycle	40%		60%	
Jitter RMS	Integration Band: 12 kHz to 5 MHz			11	ps

3.4 Peripheral Pin Checks

The following section details the expected values of various peripheral output pins of the PHY during operation - measure and compare the noted pin outputs to verify PHY operation.

3.4.1 Power Supplies

The power supplies are the first key item to check. Power up the device and perform DC measurement of the supplies as close to the pin as possible. Confirm that each measurement is within the limits defined in the *Recommended Operating Conditions* section of the datasheet.

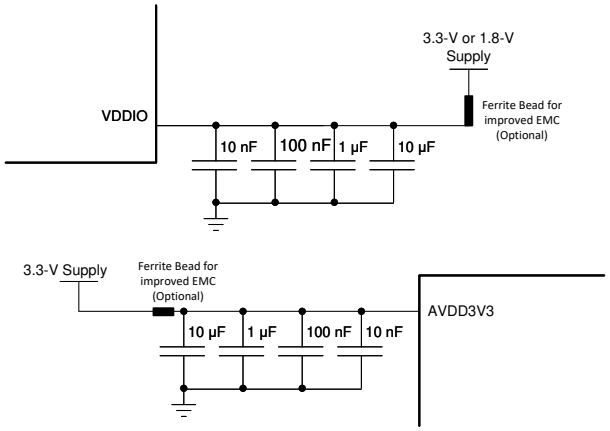

Figure 3-1. Power Supply Decoupling Recommendation

3.4.2 Probe the XI Clock

Verify the frequency and signal integrity. For link integrity the clock must be 25 MHz ±50 ppm in MII and RMII Master modes, 50-MHz ±50 ppm in RMII Slave mode.

If using a crystal as the clock source, probe the CLK_OUT signal. Probing the crystal can change the capacitive loading and therefore change the operational frequency. The default signal on CLK_OUT is a buffered version of the XI reference and will provide a representative measurement.

3.4.3 Probe the RESET_N Signal

The reset input is active low. It is important to confirm that the controller is not driving the RESET_N signal low. Otherwise, the device will be held in reset and will not respond.

3.4.4 Probe the Strap Pins During Initialization

In some cases, other devices on the board (for example, the MAC) will pull or drive these pins unexpectedly. The strap values can be read from the registers. The values are available in register 0x006E (STRAP_STS1) and register 0x006F (STRAP_STS2). If you're still not sure about the PHY's Strapping, confirm that these signals are in the range of the target voltages described in Table 9-6 found in the *Programming* section of the datasheet. Measurements can be made during power up and after power up when the RESET_N signal is asserted.

3.4.5 Probe the Serial Management Interface Signals (MDC, MDIO)

MDIO should pull up to the I/O supply when undriven. Probe MDIO to confirm the default voltage.

Attempt to read the registers. Verify the MDIO data sequence with the datasheet to make sure the MDIO read access timing is correct.

3.4.6 Probe the MDI Signals

In the default configuration, Auto-negotiation and Auto-MDIX will be enabled. A link pulse should be visible on the channel transmit and receive differential pair (TD_P, TD_M).

A short Ethernet cable with 100 Ohm terminations can be used for measuring the MDI signals. A terminated cable is shown in Figure 3-2. A connection diagram for making measurements with the terminated cable is shown in Figure 3-3.

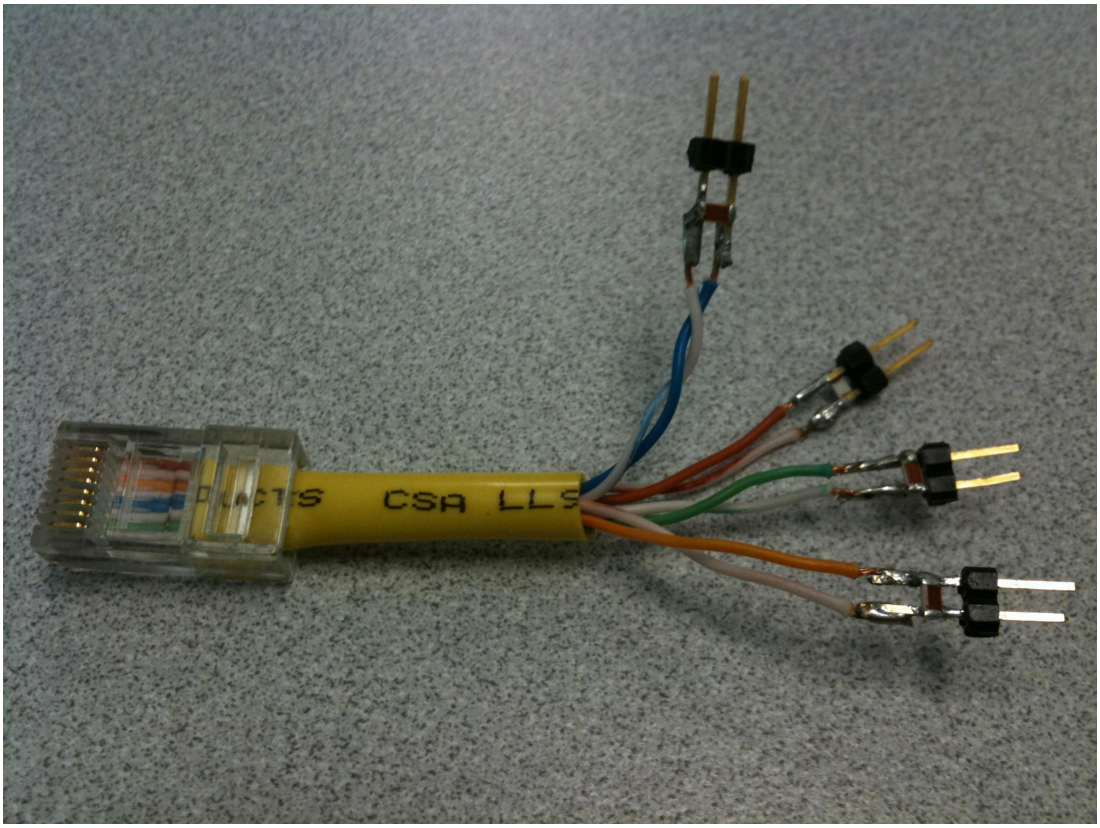

Figure 3-2. 100 Ω Terminated Cable for MDI Signal Measurement

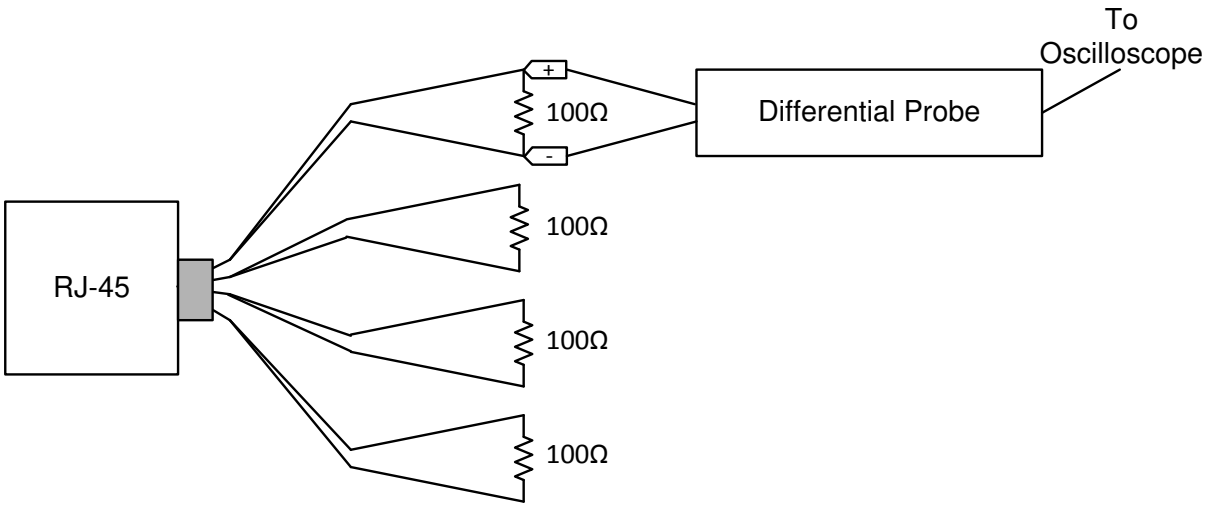

Figure 3-3. Connection Diagram for 100 M Terminated Cable

Auto-Negotation link pulses are nominally 100ns wide. Pulses are spaced by 62 µs or 125 µs and are transmitted in bursts. The bursts are nominally 2 ms in duration and occur every 16 ms. Figure 3-4shows a link pulse.

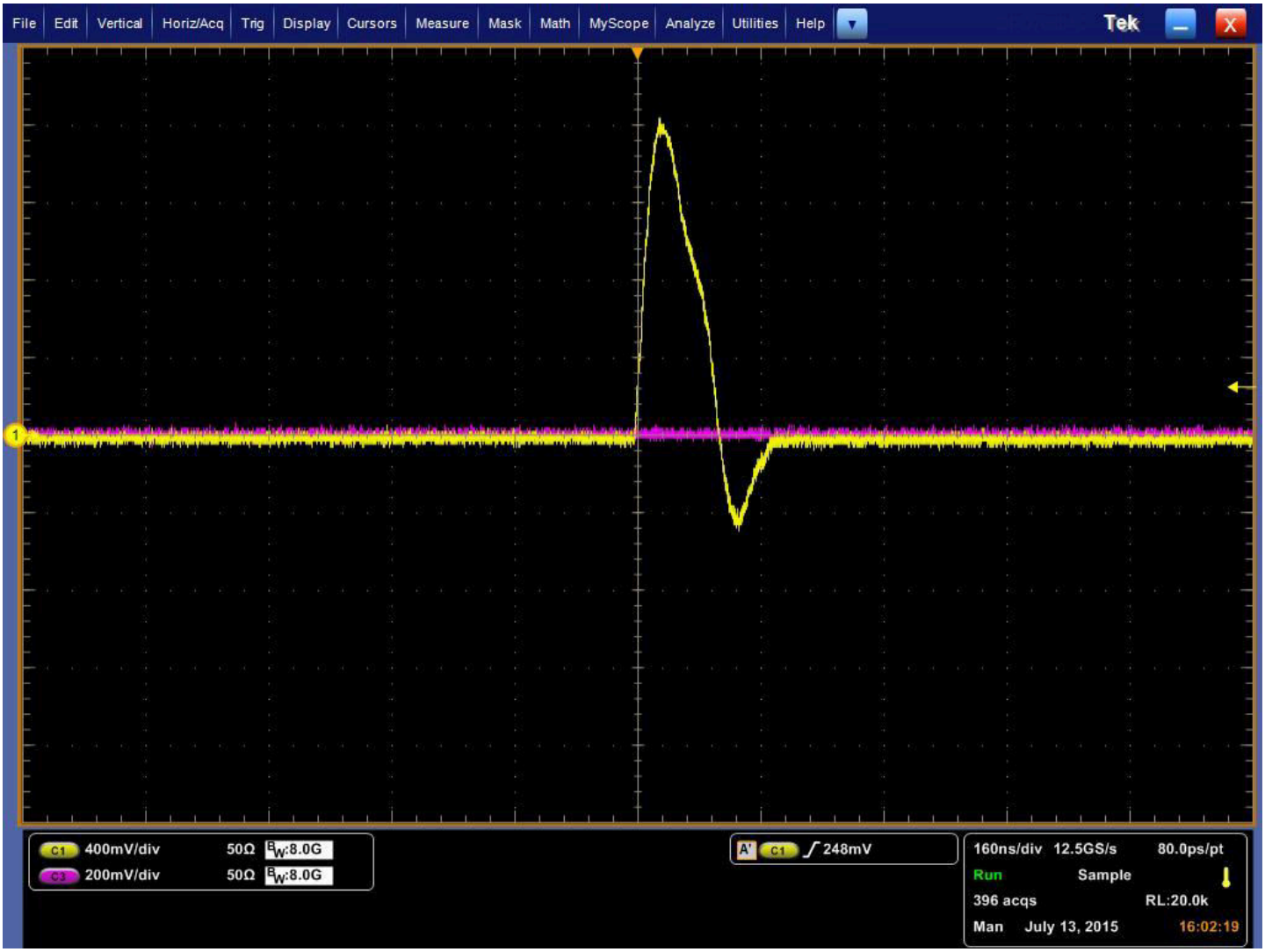

Figure 3-4. DP83826 Link Pulse

3.5 Link Quality Check

After establishing a valid link, confirming the key status register values and visually verifing that the link LED is lit, the next data transfer debug step is to check the MAC Interface.

There are several possible sources of link problems:

1. Link partner transmit problem
2. Cable length and quality
3. Clock quality of the 25 MHz reference clock
4. MDI signal quality

IEEE compliance measurements can be made to verify the signaling. For details on these measurements, please refer to the application note *DP83826 Ethernet Compliance Testing* (SNLA239).

With the PHY powered and connected to a link partner, the following registers can be read from to determine the health of the link:

Table 3-6. Link Quality MSE Registers

CHANNEL	REGISTER ADDRESS
A	0x225

For a given channel, read the register value to determine the MSE (Mean Square Error), convert to decimal, and refer to the following table to determine link quality:

Table 3-7. MSE Link Quality Ranges

LINK QUALITY	MSE RANGE
Excellent	< 522
Good	522 - 827
Poor	> 827

3.6 Built-In Self Test with Various Loopback Modes

There are several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DP83826 may be configured to one of the Near-end loopback modes or to the Far-end (reverse) loopback. MII Loopback is configured using the BMCR (register address 0x0000). All other loopback modes are enabled using the BISCR (register address 0x0016). Except where otherwise noted, loopback modes are supported for all speeds (10/100) and all MAC interfaces.

The device incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. BIST can be performed using various loopback modes to isolate any issues to specific parts of the data path. The BIST generates packetized data with variable content and IPG. The following diagrams illustrate the various data paths that each loopback mode can be used to verify:

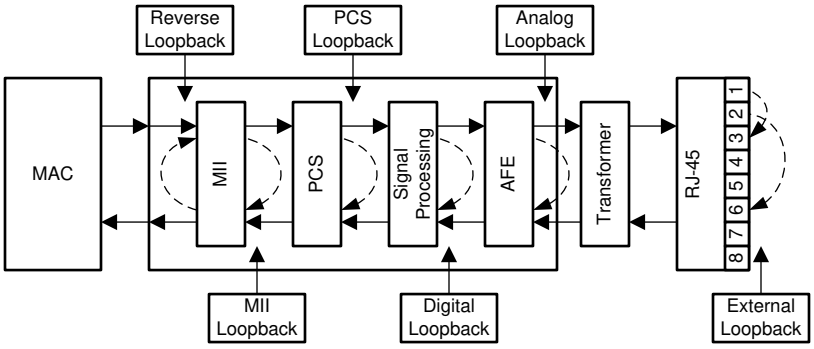

Figure 3-5. Block Diagram, Loopback Modes

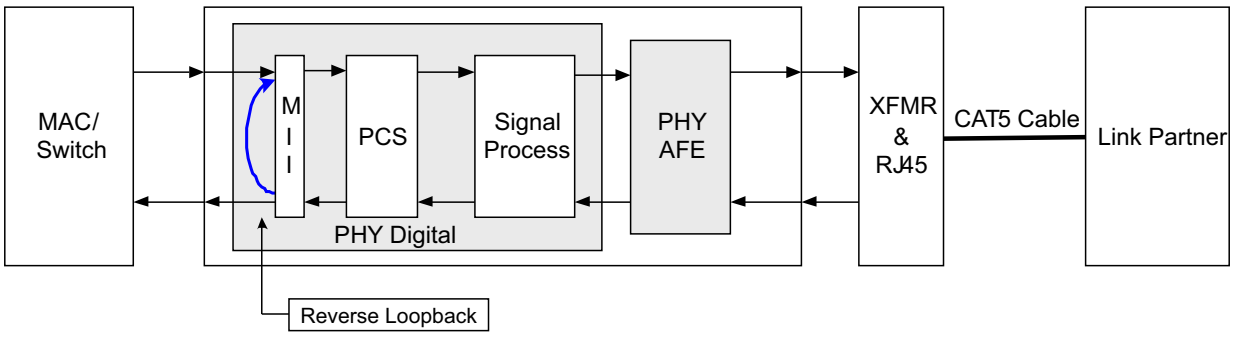

Figure 3-6. Block Diagram, Reverse Loopback Mode

Analog loopback is typically used to verify the PHY's full internal data path, while reverse loopback is used with a link partner to verify the data path along the MDI.

Transmitting and Receiving Packets with the MAC:

If generating and checking packets with the MAC is possible, and the PHY has a working link partner with reverse loopback capability, verify the full data path as follows:

1. Power and connect the PHY to the MAC and a working link partner.
2. Enable reverse loopback on the link partner (for DP83826 link partner, write 0x16 to 0010).
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receieves the same test packets.

If the MAC receives the same test packets transmitted without issue, the full data path through MAC → PHY → MDI is valid. If this test does not pass, perform analog loopback to isolate the issue along the data path:

1. Power and connect the PHY to the MAC.
2. Enable analog loopback on the PHY (write 0x16 to 0008).
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receives the same test packets.

If the MAC receives the same test packets, the data path through MAC → PHY is valid, and the issue has been isolated to the MDI data path. If this test does not pass, the issue can be on the MAC interface or the internal data path. To verify the MAC interface, refer to Debugging MAC Interface. To verify the internal data path, perform PRBS with analog loopback using the following script.

Transmitting and Receiving Packets with BIST:

If generating and checking packets with the MAC is not possible, use PRBS packet generation and checking functionalities to verify the data path. Perform reverse loopback with PRBS and a working link partner as follows:

1. Power and connect the PHY to a link partner.
2. Enable PRBS packet generation on the PHY (write 0x16 to 5000).
3. Enable reverse loopback on the link partner (for DP83826 link partner, write 0x16 to 0020).
4. Wait at least one second, then check PRBS lock status on the PHY (read register 0x17[11:10]).

If register 0x17[11] is high, the data path through PHY → MDI is valid. If this test does not pass, the issue could be on the PHY's internal data path or the MDI. To verify the internal data path, perform PRBS with analog loopback using the following script. If the internal data path is valid, then the issue is isolated to the MDI (assuming the link partner is working).

Below is an example sequence of register reads and writes to perform BIST with Analog Loopback in 100Mbps:

```
// Analog Loopback

begin

001F 8000 //Hard Reset
0000 2100 //Disables Auto-Neg, Selects 100 Mbps
0016 0108 //Select Analog Loopback
030B 3380 //This helps PRBS LOCK
001F 4000 //Soft Reset

0010      // LSB '5' expected.

0016 3108 //Enables PRBS Checker Config & Packet Generation Enable
      //After you write '3108' the register should Read 3b04. (Bit 11 & 9 go high)
001B 807D //Lock Error Counter's Value
001B

end
```

```
//DP83826 Digital Loopback 100Mbps PRBS Packet Generator

begin

001F 8000 //Hard Reset
0000 2100 //Disable Auto Negotiation and Chooses 100 Mbps
0016 0104 //Enable Digital Loopback
0122 2000
0123 2000
0130 47FF
001F 4000 //Soft Reset
```

```
0010      //Bit 0 = '1' confirms Link (No Link expected for 10 Mbps)
      //Bit 1 = '0' confirms 100 Mbps Speed

0016 3104 //Enables PRBS Checker Config & Packet Generation Enable
      //After you write '3104' the register should Read 3b04. (Bit 11 & 9 go high)
001B 807D //Lock Error Counter's Value
001B

end
```

3.7 Debugging MAC Interface

MII Link

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2002 clause 22.

MII is set by default in the PHY with Hardware Strap 8 RX_D2 = '0'. Register 0x0467, bit 8, can confirm the status of strap 8 (High or Low) and Register 0x0468, bit 4, can confirm the PHY's MAC Mode(MII = '0' | RMII = '1').

The MII signals are summarized below:

Table 3-8. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_EN
	RX_DV
Line-Status Signals	CRS
	COL
Error Signals	RX_ER

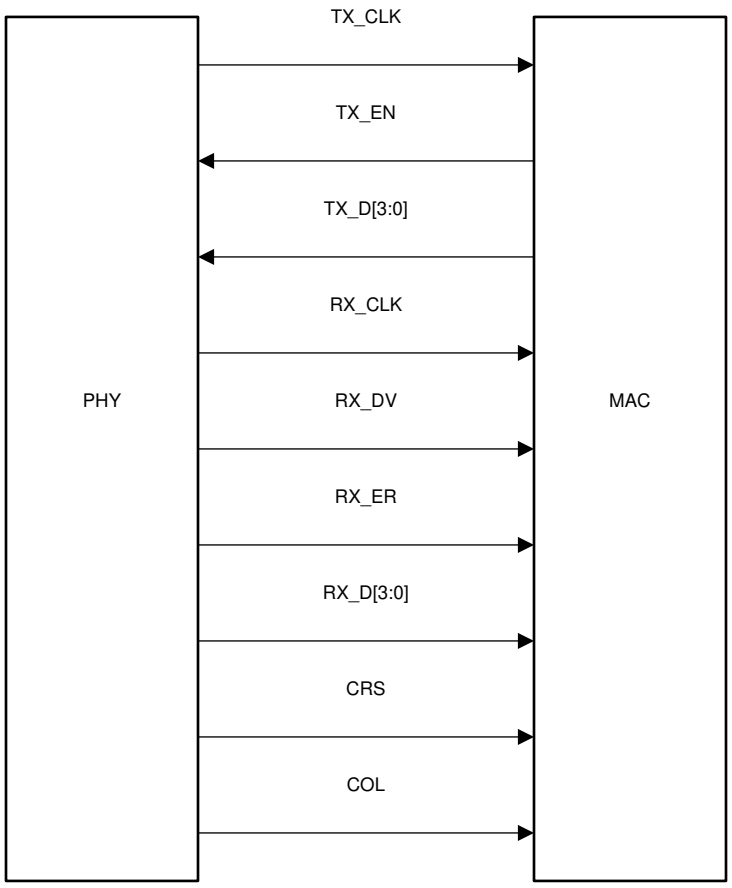

Figure 3-7. MII Signaling

Reference the waveforms below to verify the expected MAC data and clock signals for 100BASE-Tx MII Mode. The table displays specs taken from the Datasheet that are shown in the waveforms.

Table 3-9. 100M MII Receive Timing

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T1	RX_CLK High / Low Time	16	20	24	ns
T2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising	10		30	ns

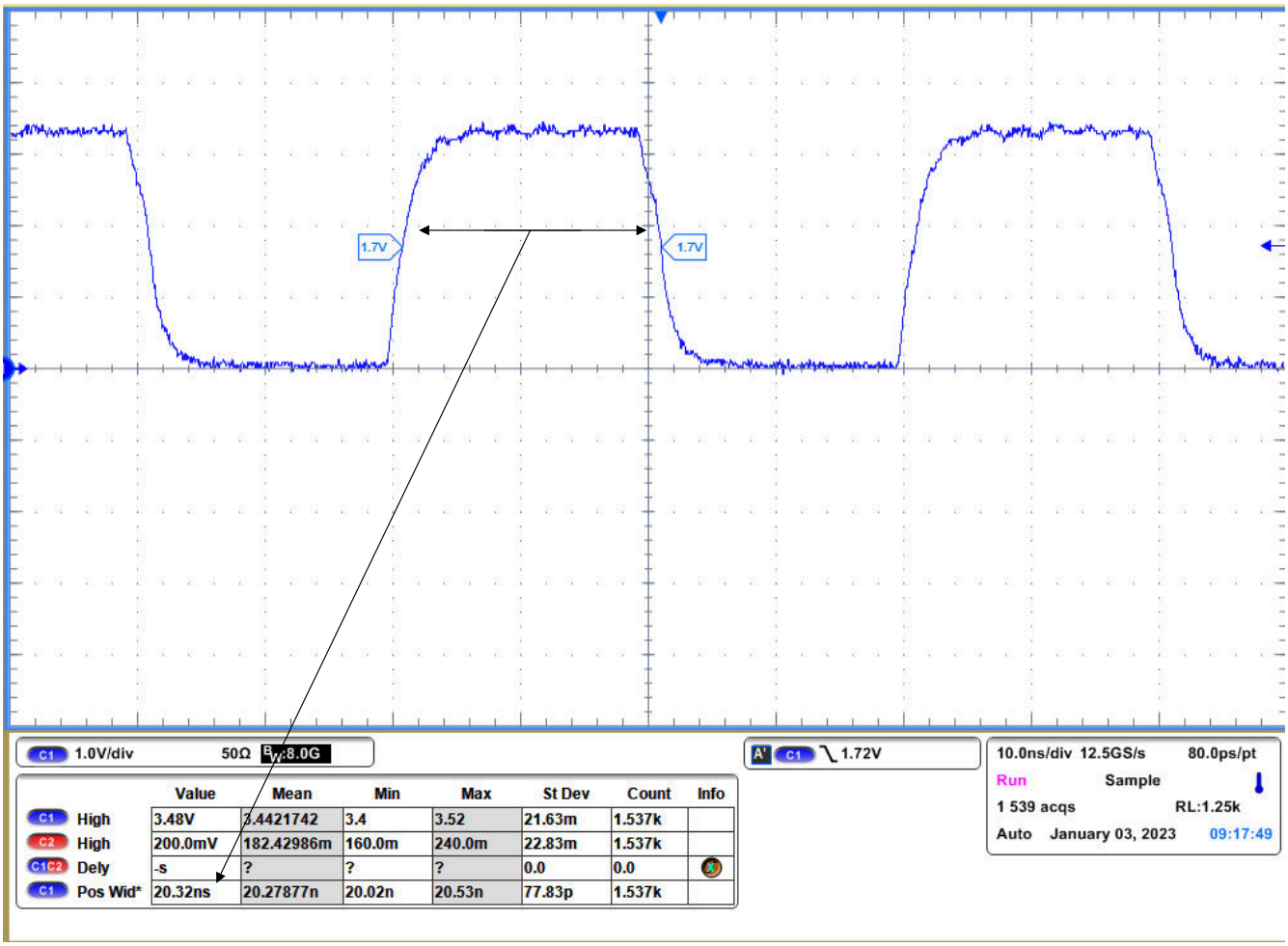

Figure 3-8. RX_CLK High Time

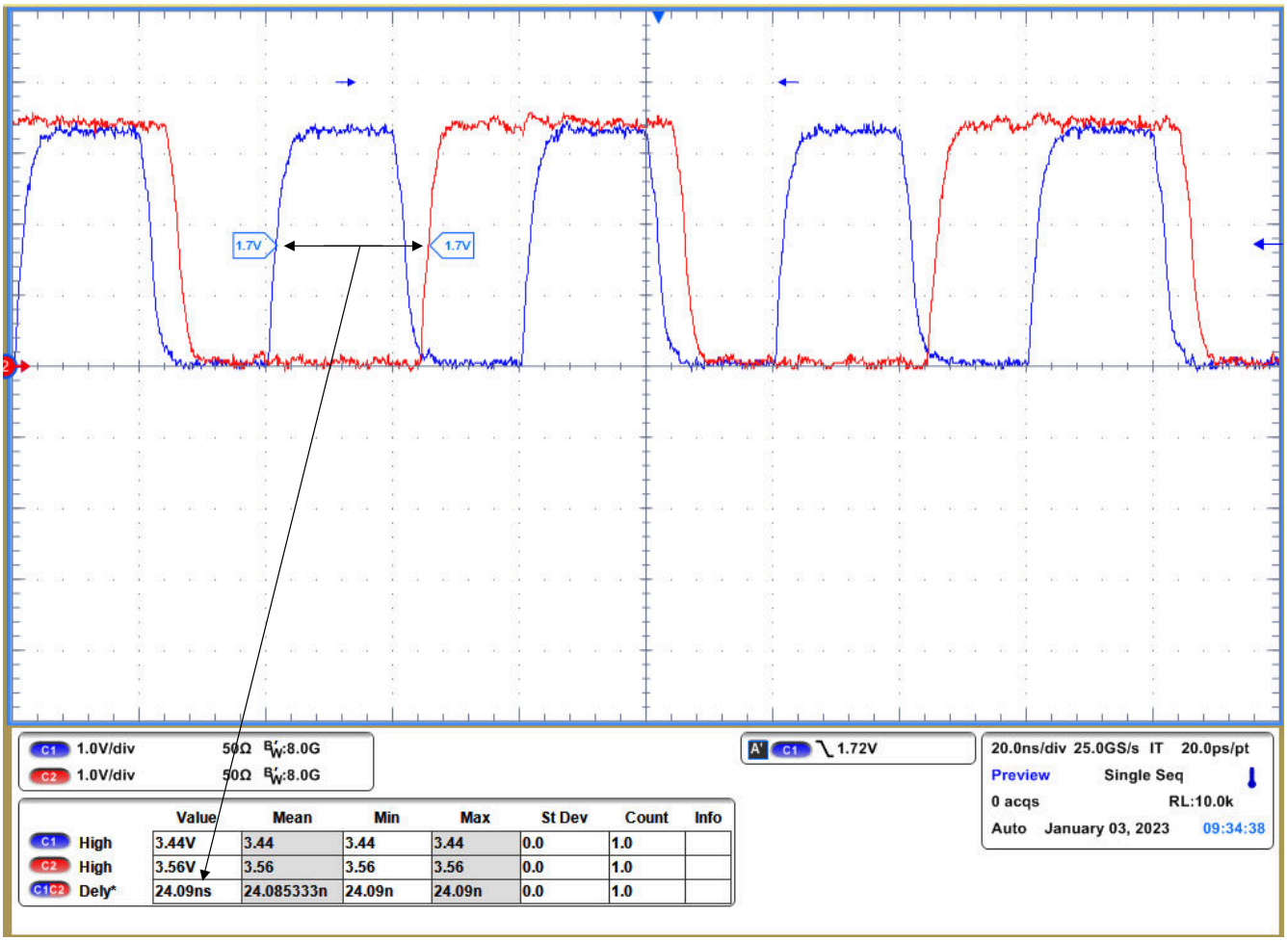

Figure 3-9. RX_D1 Delay from RX_CLK rising

RMII Link

Reduced Media Independent Interface, as specified in the RMII specification v1.2, provides a reduced pin count alternative to the IEEE 802.3 MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII. The DP83826 offers two types of RMII operations: RMII Master and RMII Slave.

In RMII Master operation, the DP83826 operates from either a 25-MHz CMOS-level oscillator connected to XI pin or a 25-MHz crystal connected across XI and XO pins. A 50-MHz output clock referened from DP83826 can be connected to the MAC.

In RMII Slave operation, the DP83826 operates from a 50-MHz CMOS-level oscillator connected to the XI pin and shares the same clock as the MAC. Alternatively, the PHY can operate from a 50-MHz clock provided by the Host MAC.

The RMII specification has the following characteristics:

- Supports 100BASE-TX and 10BASE-Te
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2-bit wide transmit and receive data paths
- Uses CMOS signal levels, the same levels as the MII interface

RMII can be set with pulling up Hardware Strap 8 RX_D2 = '1'. Register 0x0467, Bit 8 can confirm the Status of Strap 8 (High or Low) and Register 0x0468, can confirm the PHY's MAC Mode(MII = '0' | RMII = '1').

In this mode, data transfers are 2 bits for every clock cycle using the internal 50-MHz reference clock for both transmit and receive paths. The RMII signals are summarized below:

Table 3-10. RMII Signals

FUNCTION	PINS
Receive data lines	TX_D[1:0]
Transmit data lines	RX_D[1:0]
Receive control signal	TX_EN
Transmit control signal	CRS_DV

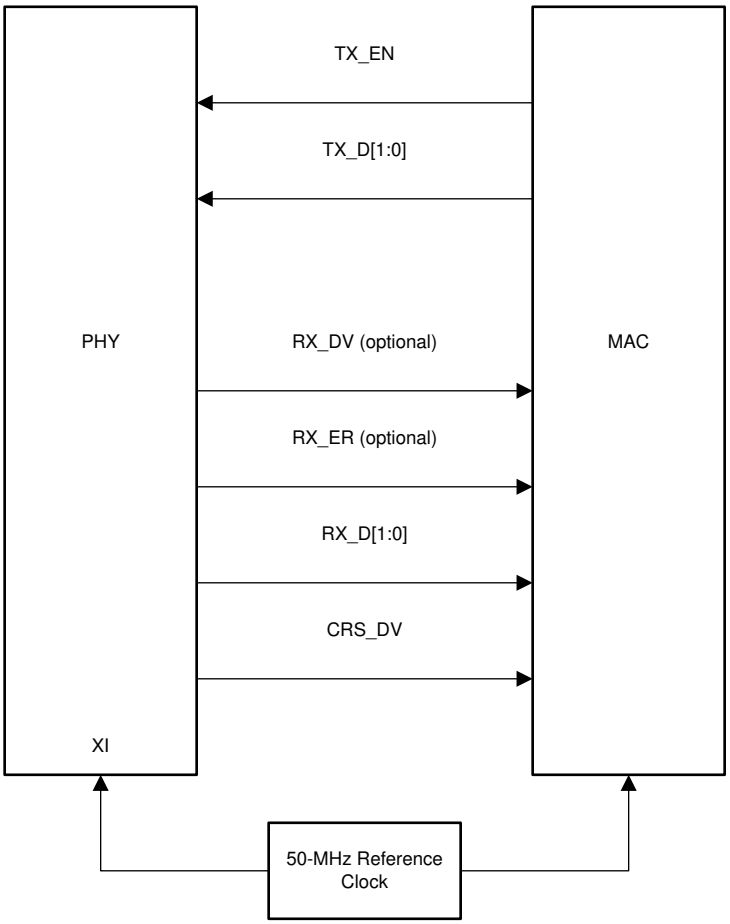

Figure 3-10. RMII Slave Signaling

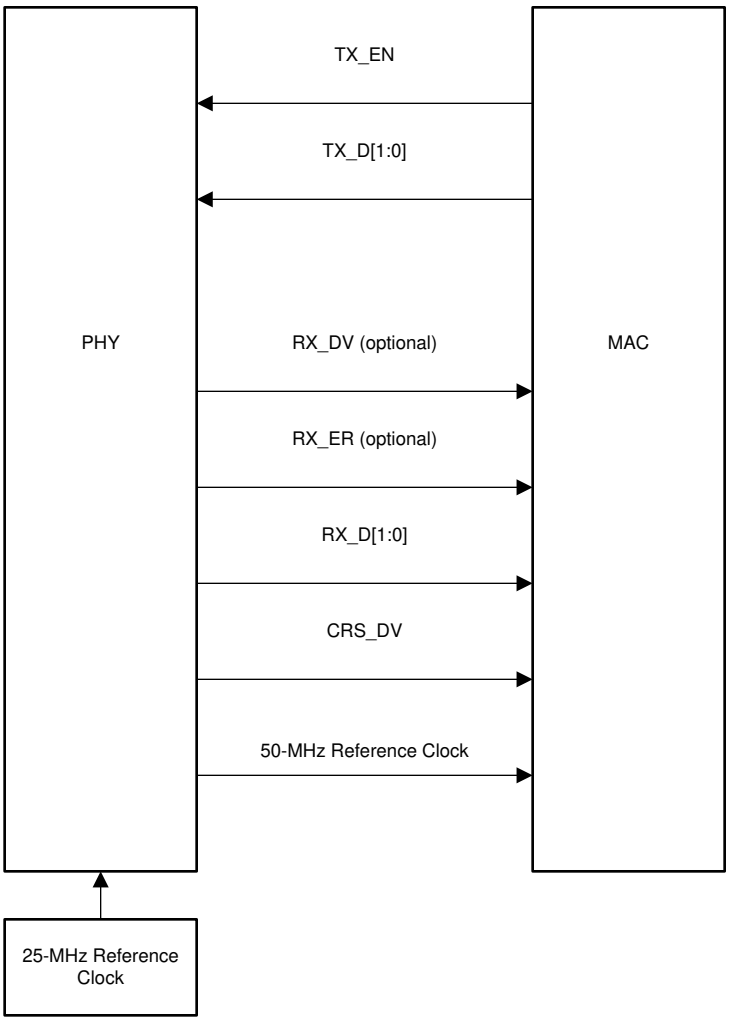

Figure 3-11. RMII Master Signaling

Data on TX_D[1:0] are latched at the PHY with reference to the 50 MHz-clock in RMII master mode and slave mode. Data on RX_D[1:0] is provided in reference to 50-MHz clock. In addition, CRX_DV can be configured as RX_DV signal. It allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication.

3.8 Tools and References

3.8.1 DP83826 Register Access

If register access is not readily available in the application, USB-2-MDIO GUI is available from TI and can be used with an MSP430 Launchpad, purchasable through the TI eStore (https://store.ti.com/). The GUI supports reading and writing registers as well as running script files. It can be used with the DP83826 and the other devices in TI's Ethernet portfolio. The USB-2-MDIO User's Guide and GUI are available for download at: http://www.ti.com/tool/usb-2-mdio

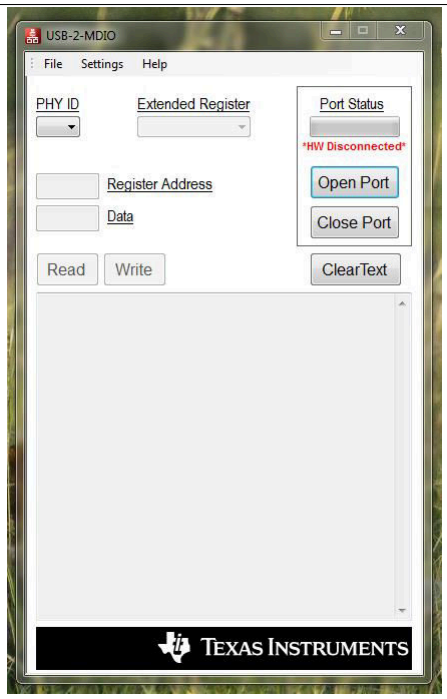

Figure 3-12. USB-2-MDIO GUI

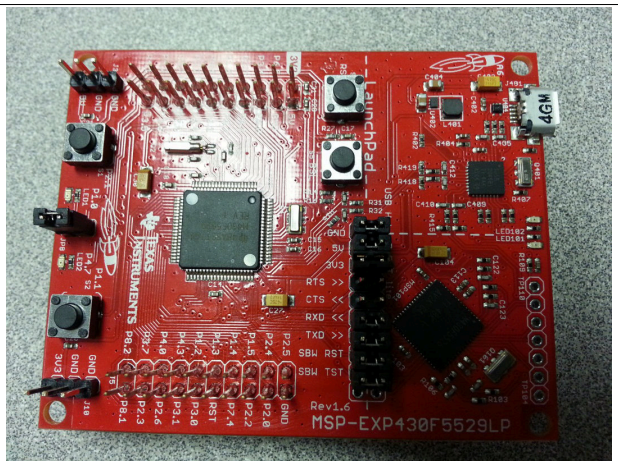

Figure 3-13. MSP430 LaunchPad

Below is an example script that can also be found in the USB-2-MDIO GUI in the Help menu:

```
// This is how you make a comment. All scripts must start with 'begin'
begin
// To read a register, all you need to do is put down the 4 digit
// HEX value of the registers (from 0000 to FFFF)
// Example to read registers 0001, 000A, and 0017
0001
000A
0017
// To write a register, all you need to do is put down the 4 digit
// HEX value of the register (from 0000 to FFFF) followed by the
// HEX you desire to configure the register to (from 0000 to FFFF)
// Example to write 2100 to register 0000 and
// Example to write 0110 to register 0016
0000 2100
0016 0110
// You must end the script by adding 'end' once you are finished
end
```

The Serial Management Interface defined by IEEE 802.3 is a single master bus. The MDC clock is generated by the bus master, typically an Ethernet MAC. To use the USB-2-MDIO GUI, connections must be made directly between the MSP430 Launchpad and the DP83826 MDIO and MDC pins.

- MSP430 Pin 4.2 → PHY's MDIO Pin
- MSP420 Pin 4.1 → PHY's MDC Pin

3.8.2 Extended Register Access

To read and write registers in extended register space, refer to the following procedures:

Write procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

write reg<000E> = <value>

Read procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

read reg<000E>

Note

To read/write MMD "1" registers, replace 1F with 01.

Note

Above write and read procedure is normally used for registers with address greater than 0x001F, but the procedure can also be used for any address in gernal.

3.8.3 Application Note References

Refer to the following application notes for information on hardware and software configurations for EMC.EMI compliance tests:

4 Conclusion

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations will help ease board bring up and initial evaluation of DP83826 designs.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2023	*	Initial Release

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