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Application Report

AN-1328 Using Built-In Self-Tests (BIST) With SCAN50C400

ABSTRACT

The SCAN50C400 is a high-speed backplane serializer/deserializer (SerDes) with four channels of 5 Gbps serializers and de-serializers capable of error-free data transmission across a backplane. It provides a total through-put of 20 Gbps in each direction (40 Gbps total throughput), providing a cost-effective migration path to higher bandwidth line cards while maintaining backwards compatibility to legacy 1.25 Gbps or 2.5 Gbps line cards.

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TEXAS
INSTRUMENTS

1   Introduction

Testing high speed serdes at multi-gigabit data rates poses a huge challenge for both chip vendors and system vendors. To assist vendors with test verification, the SCAN50C400 is equipped with built-in self-test (BIST) and internal loopback modes to support both system manufacturing and field diagnostics. These features provide a simple method for a system host to perform diagnostic testing of the serializer and de-serializer. The BIST function is easily configured through the MDIO serial control interface. Figure 1 shows the functional block diagram of the SCAN50C400, highlighting the BIST functions of one channel. This application note provides detailed information on how to use the BIST and loopback modes.
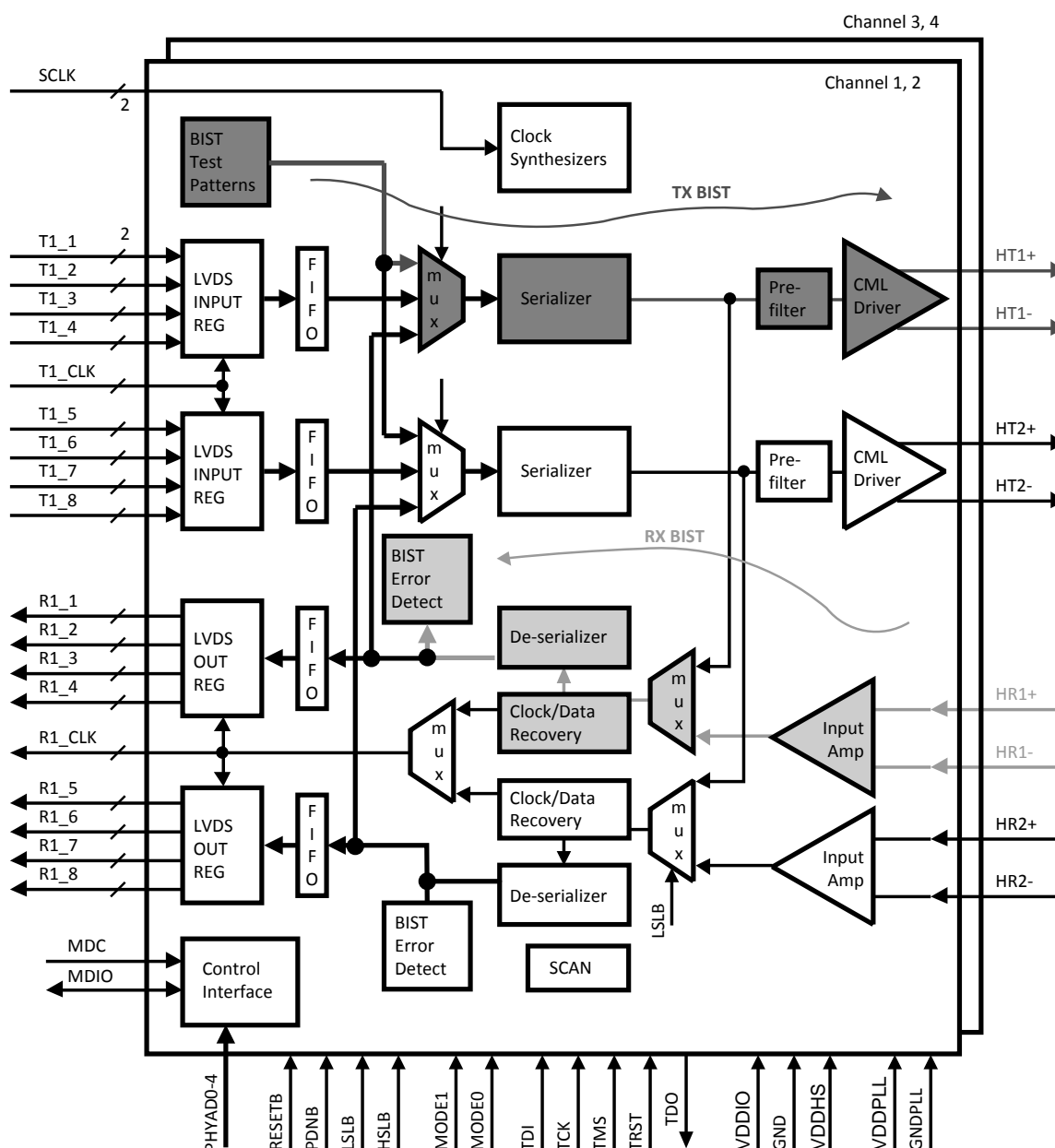
BIST Signal Paths of Channel 1 Highlighted

Figure 1. Functional Block Diagram of the SCAN50C400

2 Transmit BIST

The Transmit BIST (TX BIST) circuitry contains a pseudo-random word (PRW) pattern generator, a 256-bit memory-based pattern generator, synchronization header generator and the necessary control logic. Each serializer of the SCAN50C400 can be individually programmed into the TX_BIST mode through the MDIO serial control interface. In the TX BIST mode, one of four test patterns (described in the following sections) can be activated, serialized and output at the high-speed CML drivers. The TX BIST data path is shown in Figure 1. Figure 4 shows the eye-diagrams of some commonly used test patterns.

PRW Patterns

An internal eight-bit pseudo-random word generator supports pseudo-random patterns with polynomial orders of 7 and 13 to provide more flexibility in testing. The 8-bit word is serialized and output as a serial test pattern at the CML output driver. These two pseudo-random word patterns are labeled as PRW7 and PRW13. Note: built-in pseudo-random word patterns do not conform to International Telecommunication Union (ITU) serial bit stream standards.

ZERO-PRW7-ONE Pattern

This test pattern consists of 1.6ns of continuous zero's, followed by a PRW7 pattern, then 1.6ns of continuous one's, see Figure 2

ONE-PRW7-ZERO Pattern

This test pattern consists of 1.6ns of continuous one's, followed by a PRW7 pattern, then 1.6ns of continuous zero's, see Figure 2

Memory-Based Pattern

Registers 30.16 to 30.31 store a 256-bit user-defined bit sequence. When a memory-based pattern is selected and TX BIST is activated, D0 of register 30.16 is the first bit of the test pattern transmitted. After the last bit (D15 of register 30.31) is transmitted, the SCAN50C400 will loop the test pattern and continue at D0 of register 30.16, forming a 256-bit repeating fixed pattern. The bit sequence used in the memory should be DC-balanced and with a run length of less than 20-bits.

TX Fixed-Pattern Registers

(Offset = 30.16 - 30.31)

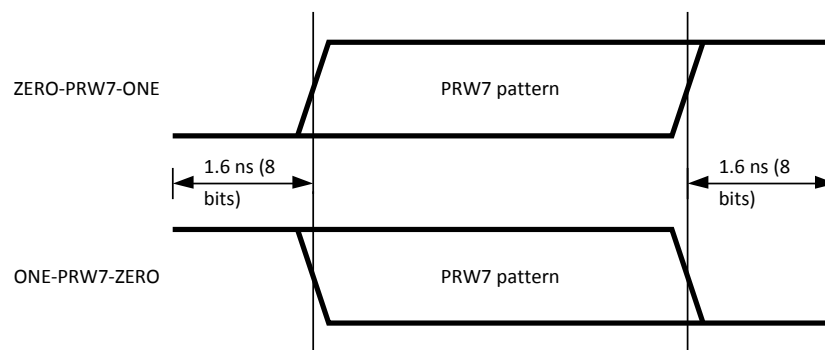| Bit	Bit Name	Access	Default	Description
15:0	TX_PAT	RW	AAAA 'h	Registers 30.16 to 30.31 stores the 256-bit bit sequence as the test pattern when memory-based pattern is selected and TX BIST is activated.

Figure 2. ONE-PRW7-ZERO or ZERO-PRW7-ONE Pattern

Figure 3. PRW7 Pattern
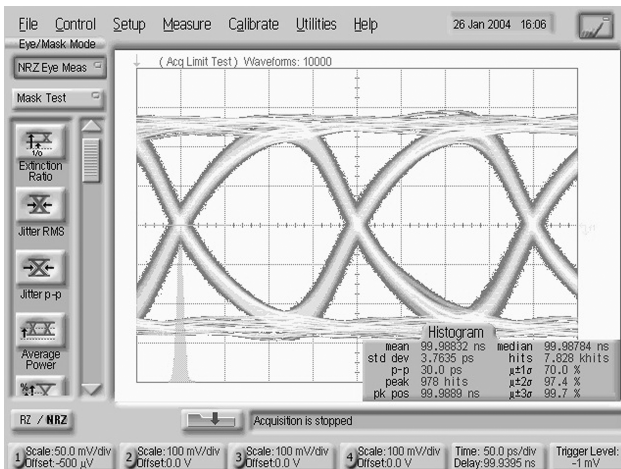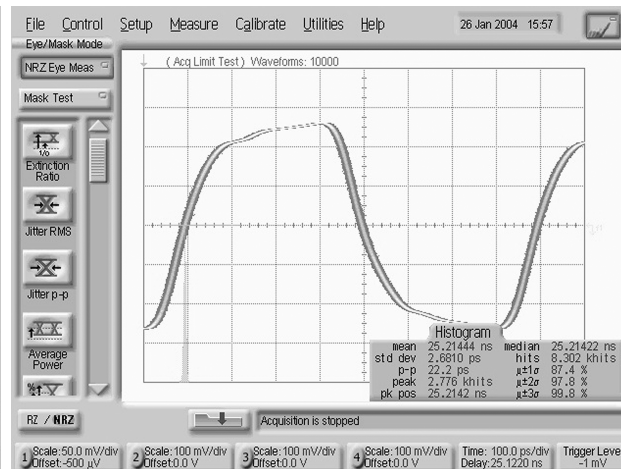
Eye Diagram and Waveforms of TX BIST Test Patterns
Figure 4. Memory-Based: Alternating-1100 Pattern
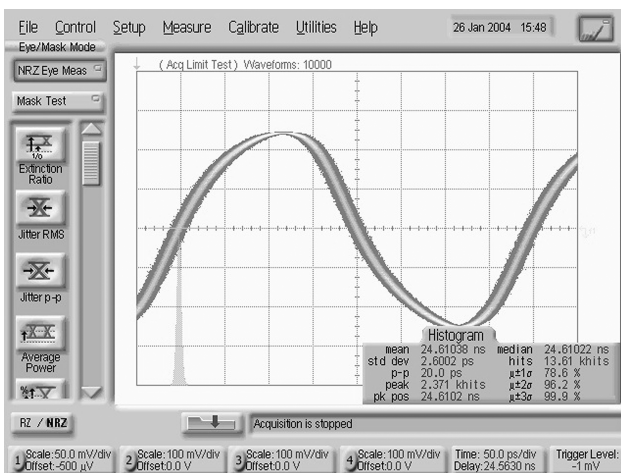
Figure 5. Memory-Based: Alternating-10 Pattern
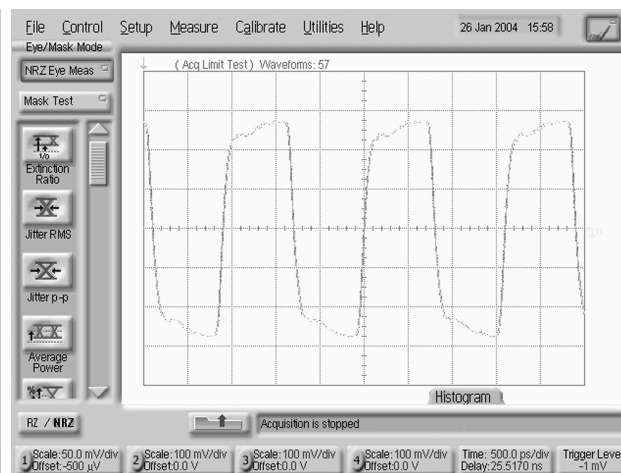
Eye Diagram and Waveforms of TX BIST Test Patterns
Figure 6. Memory-Based: Alternating-11110000 Pattern

Selecting a TX BIST Pattern

Register 30.12 selects the PRWS or memory-based pattern.

BIST TX Control Register

(Offset = 30.12)

Bit 15:0	Description
3FF1 'h	Selects PRW7 test pattern.
3FF5 'h	Selects PRW13 test pattern.
3FF3 'h	Selects ONE-PRW7-ZERO pattern. (See Figure 2)
3FF2 'h	Selects ZERO-PRW7-ONE pattern. (See Figure 2)
3FF0 'h	Selects Memory-based test pattern defined by registers 30.16 to 30.31.

Synchronization Header

A header is sent preceding the selected test pattern when the TX BIST is first activated. This header is used to synchronize the downstream receiver's RX BIST circuitry such that the RX BIST can determine the proper bit boundary when comparing against the expected bit sequence for error detection. For a graphical representation, see Figure 7.

Activating the TX BIST

Bits 3:0 of register 30.11 activate or de-activate the TX BIST mode for one or all of the four serializers. In normal serdes mode, data from T1_D[1:8] or T2_D[1:8] is transmitted. When TX BIST mode is activated, the switch-over from the normal data path (T1_D[1:8] or T2_D[1:8]) to the selected test pattern occurs at the next clock cycle of the internal 625 MHz nibble clock. Similarly, when the TX BIST mode is de-activated, the last data word of the test pattern is sent out before exiting and reverting back to normal serdes mode..

While the TX BIST is activated, users **should not** change the contents of registers 30.12, 30.16–31. Any change in the TX BIST test pattern will take effect only after the TX BIST mode is disabled and re-activated.
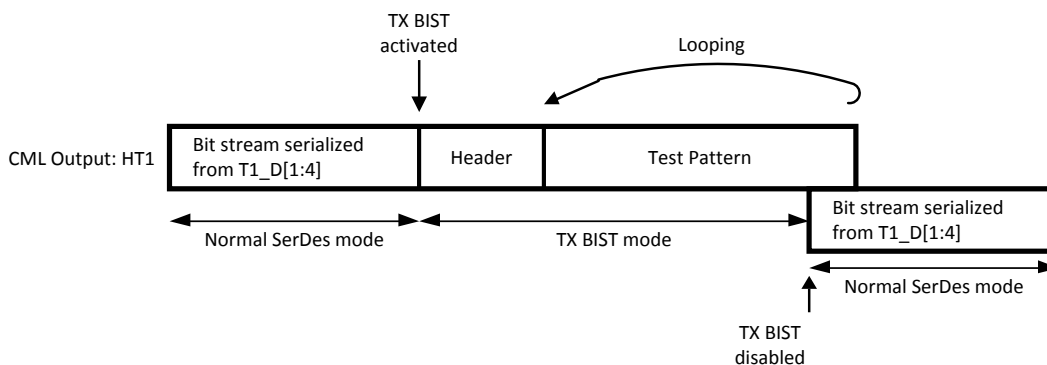

Figure 7. Serial Bit Stream Output From CML Output Before and After TX BIST Mode

3   Receive BIST

The Receive BIST (RX BIST) circuitry consists of header detection, error detection, and the necessary control logic. Each de-serializer can be individually programmed into the RX BIST mode through the MDIO serial control interface. When the RX BIST mode is activated, the de-serializer is ready to detect a synchronization header from the upstream transmitter. Once a valid synchronization header is detected, the device establishes the proper bit boundary for comparing the recovered data against the expected bit sequence selected by the user. The BIST test result is reported in the BIST Status Register of each de-serializer. An 8-bit counter is used to store the number of errors detected (0 to 255 max).

Receive Test Patterns

The user selected test pattern is compared against the incoming bit stream recovered by the receiver for error detection. The receive test pattern must be identical to the test pattern sent out by the upstream transmitter.

PRW Patterns

An internal eight-bit pseudo-random word generator supports pseudo-random patterns with polynomial orders of 7 and 13 to provide more flexibility in testing. These two pseudo-random word patterns are labeled as PRW7 and PRW13. Note: built-in pseudo-random word patterns do not conform to ITU serial bit stream standards.

ZERO-PRW7-ONE Pattern

This test pattern consists of 1.6ns of continuous zero's, followed by a PRW7 pattern, then 1.6ns of continuous one's, see Figure 2.

ONE-PRW7-ZERO Pattern

This test pattern consists of 1.6ns of continuous one's, followed by a PRW7 pattern, then 1.6ns of continuous zero's, see Figure 2.

Memory-Based Pattern

There are 16 registers (30.32 to 30.47) for users to store 256 bits of user-defined data. When selected, these bits are compared against the incoming bit stream. When the de-serializer's BIST mode is turned on and a fixed pattern is selected, the on-chip BIST Error Detector will compare the recovered data bits against the user-defined data bits stored in registers 30.32–30.47. This only occurs after a valid synchronization header is detected. D0 of register 30.32 is the first expected receive bit, and D15 of register 30.47 is the last expected receive bit.

RX Fixed-Pattern Registers

(Offset = 30.32 -30.47)

Bit	Bit Name	Access	Default	Description
15:0	RX_PAT	RW	AAAA 'h	Registers 30.32 to 30.47 store 256 bits of user-defined data bit sequence that are used as the expected data for comparing the recovered bit stream. D0 of register 30.32 is the first expected receive bit.

Selecting a RX BIST Pattern

Register 30.13 selects the expected test pattern for error detection.

BIST RX Control Register

(Offset = 30.13)

Bit 15:0	Description
3FF1 'h	Selects PRW7 test pattern.
3FF5 'h	Selects PRW13 test pattern.
3FF3 'h	Selects ONE-PRW7-ZERO pattern.
3FF2 'h	Selects ZERO-PRW7-ONE pattern.
3FF0 'h	Selects Memory-based test pattern defined by registers 30.32 to 30.47.

Activating the RX BIST

Bits 7:4 of Register 30.11 activate or de-activate the RX BIST mode for one or all four de-serializers.

RX BIST Status

Registers 30.57 – 30.60 report the BIST status of channels 1:4. Bit 8 reports whether any errors occurred after a valid synchronization header was received. If Bit 8 reports errors occurred, Bits 7:0 will report the number of errors detected.

Table 1. BIST Status Registers [1]

Bit	Bit Name	Access	Default	Description
15:12	Reserved	NA		Reserved.
11	BIST_HDR	RO	0'b	Transmitter sends a header and then stays high until BIST is de-activated.
10	BIST_ST	RO	0'b	BIST_ST = 1 indicates detection of a synchronization header.

[1] Channel 1 (Offset = 30.57)
Channel 2 (Offset = 30.58)
Channel 3 (Offset = 30.59)
Channel 4 (Offset = 30.60)

Table 1. BIST Status Registers [1] (continued)

Bit	Bit Name	Access	Default	Description
9	BIST_END	RO	0′b	After the user disables the de-serializer's BIST mode (D7-4 of Control Register 2, offset 30.11), the SCAN50C400 will complete processing the last data word and then exit BIST mode. BIST_END is set high to indicate completion of the receiver's BIST error detection.
8	BIST_OK	RO	0′b	BIST_OK = 0 indicates no error was detected. BIST_OK is valid only after BIST_ST is at a logic 1 state.
7:0	BIST_ERR	RO	FF′h	BIST_ERR is an 8-bit error counter that tells the number of errors detected by the internal BIST. When the error counter overflows, it will stay at FF′h. BIST_ERR is valid only if BIST_ST is at logiic 1. BIST_ERR is set to default values after reset and is cleared after RX BIST has been re-started. BIST_ERR has a value of 0-255.

4   Activating and De-Activating BIST

The SCAN50C400 supports BIST at 5 Gbps when MODE0 and MODE1 are driven low. It is recommended to activate RX BIST while the upstream transmitter is at its normal serdes mode, sending out data serialized from its parallel inputs (T1_D[1:8] and T2_D[1:8]). This ensures the receiver's PLL's are locked to the incoming bit stream sourced from its upstream transmitter before entering the RX BIST mode. When TX BIST is activated at its upstream transmitter, the transition from normal data path to the selected test pattern occurs at the next clock cycle of its internal 625 MHz nibble clock. This transition will not cause the receiver's PLL's to lose lock and ensures the receiver's are ready to receive the synchronization header at any time. Once a valid synchronization header is detected, the device establishes the proper bit boundary for comparing the recovered data against the expected bit sequence, and error detection begins. Once BIST testing is complete, it is recommended to de-activate RX BIST before de-activating the TX BIST mode. To avoid sending out a quiet state at the transmitter's CML driver while entering and exiting TX BIST mode, T1_D[1:8] and T2[1:8] should be sourced with valid data and T1_CLK and T2_CLK should be running.

5   Using BIST With Internal Loopback Modes

The internal loopback modes of the SCAN50C400 further enhance its self-test capabilities. With LVDS Loopback mode (also called serial loopback), the TX BIST and the RX BIST provide a self-diagnostics data path through the serializer and de-serializer, with the exception of the LVDS I/O's and the high speed CML I/O's. With High-speed Loopback (HSLB) mode activated on a remote device and the TX BIST and RX BIST modes activated on a local device, the SCAN50C400 provides a powerful self-diagnostics data path through the local device, the transmission medium, and the remote device. For a graphical representation, see Figure 9.

Table 2. Example: BIST Running a PRW7 Test Pattern With Internal LVDS Loopback Mode

Operation	Descriptions
Drive MODE0 to low and MODE1 to low	Sets device to 5 Gbps mode.
Drive LSLB to low and HSLB to high	Sets device to internal LVDS Loopback mode.
Drive T1_D[1:8] and T2_D[1:8] with valid data with T1_CLK and T2_CLK running	Transmitter sends a valid serial bit stream that loops back to the receiver. Receiver PLL's lock to the transmitter's bit stream.
Write Reg 30.12 to 3FF1 ′h	Selects PRW7 as the TX BIST pattern.
Write Reg 30.13 to 3FF1 ′h	Selects PRW7 as the RX BIST pattern.
Write Reg 30.11 to 00F0 ′h	Activates RX BIST. Receivers are still locked to the data stream and are ready to detect the synchronization header.
Write Reg 30.11 to 00FF ′h	Activates TX BIST. Transmit data switched to the bit sequence defined by the selected TX BIST pattern, preceded by a synchronization header. The user should start the timer for error rate measurement at this point.

Table 2. Example: BIST Running a PRW7 Test Pattern With Internal LVDS Loopback Mode (continued)

| Operation	Descriptions
Read Reg 30.57-60	Reads BIST Status registers for the 4 channels. Should read 00C0 ′h if no errors were detected. Should read 00Dx ′h if errors are detected. The decimal value of x (0 to 255 max) is the number of errors detected. Keep polling these four status registers for an error count for the entire duration of the BIST test. The user should keep track of the elapsed time for the test. To achieve an error rate of 10^{-12}, the elapsed time is 200 seconds. To achieve an error rate of 10^{-14}, the elapsed time is 5 hours, 33 minutes, and 20 seconds.
Write Reg 30.11 to 000F ′h	Disables RX BIST to terminate error detection while TX BIST is still running.
Write Reg 30.11 to 0000 ′h	Disable TX BIST. Transmitter returns to normal serdes mode and sends data sourced from T1_D[1:8] and T2_D[1:8].
Drive LSLB to high and HSLB to high	Exits LVDS Loopback mode and returns to the normal serdes mode.
Drive MODE0 and MODE1 to the states corresponding to the intended data rate	Sets device to the desired data rate.
Toggle RESETB low for 10 millisecond	Executes a hardware reset to prepare the device for normal operation.

6   Using BIST With Internal Loopback Modes
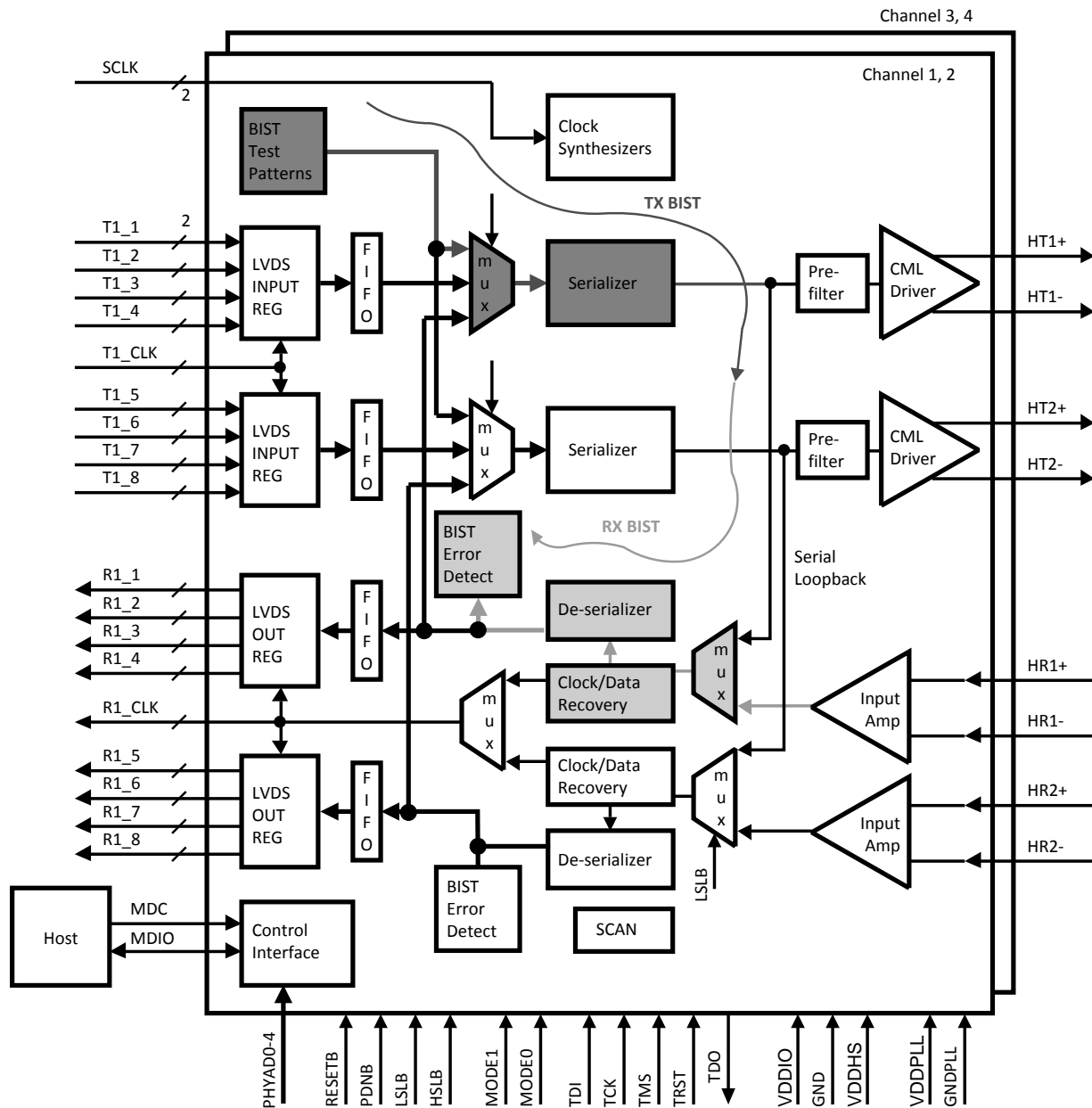
Figure 8. Using BIST With LVDS Loopback Mode (Channel 1 Highlighted)
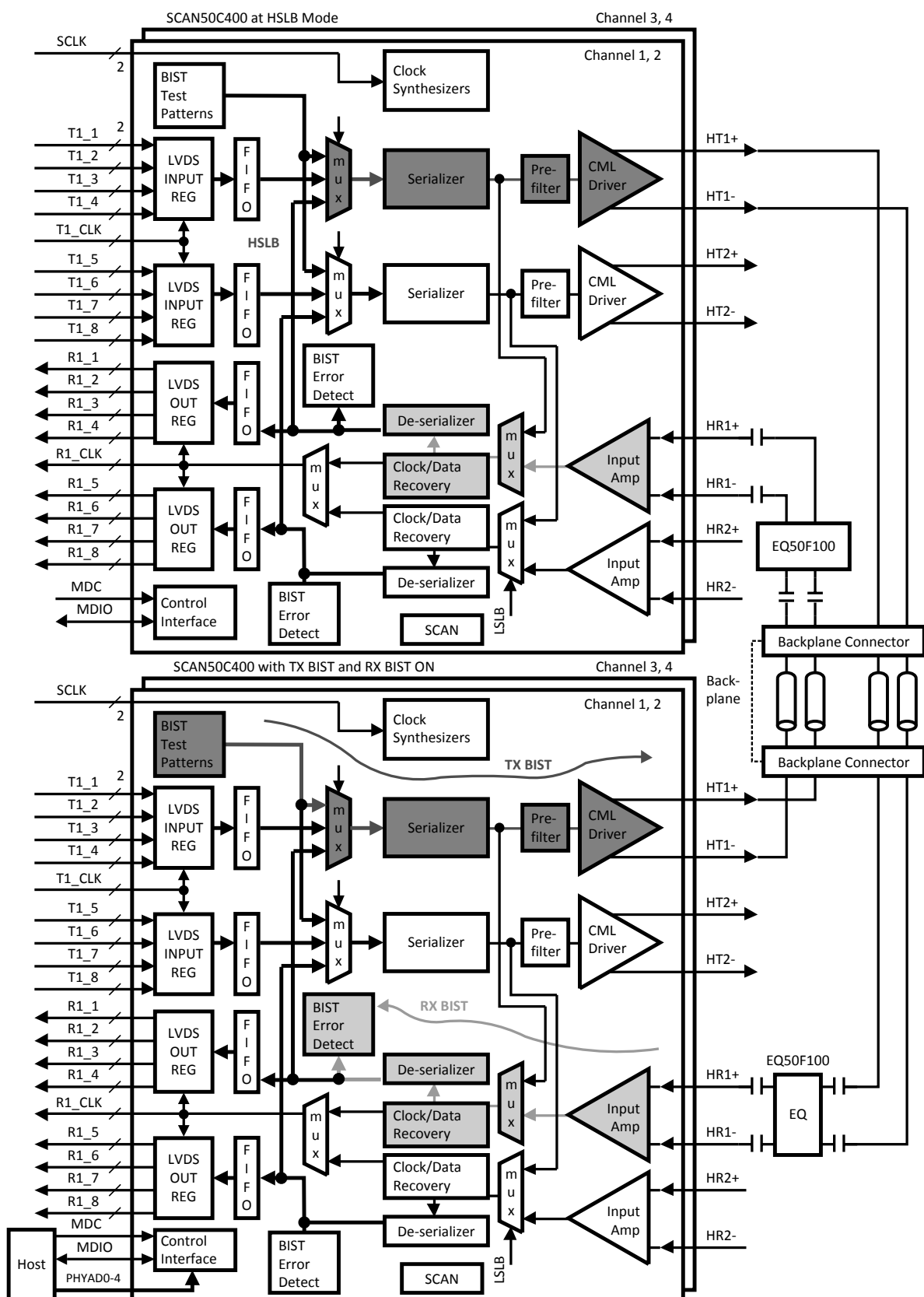
Figure 9. Using BIST With High-Speed Loopback Mode (Channel 1 Highlighted)

7   References

SCAN50C400A 1.25/2.5/5.0 Gbps Quad Multi-Rate Backplane Transceiver Data Sheet ([SNOSA22](#))

Appendix A MDIO Registers for BIST Operations

Table 3. Registers for BIST operations

Register Offset	Access	Description
30.11	RW	Control Register 2.
30.12	RW	BIST TX Control Register.
30.13	RW	BIST RX Control Register.
30.16-31	RW	TX Fixed Pattern Registers.
30.32-47	RW	RX Fixed Pattern Registers.
30.57	RO	BIST Status Register for Channel 1.
30.58	RO	BIST Status Register for Channel 2.
30.59	RO	BIST Status Register for Channel 3.
30.60	RO	BIST Status Register for Channel 4.

BIST TX Control Register (Offset = 30.12)

BIST RX Control Register (Offset =30.13)

Bit 15:0	Description
3FF1 'h	Selects PRW7 test pattern.
3FF5 'h	Selects PRW13 test pattern.
3FF3 'h	Selects ONE-PRW7-ZERO pattern.
3FF2 'h	Selects ZERO-PRW7-ONE pattern.
3FF0 'h	Selects Memory-based test pattern defined by registers 30.16 to 30.31.

TX Fixed-Pattern Registers (Offset = 30.16 - 30.31)

Bit	Bit Name	Access	Default	Description
15:0	TX_PAT	RW	AAAA 'h	There are 16 registers (30.16 to 30.31) for users to store 256 bits of user-defined data bits to be transmitted at HT when TX BIST is enabled. All 256 bits are transmitted sequentially. D0 of register 30.16 is the first bit transmitted. After the last bit (D15 of register 30.31) is transmitted, the SCAN50C400 will loop the test pattern and re-start at D0 of register 30.16, forming a repeating fixed pattern.

RX Fixed-Pattern Registers (Offset = 30.32 - 30.47)

Bit	Bit Name	Access	Default	Description
15:0	RX_PAT	RW	AAAA 'h	There are 16 registers (30.32 to 30.47) for users to store 256 bits of user-defined data. When selected, these bits are compared against the incoming bit stream. When the de-serializer's BIST mode is turned on and a fixed pattern is selected, the on-chip BIST Error Detector will compare the recovered data bits against the user-defined data bits stored in registers 30.32–30.47. This only occurs after a valid synchronization header is detected. D0 of register 30.32 is the first expected receive bit.

Control Register 2 (Offset = 30.11)

Bit	Bit Name	Access	Default	Description
15:12	DISABLE_LVDS	RW	0'h	Disables the LVDS output stages of an individual de-serializer, during which the LVDS outputs are held at logic high (+VOD). D15 = 1: Disables the LVDS outputs for CH4 (R2[5-8]±) D14 = 1: Disables the LVDS outputs for CH3 (R2[1-4]±) D13 = 1: Disables the LVDS outputs for CH2 (R1[5-8]±) D12 = 1: Disables the LVDS outputs for CH1 (R1[1-4]±) The user is required to set D15:12 to 0'h for normal operating mode.

Bit	Bit Name	Access	Default	Description
11:8	DISABLE_HT	RW	0′h	Disables the high-speed CML output stages of an individual serializer, during which both the high-speed outputs HT+ and HT- are forced to static high. During LVDS loopback test mode and when BIST is enabled, DISABLE_HT is automatically overridden. D11 = 1: Disables the high-speed CML outputs for CH4 (HT4±) D10 = 1: Disables the high-speed CML outputs for CH3 (HT3±) D9 = 1: Disables the high-speed CML outputs for CH2 (HT2±) D8 = 1: Disables the high-speed CML outputs for CH1 (HT1±) The user is required to set D11:8 to 0′h for normal operating mode.
7:4	EN_BIST_RX	RW	0′h	Enables built-in self-test (BIST) for an individual de-serializer. The receiver will start looking for a synchronization header from the incoming bit stream. When a valid header is detected, the error detection function is activated automatically. Any error detected will be reported to bits 7:0 of the BIST Status Registers. D7 = 1: Enables BIST for the Channel 4 de-serializer. D6 = 1: Enables BIST for the Channel 3 de-serializer. D5 = 1: Enables BIST for the Channel 2 de-serializer. D4 = 1: Enables BIST for the Channel 1 de-serializer. The uer is required to set EN_BIST_RX to 0′h for normal operating mode. Note: the BIST function overrides any output enable controls.
3:0	EN_BIST_TX	RW	0′h	Enables built-in self-test (BIST) for an individual serializer. The selected test pattern will be sent out at HT± of the serializer. When EN_BIST_TX is de-asserted, the last data word is sent out before terminating self-test test mode. D3 = 1: Enables BIST for the Channel 4 serializer. D2 = 1: Enables BIST for the Channel 3 serializer. D1 = 1: Enables BIST for the Channel 2 serializer. D0 = 1: Enables BIST for the Channel 1 serializer. The user is required to set EN_BIST_TX to 0′h for normal operating mode. Note: the BIST function overrides any output enable controls.

BIST Status Registers – —Channel 1 (Offset = 30.57)
Channel 2 (Offset = 30.58)
Channel 3 (Offset = 30.59)
Channel 4 (Offset = 30.60)

Bit	Bit Name	Access	Default	Description
15:12	Reserved.	NA		Reserved.
11	BIST_HDR	RO	0′b	Transmitter sends a header and then stays high until BIST is de-activated.
10	BIST_ST	RO	0′b	BIST_ST = 1 indicates detection of synchronization header.
9	BIST_END	RO	0′b	After the user disables the de-serializer's BIST mode (D7-4 of Control Register 2, offset 30.11), the SCAN50C400 will complete processing the last data word and then exit BIST mode. BIST_END is set high to indicate completion of the receiver's BIST error detection.
8	BIST_OK	RO	0′b	BIST_OK = 0 indicates no error has been detected. BIST_OK is valid only after BIST_ST is at logic 1 state.
7:0	BIST_ERR	RO	FF′h	BIST_ERR is an 8-bit error counter that contains the number of errors detected by the internal BIST error detector. When the error counter overflows, it will stay at FF′h. BIST_ERR is valid only if BIST_ST is at logic 1. BIST_ERR is set to the default values after reset, and cleared after RX BIST has been re-started. BIST_ERR has a value of 0-255.

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