Application Report

AN-1516 SPICE Universal Test Circuits

Soufiane Bendaoud, Carolina Gomez, Gerasimos Madalvanos, Bala Ravi

ABSTRACT

This application report provides a collection of circuits that allow users to test any operational amplifier (op amp) macro model. A macro model is a SPICE (Simulation Program with Integrated Circuit Emphasis) circuit component that resembles the functioning of a real-world device. The models are uniquely configured to mimic lab tested or data sheet specifications of an op amp.

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1 Introduction

While IC manufacturers strive to provide their customers with accurate models, it is really the application engineers who dictate the trend of this accuracy and the innovation in the development of SPICE macro models. Engineers use op amp models with a SPICE simulator such as TINA-TI™or PSpice® for TI to evaluate performance of new devices, sometimes even before they are released to market. A primary benefit of using SPICE simulations is providing a rapid, low-cost functional testing of a circuit, without reliance on samples or lab equipment.

Accurate op amp macro models can be an extremely helpful design tools. However, inaccurate models can lead to false assumptions about an op amp's performance and must be used with discretion. When using SPICE models, it is important to understand both their limitations and capabilities. Carefully set the test environment to ensure accurate representation of the amplifier performance; this is best done by following the conditions outlined in the data sheet.

2 What Parameters Should Be Tested?

Macro models differ in their level of complexity. Much like data sheets, the models should emulate parameters that are relevant to applications in which the op amp is thought to be appropriate. For example if a rail-to-rail output op amp is used, then the user should be able to test and verify the output voltage versus the output current (claw curves). Likewise, a low noise amplifier should have a model that emulates at least the voltage noise among other modeled parameters.

Despite their differences, amplifier macro models have a lot in common; these parameters are of the greatest interest and they are usually the starting point of the simulation. Below is a list of these parameters along with the corresponding test circuits and the simulations, which may be downloaded here: AN1516 Test Circuits.

2.1 Open-Loop Gain (A_{OL}) and Phase Margin

The open-loop gain versus frequency is important because it shows the DC gain, the dominant pole, the unity gain bandwidth and the phase margin. Figure 2-1 shows the circuit to test *Open Loop Gain and Phase Margin Test Circuit*. At DC, the capacitor is open and the inductor is short creating a feedback loop from output to inverting input of the op amp. At higher frequencies, the capacitor is a short and the inductor is open, this places the op amp in an open loop configuration. The capacitor and inductor values are chosen to be large to provide an early roll off [as seen in the formula below (1)] so that even if the op amp tested has a very low frequency dominant pole, the simulation shows a smooth transition and 20 dB per decade roll off. For more information on performing op amp stability analysis, please refer to the Texas Instruments Precision Labs video series on stability.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

When testing open-loop gain and phase, the user should choose an upper frequency limit that goes beyond the unity-gain bandwidth of the amplifier. In the example provided, the unity-gain bandwidth of OPA191 is 2.5 MHz, Figure 2-2 shows the simulated A_{OL} plot for OPA191 and Figure 2-3 shows the data sheet A_{OL} plot for OPA191.

When using rail-to-rail output models, it is important to use the test circuit with the same load (R_L and C_L) indicated in the data sheet, otherwise the result might not reflect the actual amplifier's capabilities. This is especially true about the DC gain (in consideration with formula 2). In the example provided, the OPA191 data sheet specifies an R_L of 10 kΩ and C_L of 100 pF.

$$A_{OL} = g_m \times R_L \tag{2}$$

For a more complete simulation test analysis, please refer to the following EDN article, authored by Ian Williams. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

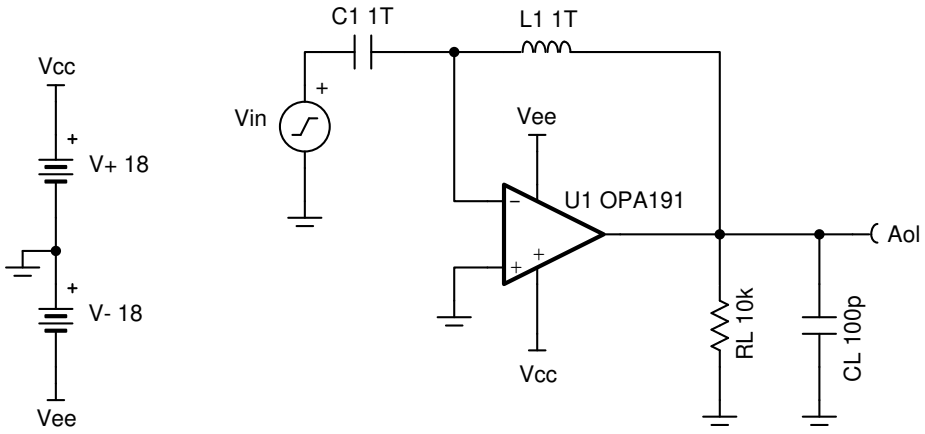

Figure 2-1. Open-Loop Gain and Phase Margin Test Circuit

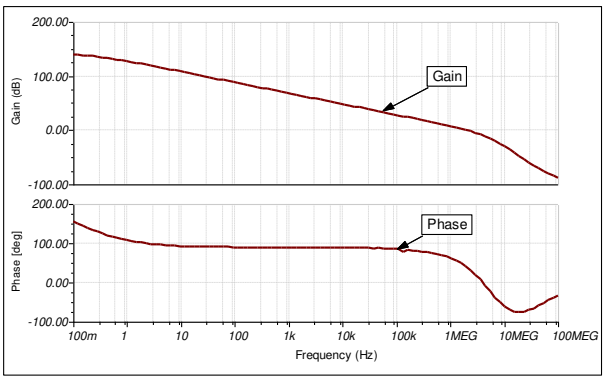

Figure 2-2. Simulated Open-Loop Gain and Phase for OPA191

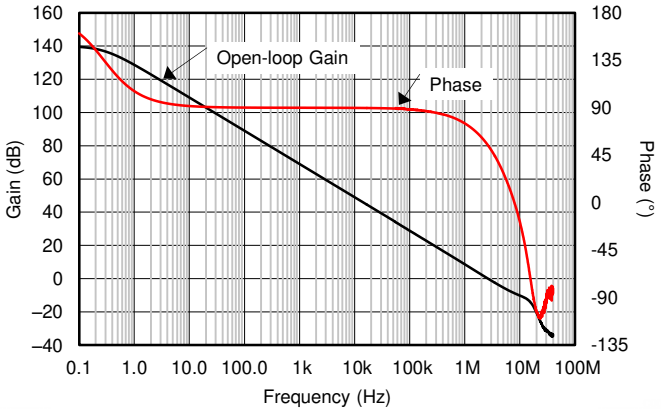

Figure 2-3. Data sheet Graph of Open Loop Gain and Phase for OPA191

2.2 Slew Rate

Slew Rate is a measure of how fast an op amp's output can change. Slew rate is related to the ratio of the tail current and the compensation capacitance inside the op amp.

To measure slew rate, use a simple buffer circuit as shown in Figure 2-4. It is important to use the test circuit with the same load (R_L and C_L) indicated in the data sheet, in this example the OPA2990 data sheet specifies R_L of 10 kΩ and a C_L of 20 pF. This test circuit inputs a square wave and generates an output in which the slope of the rising edge and falling edge is the slew rate. The amplitude and time at 10 percent and 90 percent of the output's amplitude is used to calculate the slope, or slew rate. For more information on slew rate please refer to Texas Instruments Precision Labs video series on slew rate.

To assure this test circuit works properly, the square wave input should have an amplitude large enough so that the effects of slew rate limitation dominate. When running the simulation for slew rate, make sure the input signal rise and fall times are shorter the amplifier's expected slew rate. This is to ensure that the test results are dominated by the amplifier's slew rate. On the other hand, choose the input signal frequency accordingly with the op amp's speed. An input signal that's too fast will give you convergence problems. Figure 2-5 shows the simulated slew rate for OPA2990 and it corresponds with Figure 2-6 that shows the data sheet specification for slew rate. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

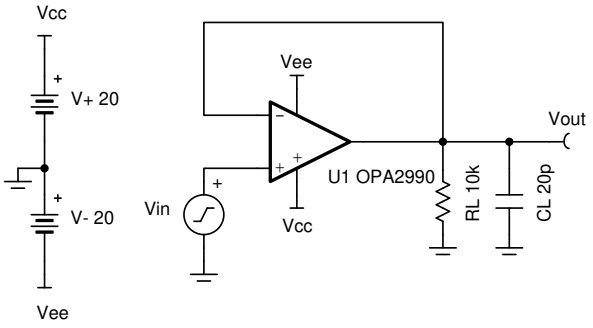

Figure 2-4. Slew Rate Test Circuit

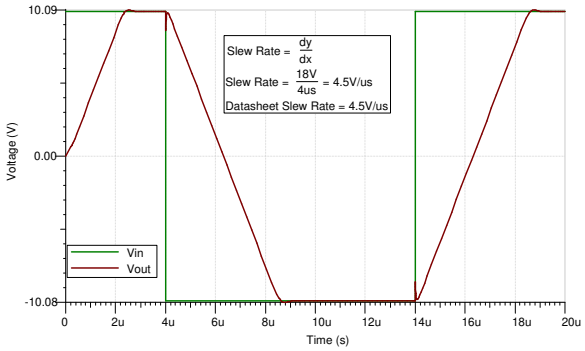

Figure 2-5. Simulated Slew Rate for OPA2990

SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF	4.5	V/µs

Figure 2-6. Data Sheet Specification of Slew Rate for OPA2990

2.3 Common-Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR)

Common-Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR) are two parameters not always modeled but they can be equally important. Common mode voltage is defined as the average voltage at both inverting and non-inverting input of an op amp.

$$\text{Common Mode} = \frac{\text{In}_+ + \text{In}_-}{2} \tag{3}$$

CMRR quantifies how well an op amp rejects common mode signals, such as common mode noise. Hence, higher value is better because more of the common mode signal is rejected and therefore has less effect on the op amp. Common mode effect on output can be shown as follows:

$$V_{out} = (V_{diff} + V_{CM}) \times \text{Gain} \tag{4}$$

CMRR changes across frequency. CMRR is highest at lower frequencies, usually in the range of 80 dB to 160 dB at DC. CMRR rolls off at higher frequencies, so when selecting a device make sure CMRR performance is sufficient at higher frequcies of interest. CMRR is especially important in non-inverting configurations because the common-mode voltage is equal to the input voltage. CMRR is defined as the ratio of op amp's open-loop differential gain (ADM) to its open-loop common mode gain (ACM). In reality, these two gain characteristics can be tricky to isolate from one another. Luckily, the power of simulation allows the user to do it effectively. For more information on CMRR please refer to Texas Instruments Precision Labs video series on CMRR.

$$\text{CMRR} = \frac{\text{ADM}}{\text{ACM}} \tag{5}$$

Figure 2-7 below shows "CMRR Test Circuit". This test circuit uses two copies of an op amp under test to measure the ADM and ACM separately. In the top circuit, AC source V_{IN} is applied to both input of op amp to create a clean common mode input signal. Inductor L_1 acts as a short at DC and an open circuit at AC to allow for both a valid DC operating point and measurement of the ACM.

In the bottom circuit, AC source V_{IN} is routed to voltage controlled voltage sources E1 and E2. This generates a differential version of V_{IN} biased around 0V, which is then applied to the input of the op amp. Similar to the top circuit, inductor L_2 acts as a short circuit at DC and open circuit at AC to allow for both a valid DC operating point and measurement of ADM.

It is important to check the DC operating point to ensure that the op amp is operating in its linear region. Make sure to match the specified data sheet conditions such as: power-supply voltage common mode voltage, capacitive and resistive loads (C_L and R_L). To measure CMRR, run an AC transfer characteristics over the

desired frequency range and plot the magnitude in dB for ACM and ADM. Then use the post-processing tool to generate the curve for ADM over ACM (the definition of CMRR). Figure 2-10 shows the simulated CMRR result for TLV9102. For a more complete simulation test analysis, please refer to the following EDN article, authored by Ian Williams. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

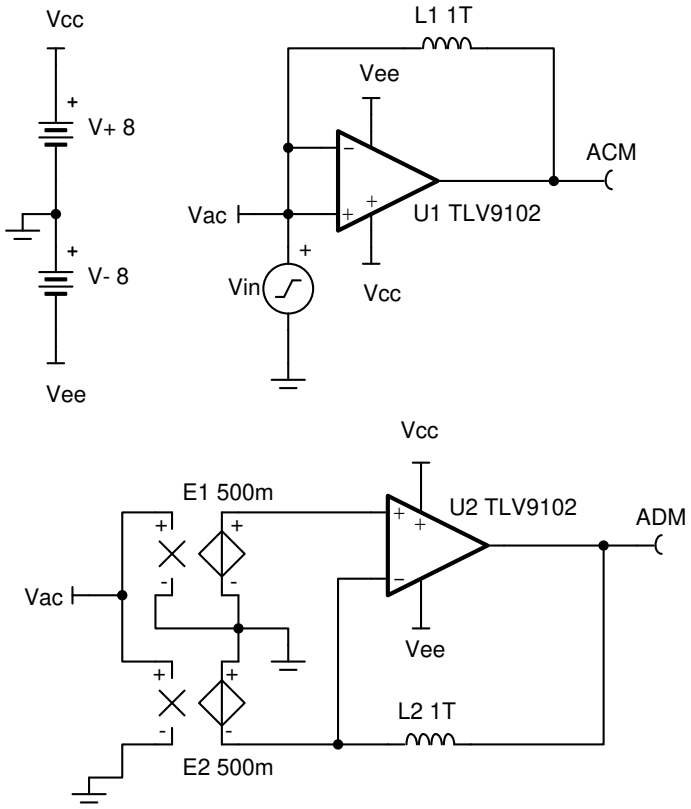

Figure 2-7. Common-Mode Rejection Ratio (CMRR) Test Circuit

PSRR is defined as the ratio of the signal applied to either op amp power supply pin versus the resulting input offset voltage as shown in the equation below. PSRR specifies how well an op amp rejects the signal present at its power supply pins. Similar to CMRR, PSRR changes over frequencies, specifically it is less at higher frequencies. This is a concern when using switching power supply that switches at frequencies above the unity-gain bandwidth of the op amp, so make sure to use appropriate filtering and decoupling. For more information on PSRR please refer to Texas Instruments Precision Labs video series on PSRR.

$$\text{PSRR} = \frac{V_{\text{IN (Supply)}}}{V_{OS}} \tag{6}$$

It is important to simulate and test both PSRR+ and PSRR-. Some data sheets give only one PSRR value, which can imply that the same PSRR applies to both supplies.

Figure 2-8 shows the recommended "PSRR+ Test Circuit" and Figure 2-9 shows the recommended "PSRR- Test Circuit." These test circuits have an additional AC source "V_{IN}" in series with one of the power supply voltages to generate DC plus AC signal. The op amp is placed in a standard unity gain buffer configuration with its non-inverting input shorted to ground. The induced offset voltage across the op amp input pins (V_{OS}) is measured.

PSRR is important in any application where the voltage supply is susceptible to any interference or for DC PSRR where the supplies can experience signification variation. To plot PSRR, run an AC transfer characteristics over the desired frequency range, then using the post-processing tool generate the curve for V_{IN} over V_{OS} (the definition of PSRR).

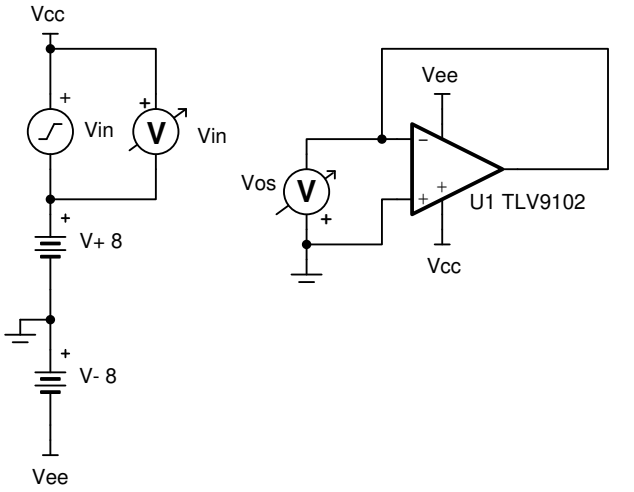

Figure 2-8. Power Supply Rejection Ratio (PSRR+) Test Circuit

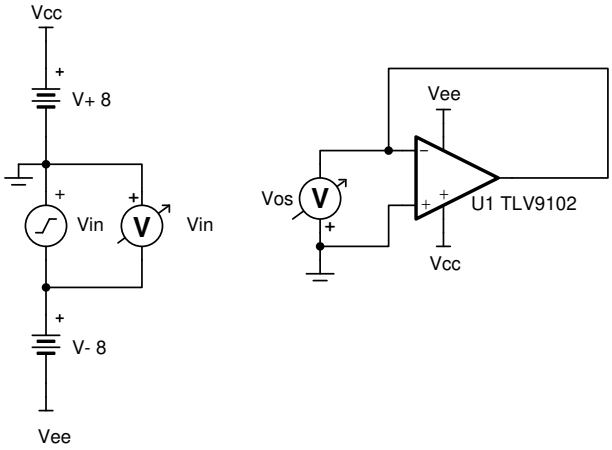

Figure 2-9. Power Supply Rejection Ratio (PSRR-) Test Circuit

Check the DC operating point to verify that the op amp is operating in the linear region. When modeled correctly, the pole and zero location should match the graphs in the data sheet. Parasitic and higher-order effects at higher frequencies are problematic and cause some deviation from data sheet curves and the measured simulation characteristics in that region. Figure 2-10 shows the simulated PSRR+ and PSRR- results for TLV9102. Figure 2-11 shows the data sheet plot for CMRR, PSRR+, and PSRR- for TLV9102. For a more complete simulation test analysis; please refer to the following EDN article, authored by Ian Williams. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ and PSpice® for TI.

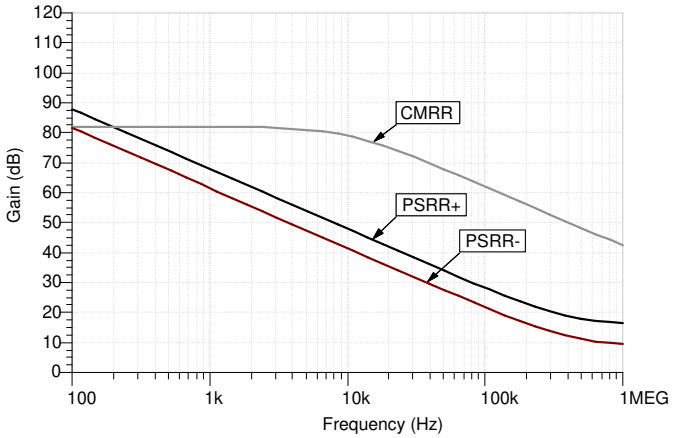

Figure 2-10. Simulated CMRR, PSRR+, PSRR- for TLV9102

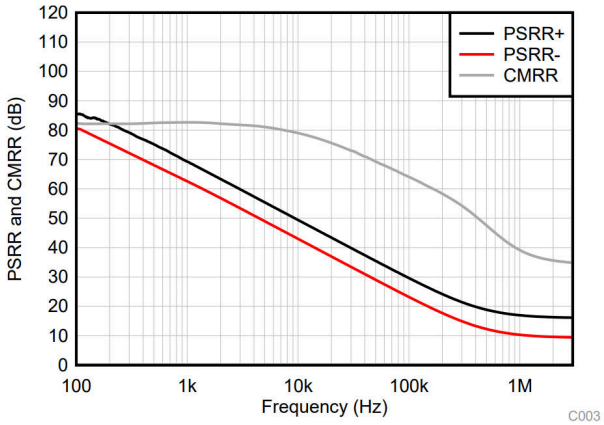

Figure 2-11. Data sheet Graph of CMRR, PSRR+, PSRR- for TLV9102

2.4 Open-Loop Output Impedance (Z_o)

Open-loop output impedance (Z_o) is a specification that is often omitted from the data sheets but is very important when performing a stability analysis. Zo forms a RC circuit in combination with a capacitive load and plays a key role in where the pole is created in the A_{OL} curve.

When modeled correctly, the Z_o helps in getting a more accurate settling time behavior under various capacitive loads. Z_o is also needed to calculate the proper component values when a compensation scheme is considered to assure the phase margin stays above 45 degrees. To learn more about Z_o, please refer to Texas Instruments Precision Lab video series on Stability.

Figure 2-12 below shows the "Open Loop Output Impedance (Z_o) Test Circuit." Z_o is output impedance looking from the output of the op amp.

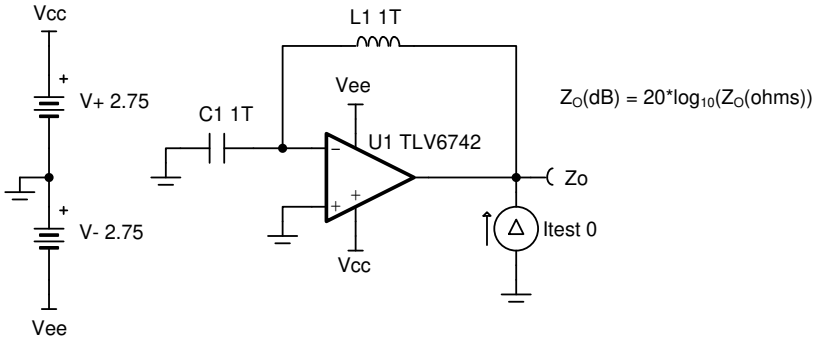

Figure 2-12. Open Loop Output Impedance (Z_o) Test Circuit

Simulated open-loop output impedance (Z_o) is usually in decibels (dB). But, oftentimes data sheets represent this parameter in ohms (Ω) as shown in Figure 2-14. Figure 2-13 shows the simulation Z_o for TLV6742 in ohms and Figure 2-14 shows the data sheet Z_o plot for TLV6742. For a more complete simulation test analysis, please refer to the following EDN article, authored by Ian Williams. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

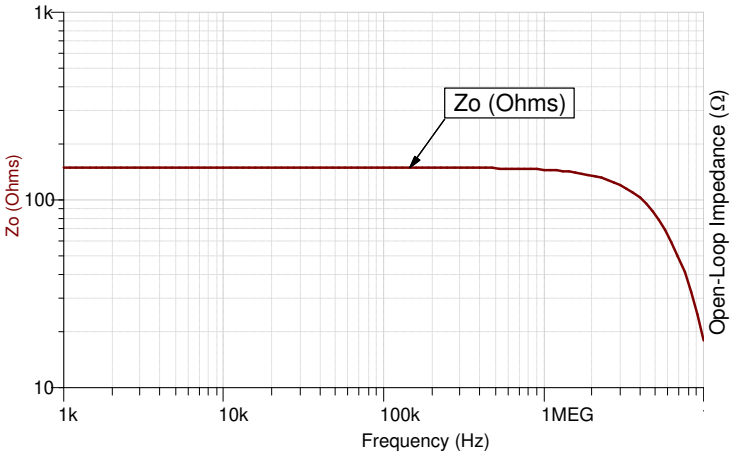

Figure 2-13. Simulated Z_o in ohms (Ω) for TLV6742

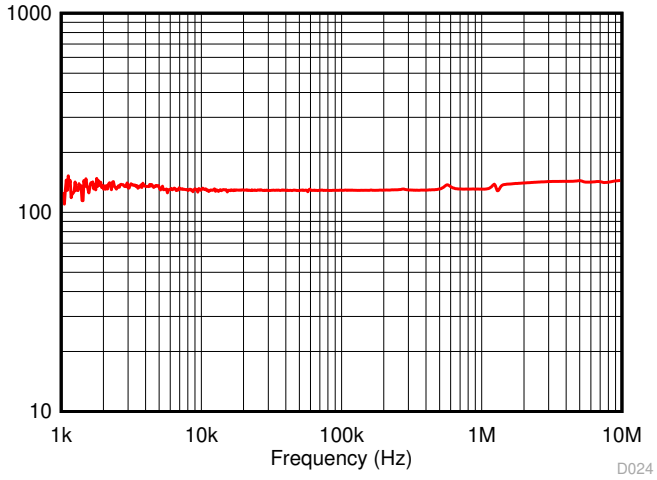

Figure 2-14. Data Sheet Graph of Z_o in ohms (Ω) for TLV6742

2.5 Voltage Noise (e_n)

Noise is simply an unwanted signal, usually random in nature, that when combined with the desired signal results in error. There are two parts to a voltage noise density curve, the 1/f noise (flicker noise, pink noise, low frequency noise, or excess noise) and the broadband noise (white noise, Johnson noise, thermal noise, or resistor noise). The 1/f noise happens at very low frequencies whereas the broadband noise is across all frequencies. Having a lower 1/f noise is desirable, since 1/f noise can become very large at lower frequencies.

The op amp's voltage noise is usually given in units of nanovolts per square root hertz (nV/√Hz). The reason for such a complex unit is because the noise of a circuit is dependent on its bandwidth. Noise calculations involve integrating the behavior of noise sources over a specific frequency range, and the unit of nanovolts per root hertz simplifies to the RMS voltage after calculating the square root of the integral. Figure 2-15 below shows the *Voltage Noise Test Circuit*. To learn more about voltage noise (e_n), please refer to Texas Instruments Precision Labs video series on noise.

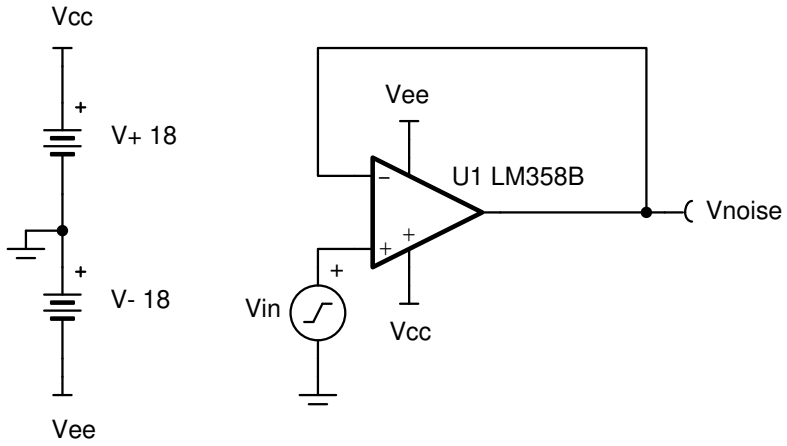

Figure 2-15. Voltage Noise (e_n) Test Circuit

This circuit places the op amp in a unity gain buffer configuration, with the input voltage source connected to the non-inverting input. This test setup generates a buffered copy of the input voltage noise at the op amp's output terminal for easy measurement. It's good practice to verify that the op amp is operating in the linear region by running a DC operating point test. Make sure to match the specified data sheet conditions for the power supply voltage, input common-mode voltage and load resistance (R_L) if any. To measure e_n, run a noise analysis over the desired frequency range and plot the results at the output node with respect to the input source. Figure 2-16 shows the simulated voltage noise results for LM358B and is confirmed by Figure 2-17 that shows the data sheet graph of voltage noise for LM358B. For a more complete simulation test analysis, please refer to the following EDN article, authored by Ian Williams. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

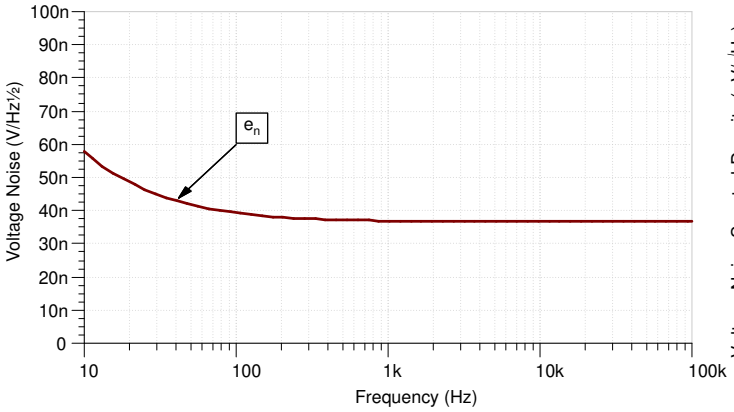

Figure 2-16. Simulated Voltage Noise (e_n) for LM358B

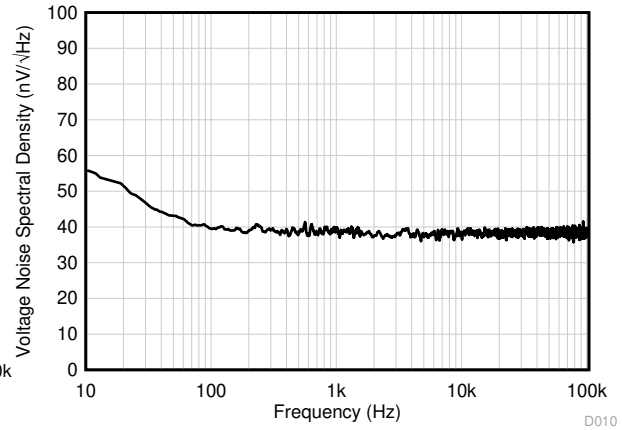

Figure 2-17. Data sheet Graph of Voltage Noise (e_n) for LM358B

2.6 Current Noise (i_n)

The second type of op amp noise is input current noise spectral density (i_n). Current noise is an input referred noise that gets converted to voltage by the input and feedback resistance of the circuit in accordance with Ohm's law. For large resistances, like ultra-low power devices, the contribution of current noise is significant. The op amp's current noise is usually given in units of femtoamps per square root hertz (fA/√Hz) or picoamps per square root hertz (pA/√Hz). Current noise is either characterized as a single value in the op amp's electrical characteristics table or as a curve over frequency. Similar to voltage noise, current noise over frequency may have both 1/f and broadband regions. To learn more about current noise (i_{in}) please refer to the Texas Instruments Precision Labs video series on noise.

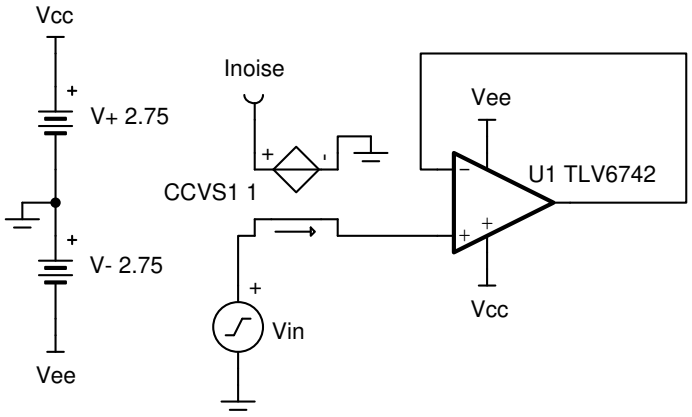

Figure 2-18. Current Noise (i_n) Test Circuit

The test circuit for current noise is very similar to the test circuit for voltage noise. This circuit adds in a current controlled voltage source (CCVS1) to convert current to voltage with a transresistance of 1V/A. The CCVS is added as a workaround for simulators that have difficulty measuring current noise directly, and will work in most tools. It's a good practice to verify that the op amp is operating in its linear region by first running a DC operating point test. Make sure to match the specified data sheet conditions for the power supply voltage, input common-mode voltage and load resistance (R_L) if any. To measure i_n, run a noise analysis over the desired frequency range and plot the results at node "Inoise" with respect to input source (V_{in}). Keep in mind that the simulator will report the result in volts instead of amps. Figure 2-19 shows the simulated current noise (i_N) for TLV6742, and is confirmed by the data sheet specification shown in Figure 2-20. As you can see, the current noise is dominated by the broadband region. The simulated results for TLV6742 match well with the data sheet value of (23fA/ √Hz). For a more complete simulation test analysis, please refer to the following EDN article, authored by Ian Williams. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

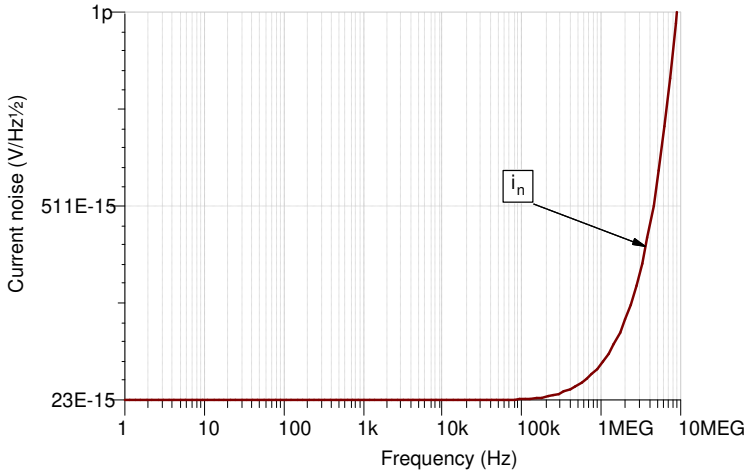

Figure 2-19. Simulated Current Noise (i_n) for TLV6742

i_N	Input current noise	f = 1 kHz		23	fA/√Hz

Figure 2-20. Data Sheet Specification of Current Noise (i_n) for TLV6742

2.7 Input Offset Voltage (V_{OS}), Input Bias Current (I_b), and Quiescent Current (I_Q)

Offset Voltage (V_{OS}) is the differential voltage that would have to be applied at the input to force the op amp's output to 0V; V_{OS} happens due to the mismatch of input transistors. Typically, general-purpose op amps have offset voltages ranging from mV down to µV. Changing power-supply voltage or common mode voltage will affect input offset voltage of an op amp.

Input bias current (I_b) is the average of bias current at the inverting and non-inverting input of the op amp. These currents can be modeled as a current source connected to each input. Ideally, the two input bias currents would be equal to each other and would cancel out. In reality they are not equal, and the difference of these currents is defined as input offset current (I_{OS}). If I_{OS} is low, it is possible to match the impedances connected to each input and cancel the offset developed from I_b. To learn more about V_{OS} and I_b, please refer to the Texas Instruments Precision Labs video series on V_{OS} and I_b.

Quiescent current (I_Q) is the current level in an op amp when it is producing zero output. I_Q is also known as the idle state current. Power dissipated due to I_Q is simply equal to the total supply voltage multiplied by I_Q. I_Q is listed in the electrical characteristics table of the data sheet. To learn more about I_Q, please refer to Texas Instruments Precision Labs video series on slew rate.

$$P = I_Q \times V_S \tag{7}$$

For many general-purpose applications, V_{OS} and I_b are amongst the first parameters that are considered when selecting an op amp, whereas for some low-power applications I_Q is one of the most important parameters. V_{OS} can be modeled as a DC error voltage in series with the op amp's non-inverting input. Vos does not change with frequency but drifts over temperature. I_b and I_Q can be modeled as a DC current source flowing from each op amp's input pin to ground. Like V_{OS}, these do not change significantly over frequency but exhibit temperature drift. It is important to keep in mind that models are typically made with 25C conditions. Be cautious when using large input or feedback resistors because the resulting voltage drop across those resistors may cause DC errors. Figure 2-21 shows the Electrical Characteristics table from the data sheet giving both typical and maximum values for OPA2991. Op amp SPICE models are commonly designed to show typical behavior, *not maximum*, but check with the manufacturer if there's any confusion about a particular model. Figure 2-22 shows the recommended test circuit.

OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = V–		±125	±750	µV
			T_A = –40°C to 125°C		±780	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C	±0.3		µV/°C
INPUT BIAS CURRENT						
I_B	Input bias current			±10		pA
I_{OS}	Input offset current			±10		pA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_{CM} = V–, I_O = 0 A		560	685	µA
			T_A = –40°C to 125°C		750	

Figure 2-21. Data Sheet Specification of V_{os}, I_b, I_Q for OPA2991

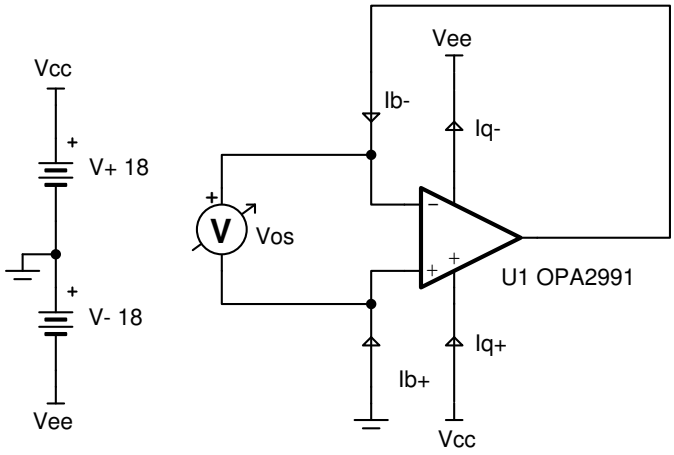

Figure 2-22. V_{os}, I_b, I_Q Test Circuit

This circuit is a voltage-follower with the non-inverting input of the op amp grounded. Current meters are placed at both op amp inputs in order to measure I_{b+} and I_{b-}, and the differential voltmeter to measure the V_{OS} across the inputs of the op amp pins. Ensure that the power supply voltage and input common-mode voltage match the test conditions given in the op amp's data sheet. Figure 2-23 shows the simulated results for OPA2991. Comparing the measured results to Figure 2-21, we can see that the simulated results match well with the data sheet for OPA2991. For a more complete simulation test analysis, please refer to the following EDN article, authored by Ian Williams. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

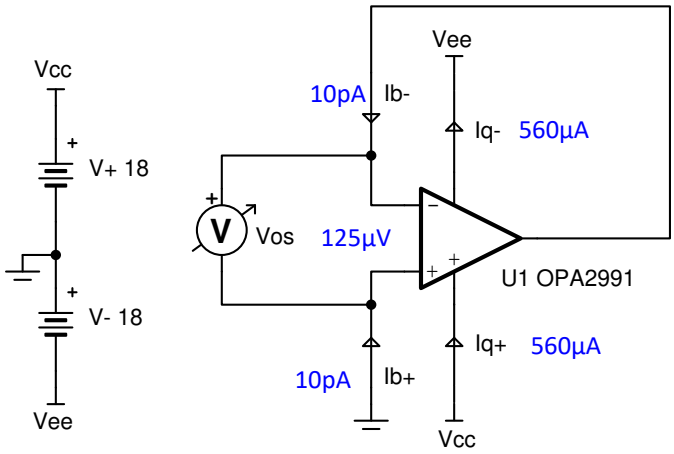

Figure 2-23. Simulate V_{OS}, I_b, and I_Q for OPA2991

2.8 Output Voltage Versus Output Current (Claw Curve)

Output voltage (V_{out}) versus output current (I_{out}) is usually referred to as the claw curve because they are shaped like an animal claw. Claw curves show the slam limit, or saturated output limit, with respect to output current and temperature. This is particularly important in rail to rail output amplifier models as it can help circuit designers to choose the appropriate op amp especially when driving heavy loads or when dynamic range is a concern. Figure 2-24 shows the data sheet claw curve for TLV9002. Claw curves are composed of two parts, the positive side (claw+) and the negative side (claw-). This value can be given in a data sheet as either absolute or relative. Absolute is when V_{out} is a specific power-supply voltage, whereas relative is when V_{out} is a generic power-supply voltage. To learn more about claw curves, please refer to the Texas Instruments Precision Labs video series on input and output limitations.

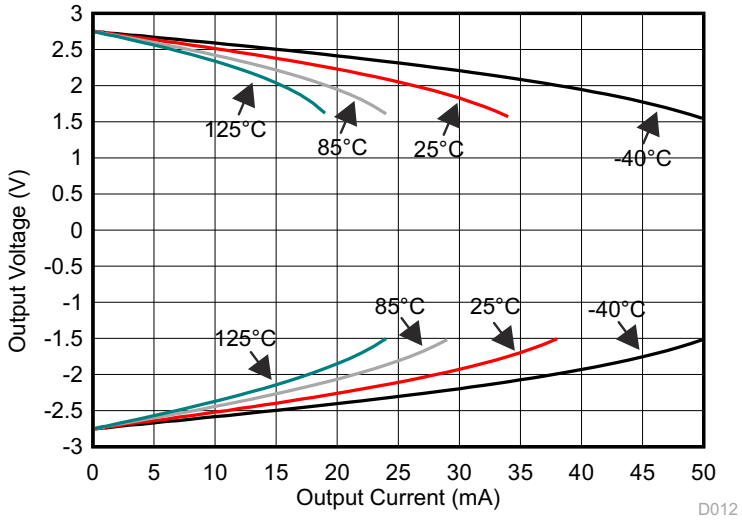

Figure 2-24. Data sheet Graph Claw Curve for TLV9002

Op amp models are designed to replicate the claw curve behavior at room temperature or 25°C. Figure 2-25 and Figure 2-27 show the recommended test circuit to simulate sourcing (claw+) and sinking (claw-) curves. The test circuit is a simple inverting buffer circuit with the non-inverting input pin grounded and the output connected to a current generator. Adjust the V_{cc} and V_{ee} to match the recommended supply voltage from the data sheet. For claw+ make sure to set V_{in} equal to V_{ee} so that the op amp sources current. Similarly for claw- make sure to set V_{in} equal to V_{cc} so that the op amp sinks current. Figure 2-26 and Figure 2-28 show the simulated claw curve for TLV9002. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

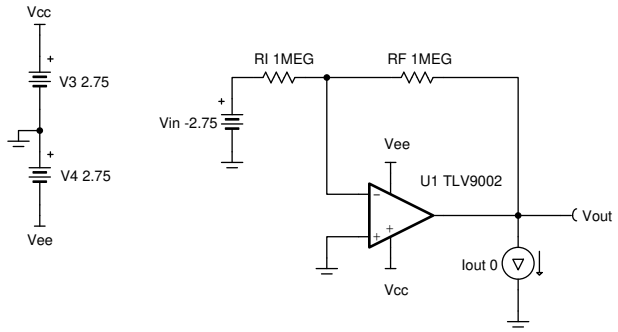

Figure 2-25. Claw+ Test Circuit

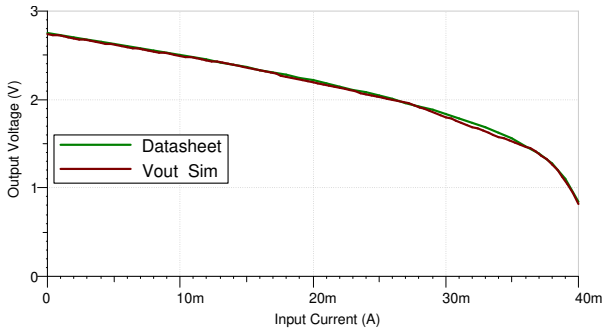

Figure 2-26. Simulated Claw+ Curve (Sourcing) for TLV9002

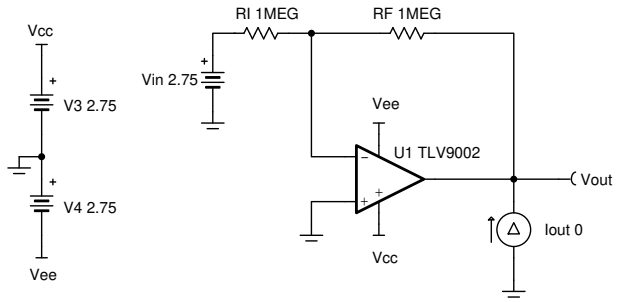

Figure 2-27. Claw- Test Circuit

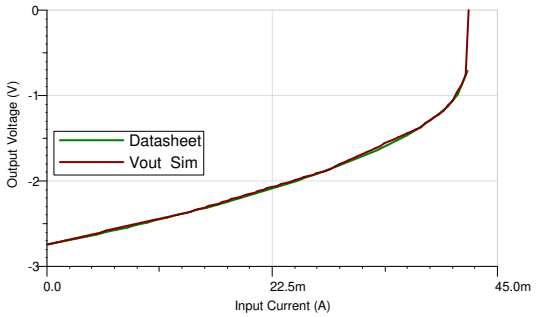

Figure 2-28. Simulated Claw- Curve (Sinking) for TLV9002

2.9 Overload Recovery Time (t_{OR})

Driving the output beyond its linear range is called overloading the output. When the overload condition is corrected, there is a time delay before the overloaded output can recover. Overload recovery time (t_{OR}) is the time required for the op amp to recover or catch-up to its rated output voltage from a saturated condition. This condition occurs when the amplifier is driven beyond its output swing limits causing the output to saturate. In other words t_{OR} is the time required for all the internal transistors in the output stage to transition from an abnormal stage, whether saturated or cutoff, to a normal state. In some amplifiers, t_{OR} increases for large input impedances. Usually, data sheet specification applies for low impedances and assumes that t_{OR} is not degraded by stray capacitance. It is important to not exceed the absolute max limits when over-driving the device. To learn more about overload recovery time, please refer to the Texas Instruments Precision Labs video series on slew rate.

In addition to the input impedance, the t_{OR} is also dependent on how strong the op amp is overdriven; the delay is much smaller when the op amp is barely overdriven as compared to significantly overdriven. There is overload recovery positive (t_{OR+}) and overload recovery negative (t_{OR-}), where t_{OR+} is referred to the positive supply and t_{OR-} is referred to the negative supply. Figure 2-29 shows the data sheet overload recovery time for OPA191. Some data sheets only have one value for t_{OR}, meaning it's the same delay for both positive and negative supply. Figure 2-30 and Figure 2-32 show the recommended circuit to simulate the positive and negative t_{OR} respectively.

t_{OR}	Overload recovery time	$V_{IN} \times G = V_S$	From overload to negative rail	0.4	µs
			From overload to positive rail	1	

Figure 2-29. Data Sheet Specification of tOR for OPA191

Figure 2-31 and Figure 2-33 show the simulated t_{OR+} and t_{OR-} for OPA191. The simulated results below match well with the data sheet values, where t_{OR+} is equal to 0.4µs. The test circuit is a simple inverting amplifier with a gain of 10V/V. The input to this circuit is a piecewise function. Initially, the circuit outputs 18 V due to a DC level of -2V, after 5µs the output tries to catch up to the input. Notice here that the expected output is 20 V (DC level * Gain) but the output is limited to 18 V due to an output swing limitation, which is related to the supply rail. The time delay before the output reacts to the change in input is the $t_{OR,}$. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

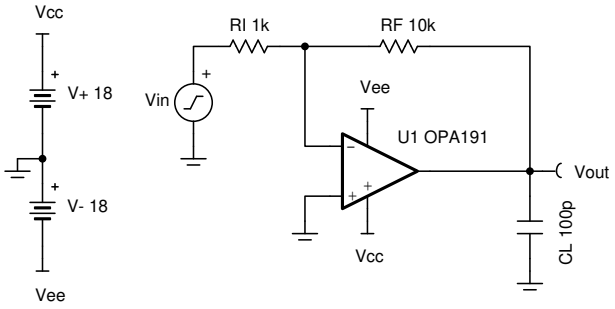

Figure 2-30. Overload (Positive) Recovery Time Test Circuit

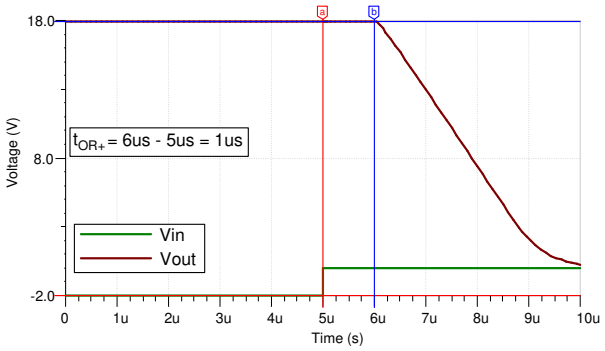

Figure 2-31. Simulated Overload (Positive) Recovery Time for OPA191

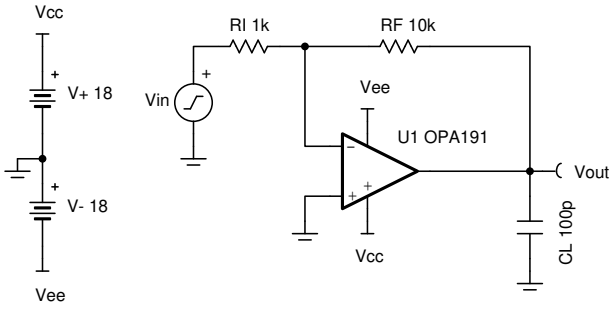

Figure 2-32. Overload (Negative) Recovery Time Test Circuit

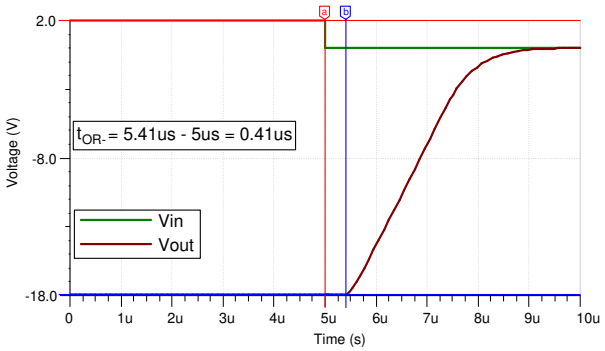

Figure 2-33. Simulated Overload (Negative) Recovery Time for OPA191

2.10 Common-mode Input Capacitance (C_{CM}) and Common-mode Differential Capacitance (C_{DIFF})

There are two types of input capacitances, namely: a differential (C_{DIFF}) and common-mode (C_{CM}) . C_{DIFF}, is the input capacitance between the non-inverting and inverting pins of an op amp. C_{CM}, is the parasitic capacitance between each input pins and ground. Figure 2-34 shows a visual representation of C_{DIFF} and C_{CM} for OPA2375. Input capacitance can be found in the electrical characteristics table of the data sheet as shown in Figure 2-35.

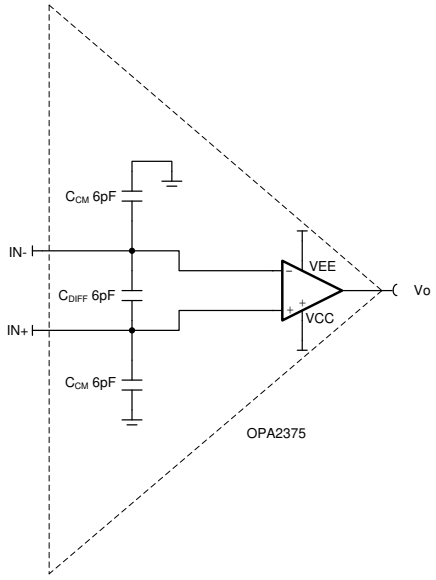

Figure 2-34. Input Capacitance Illustration for OPA2375

INPUT CAPACITANCE					
Z_{ID}	Differential			10 || 6	MΩ || pF
Z_{ICM}	Common-mode			10 || 6	GΩ || pF

Figure 2-35. Data Sheet Specifications of Input Capacitance Values for OPA2375

Op amps with low input capacitance are useful in applications such as: smoke detectors and photodiode transimpedance amplifier circuits. Input capacitance at the inverting input can affect the stability of an op amp circuit causing phase shift or delay. The feedback network can interact with the input capacitance to create unwanted pole causing stability issues if the impedance values are not carefully selected. Op amps similar to OPA2375

with low input capacitance can help increase the frequency of pole in the feedback path far enough that it has negligible effect on the circuit. To ensure stability, it is important to make sure the pole created due to the interaction between input capacitance and the feedback impedance is at least 2 to 10 times larger in frequency as compared to the bandwidth of the circuit.

Figure 2-36 and Figure 2-38 show the circuits to simulate C_{CM} and C_{DIFF}. Ensure that the power supply voltage and other test conditions match closely with the op amp's datasheet. In the C_{CM} test circuit, the op amp is configured as a buffer circuit with a 100kΩ in series with the non-inverting input of the op amp. Using the -3dB frequency of the bode plot at the non-inverting input of the op amp, C_{CM} can be simulated and calculated as shown in Figure 2-37. Similarily Figure 2-39 shows the simulated C_{DIFF} for OPA2375 and corresponding calculation. For more information on common-mode and differential input capacitances, please refer to "The Signal" authored by Bruce Trump. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

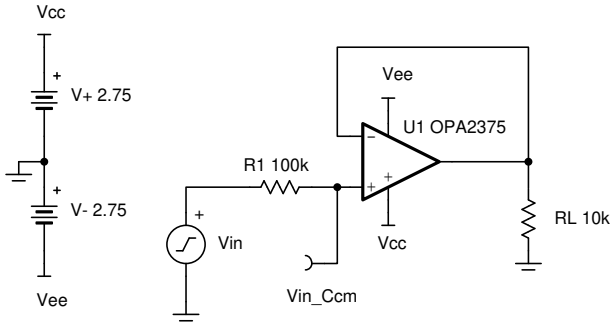

Figure 2-36. Common-Mode Input Capacitance (C_{CM}) Test Circuit

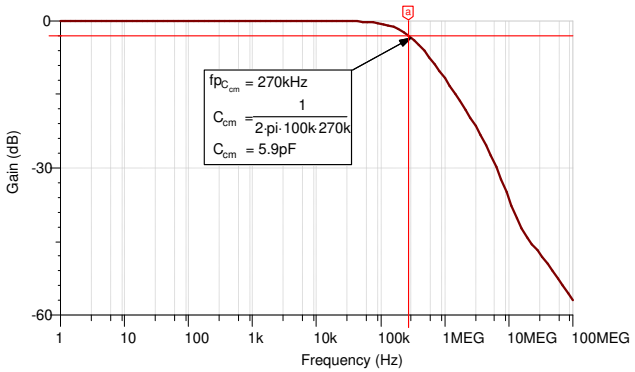

Figure 2-37. Simulated Common-Mode Input Capacitance (C_{CM}) for OPA2375

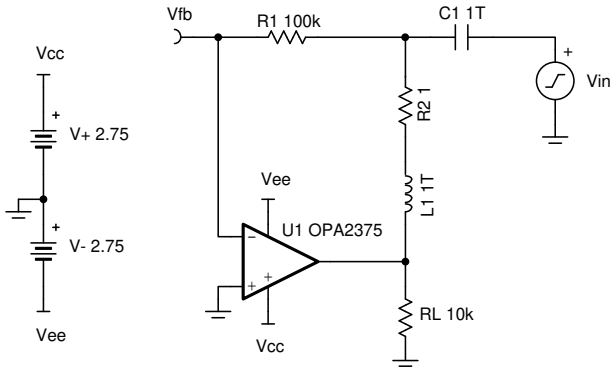

Figure 2-38. Differential Input Capacitance (C_{DIFF}) Test Circuit

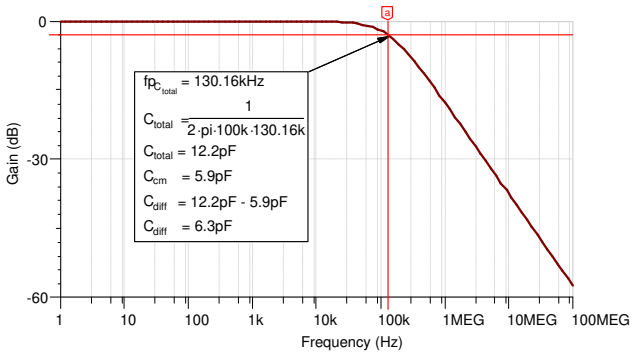

Figure 2-39. Simulated Differential Input Capacitance (C_{DIFF}) for OPA2375

2.11 Overshoot and Transient Response

Transient response is an amplifiers response to a pulse input, and consists of large signal and small signal transient responses. Overshoot is important because it indicates how much ringing an amplifier has in the presence of a capacitive load. Overshoot is a measure of stability in time domain; it is the equivalent of what "peaking" is in the frequency domain. Some macro models use extra passive components to mimic the overshoot accurately but generally, if the phase margin is accurate, the overshoot should be accurate as well. Usually datasheets indicate whether a load capacitor was used when measuring the transient response, if so use the same capacitance value indicated in the data sheet. Figure 2-40 shows the test circuit for transient response (both small and large signal). This test circuit is simply a non-inverting amplifier with a gain of 1 V/V. The convention for small signal or large signal is dependent on the op amp and the process technology used. Typically, input signals less than 100 mV is considered small signal and input signal equal or greater than 1V is considered as a large signal. Figure 2-41 and Figure 2-42 show the small signal and large signal transient responses, respectively, for TLV9062.

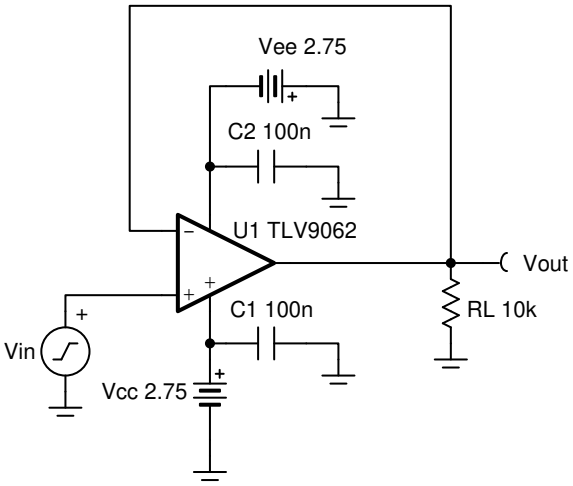

Figure 2-40. Transient Test Circuit

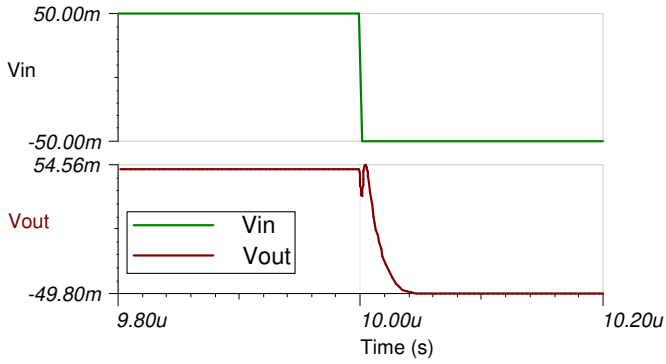

Figure 2-41. Small-Signal Transient Response for TLV9062

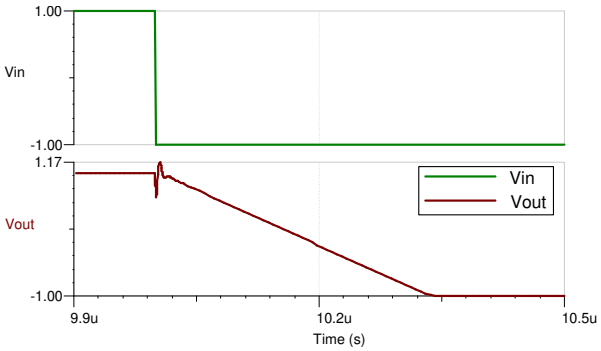

Figure 2-42. Large-Signal Transient Response for TLV9062

As you can see, the percent overshoot is much larger for small-signal as compared to large signal. Figure 2-43 shows the test circuit for overshoot and Figure 2-44 shows the corresponding simulation output of overshoot, which is confirmed in Figure 2-45. It's a simple inverting amplifier with a gain of 1V/V, with a resistive load of 10kΩ and capacitive load 100pF at the output. Capacitive loads at the output lowers the stability of an op amp circuit resulting in more overshoot as compared to a no-load circuit. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

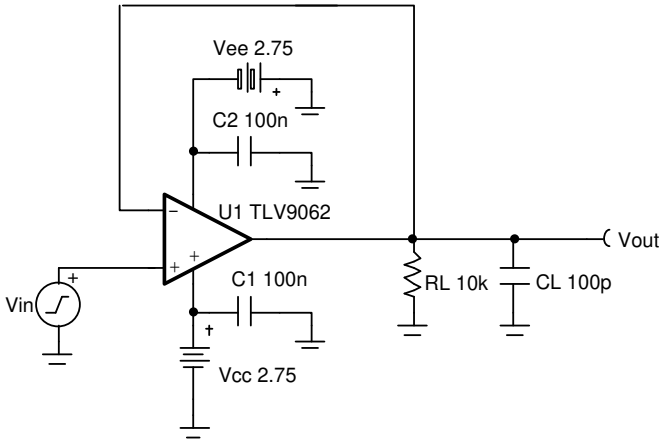

Figure 2-43. Overshoot Test Circuit

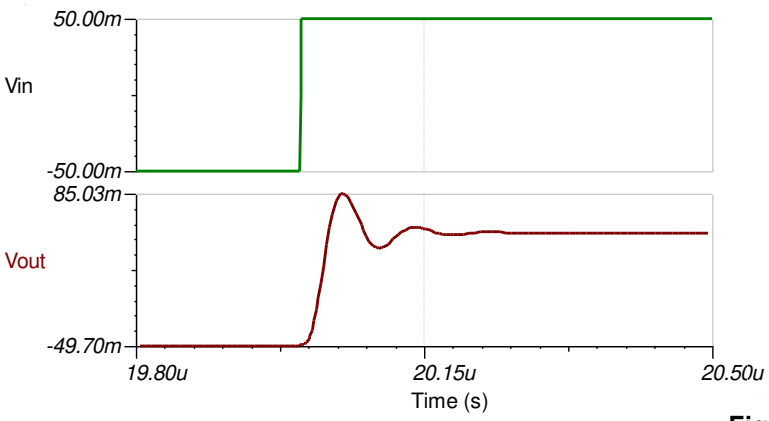

Figure 2-44. Simulated Overshoot Response for TLV9062

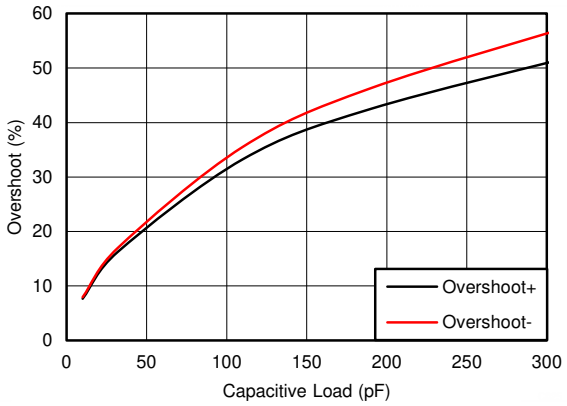

Figure 2-45. Data Sheet Specification of Overshoot for TLV9062

2.12 Common-Mode Voltage Range (CMVR)

The common-mode voltage range (CMVR) parameter is important as it allows the user to see the head room or how far away the input common-mode needs to be from the supply. Figure 2-46 shows the *CMVR Test Circuit* and Figure 2-47 shows the corresponding simulation output. To learn more about CMVR, please refer to the Texas Instruments Precision Labs video series on input and output limitations. This circuit may be simulated by downloading the AN1516 Test Circuits in either TINA-TI™ or PSpice® for TI.

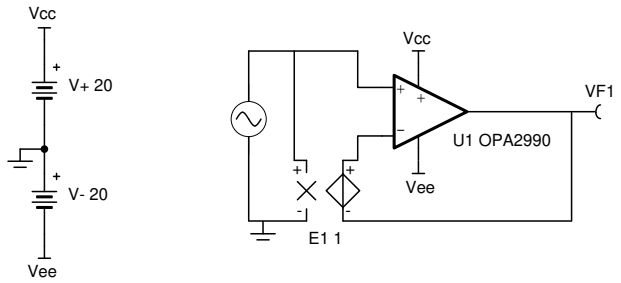

Figure 2-46. CMVR Test Circuit

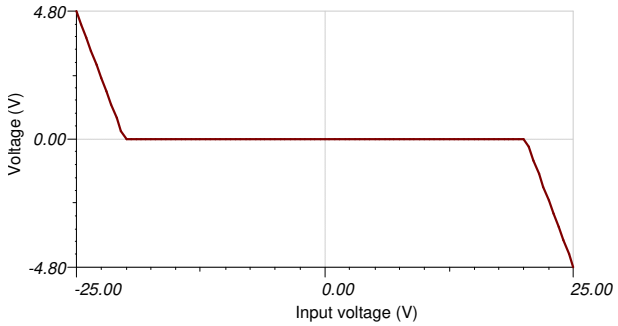

Figure 2-47. Simulated CMVR for OPA2375

INPUT VOLTAGE RANGE					
V_{CM}	Common-mode voltage range		(V–) – 0.2	(V+) + 0.2	V

Figure 2-48. Data Sheet Specification of CMVR for OPA2375

3 Conclusion

The test circuits described above are not meant to replace the evaluation of the device on the bench. Rather, they provide the user with the flexibility of making quick assessments with respect to the accuracy of the macro model.

Special thanks to the applications group and the design community at Texas Instruments for their thoughtful insights.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2020) to Revision F (September 2020)	Page
• Throughout this document, paragraphs were edited for conciseness, part numbers updated to reflect current portfolio, and simulation outputs added to confirm data sheet results and also to show examples for simulation circuits	3

Changes from Revision D (November 2006) to Revision E (May 2020)	Page
• Changed *Voltage Noise (e_n) Test Circuit* image	8

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