User's Guide
SNVA049A–June 2004–Revised April 2013

AN–1220 LM2645 Demo Board Design

1 Introduction

The LM2645 demo board was designed to provide the flexibility that allows many different circuit configuration for the two switching channels such as fixed or adjustable output voltage, with or without current sense resistor, 200kHz or 300kHz operation, and internal or external LDO supply. The LM2645 board layout is optimized based on a design with no current sense resistor – a common approach in the design of system power supplies in notebook computers. This documents provides detailed information of the LM2645 demo board with current sensing across the Rds of the upper MOSFET.

The demo board provides four DC outputs: V_{OUT1}= +5V with 3A max, V_{OUT2} = +3.3V with 3A max, L_{DOUT} = +12V with 0.1A max, and V_{LIN3} = +3.3V with 0.05A max. The input voltage range is 9V to 20V (measured at the input terminal of the demo board).

To improve the transient load response of the switching output, high value SPCAP are chosen as the output capacitors for V_{OUT1} and V_{OUT2}.

Although a 1µF capacitor is sufficient to ensure stable operation of the internal regulator OUT3, a 10µF ceramic capacitor is installed on board to eliminate the output voltage dip near the end of the +5V output soft-start. The voltage dip is due to the supply voltage of VLIN5 rail is switching over from the internal regulator to the EXT pin when the +5V rail reaches the 4.7V threshold. An inexpensive electrolytic capacitor will also work well.

Figure 1 shows the position of jumper wires for configuring the current sensing scheme of the two switching channels. Figure 2 shows the full schematic of the LM2645 demo board reference circuit. Table 1 shows how to set circuit functions using the 4 jumpers. Table 2 lists the bill of materials of the reference circuit. Figure 9 and Figure 10 show the trace layout of the board.

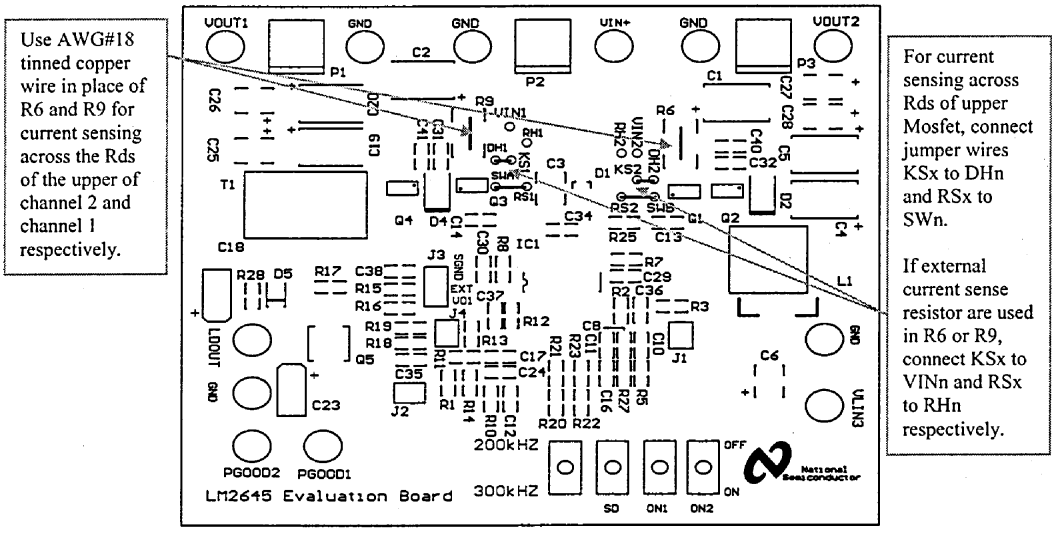

Figure 1. Jumper Wire Positions for Different Current Sensing

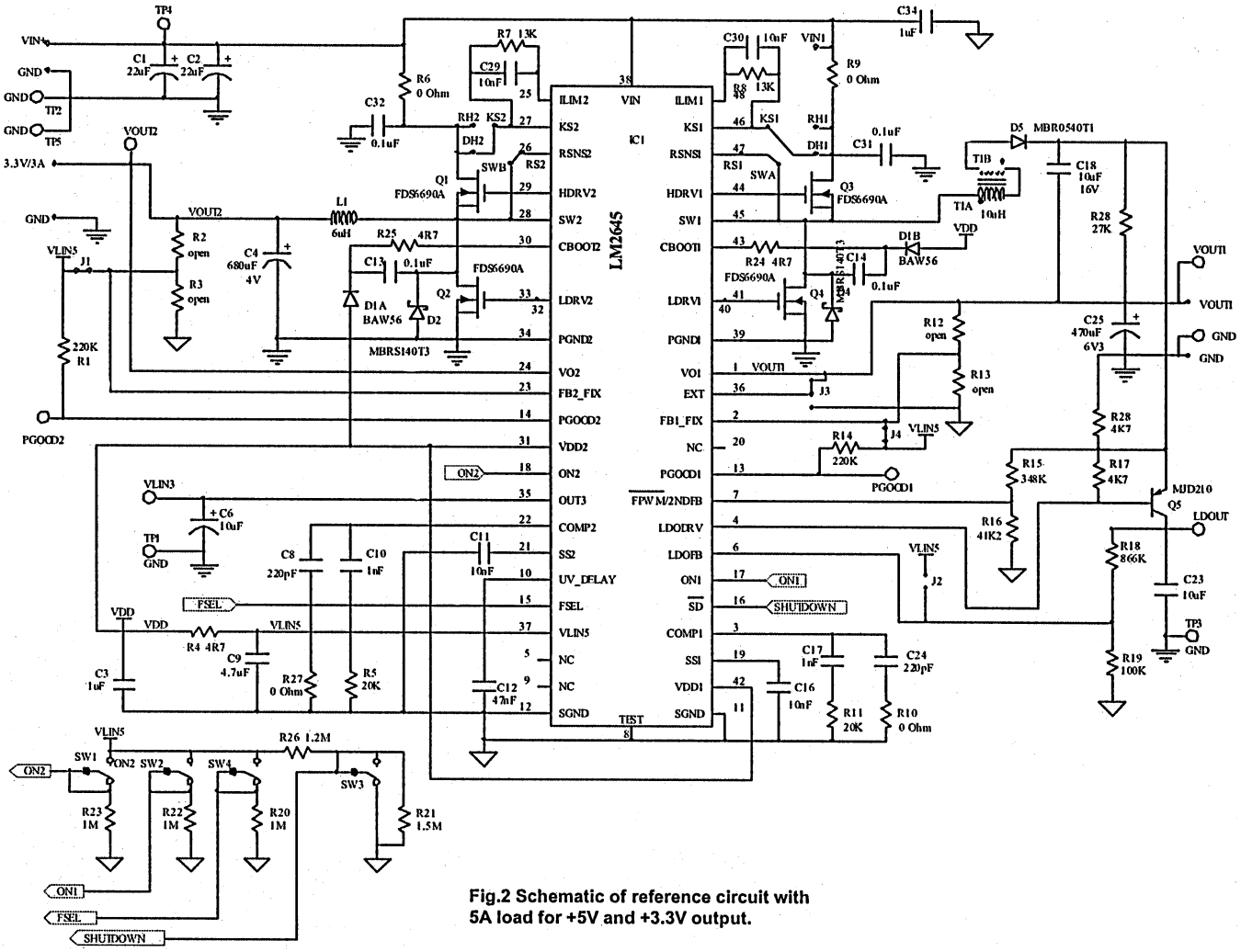

Fig.2 Schematic of reference circuit with 5A load for +5V and +3.3V output.

Figure 2. Schematic

Table 1. Jumper Selection for Circuit Function

Jumper	Connection	Function
J1	Short	Channel 2 fixed 3.3V output
	Open	Channel 2 adjustable output
J2	Short	LDODRV output disable
	Open	LDODRV output enable
J3	Connects to VO1	VLIN5 supplied from VOUT1 via the EXT pin
	Connects to Ground	Internal LDO is enabled to supply VLIN5
J4	Short	Channel 1 fixed 5V output
	Open	Channel 1 adjustable output

2 Component Selection

The LM2645 demo board has been designed for use in a wide range of applications, and can accommodate various load and output voltage requirements. To avoid improper device or circuit operation, please refer to the *LM2645 Advanced Two-Phase Switching Controller With Two Linear Outputs* (SNVS155) data sheet for operational information before modifying the reference design.

Table 2. Bill of Materials

Code	Description	Manufacturer
C1	Cap-Tantalum 22µF 35V 239D226X0035E2T	Vishay
C10	CAP-MLCC 1nF 25V VJ0805Y102KXX	Vishay
C11	CAP-MLCC 10nF 25V VJ0805Y103KXX	Vishay
C12	CAP-MLCC 47nF 25V VJ0805Y473KXX	Vishay
C13	CAP-MLCC 0.1µF 25V VJ0805Y104KXX	Vishay
C14	CAP-MLCC 0.1µF 25V VJ0805Y104KXX	Vishay
C16	CAP-MLCC 10nF 25V VJ0805Y103KXX	Vishay
C17	CAP-MLCC 1nF 25V VJ0805Y102KXX	Vishay
C18	CAP-MLCC 10µF 16V TMK325F106ZH	Taiyo Yuden
C2	Cap-Tantalum 22µF 35V 239D226X0035E2T	Vishay
C23	Cap-Tantalum 10µF 20V 293D106X9020C2	Vishay
C24	CAP-MLCC 220pF 25V VJ0805Y221KXX	Vishay
C25	POS-CAP 470µF 6.3V 6TPE470MI	Sanyo
C29	CAP-MLCC 10nF 25V VJ0805Y103KXX	Vishay
C3	CAP-MLCC 1µF 10V lMK212F105MG	Taiyo Yuden
C30	CAP-MLCC 10nF 25V VJ0805Y103KXX	Vishay
C31	CAP-MLCC 0.1µF 25V VJ0805Y104KXX	Vishay
C32	CAP-MLCC 0.1µF 25V VJ0805Y104KXX	Vishay
C34	CAP-MLCC 1µF 50V UMK212F105MG	Taiyo Yuden
C4	POS-CAP 680uF 4V 4TPE680MF	Sanyo
C6	CAP-MLCC 1µF 10V LMK212F105MG	Taiyo Yuden
C7	CAP-MLCC 0.1µF 25V VJ0805Y104KXX	Vishay
C24	CAP-MLCC 220pF 25V VJ0805Y221KXX	Vishay
C9	CAP-MLCC 4.7µF 10V LMK316BJ475ML	Taiyo Yuden
D1	Switching Diode-Dual 200mA 70V BAW56	Fairchild
D2	Schottky Diode 1A 40V MBRS140T3	ON Semiconductor
D4	Schottky Diode 1A 40V MBRS140T3	ON Semiconductor
D5	Schottky Diode 0.5A 40V MBR0540T1	ON Semiconductor
IC1	PWM CONTROLLER LM2645	Texas Instruments
L1	INDUCTOR 6µH CEP125-6R0MC	Sumida
Q1	N-MOSFET FDS6690A	Fairchild
Q2	N-MOSFET FDS6690A	Fairchild
Q3	N-MOSFET FDS6690A	Fairchild
Q4	N-MOSFET FDS6690A	Fairchild
Q5	PNP TRANSISTOR 5A MJD210	ON Semiconductor
R1	RESISTOR-Chip 0805 220K CRCW08052203J	Vishay
R27	RESISTOR-Chip 0805 0 Ohm CRCW08051002J	Vishay
R11	RESISTOR-Chip 0805 20K CRCW08051002J	Vishay
R12	RESISTOR-Chip 0805 60K4 CRCW08056042F	Vishay
R13	RESISTOR-Chip 0805 20K CRCW08052002F	Vishay
R14	RESISTOR-Chip 0805 220K CRCW08052203J	Vishay
R15	RESISTOR-Chip 0805 348K CRCW08053483F	Vishay
R16	RESISTOR-Chip 0805 41K2 CRCW08054122F	Vishay
R17	RESISTOR-Chip 0805 4K7 CRCW08054701J	Vishay
R18	RESISTOR-Chip 0805 866K CRCW08058663F	Vishay
Code	Description	Manufacturer
R19	RESISTOR-Chip 0805 100K CRCW08051003F	Vishay
R2	RESISTOR-Chip 0805 33K2 CRCW08053322F	Vishay

Table 2. Bill of Materials (continued)

Code	Description	Manufacturer
R20	RESISTOR-Chip 0805 1M CRCW08051004J	Vishay
R21	RESISTOR-Chip 0805 1M5 CRCW08051504J	Vishay
R22	RESISTOR-Chip 0805 1M CRCW08051004J	Vishay
R23	RESISTOR-Chip 0805 1M CRCW08051004J	Vishay
R24	RESISTOR-Chip 0805 4R7 CRCW08054R7J	Vishay
R25	RESISTOR-Chip 0805 4R7 CRCW08054R7J	Vishay
R26	RESISTOR-Chip 0805 1.2M CRCW08051204J	Vishay
R27	RESISTOR-Chip 0805 0 Ohm CRCW08051002J	Vishay
R28	RESISTOR-Chip 0805 27K CRCW08052702J	Vishay
R3	RESISTOR-Chip 0805 20K CRCW08052002F	Vishay
R4	RESISTOR-Chip 0805 4R7 CRCW08054R7J	Vishay
R5	RESISTOR-Chip 0805 20K CRCW08053301J	Vishay
R6	AWG#18 tinned copper wire	Vishay
R7	RESISTOR-Chip 0805 13K CRCW08051302F	Vishay
R8	RESISTOR-Chip 0805 13K CRCW08051302F	Vishay
R9	AWG#18 tinned copper wire	Vishay
T1	COUPLE INDUCTOR 10µH 4749-T047	Sumida

3 Output Voltage Setting

The output voltage for each channel is set by the ratio of a voltage divider (**R2, R3** and **R12, R13**) as shown in Figure 3. The resistor values can be determined by the following equation:

$$R_1 = \frac{R_2}{\left(\frac{V_{nom}}{V_{fb}} - 1\right)} \quad (1)$$

Where Vfb=1.238V. Although increasing the value of R1 and R2 will increase efficiency, this will also decrease accuracy. Therefore, a maximum value is recommended for R2 in order to keep the output within .3% of Vnom. This maximum R2 value should be calculated first with the following equation:

$$R_{2\ max} = \frac{.3\% \cdot V_{nom}}{200\ nA} \quad (2)$$

Where 200nA is the maximum current drawn by FBx pin.

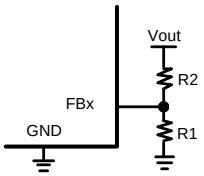

Figure 3. Output Voltage Setting

Example: Vnom=5V, Vfb=1.238V, Ifbmax=200nA.

$$R_{2\ max} = \frac{.003 \cdot 5V}{200\ nA} = 75\ k\Omega \quad (3)$$

Choose 60K

$$R_1 = \frac{60k}{\left(\frac{5V}{1.238V} - 1\right)} = 19.75\ k\Omega \cong 20\ k\Omega \quad (4)$$

4 Current Sensing and Limiting

Current sensing is accomplished either by sensing the Vds of the top FET or by sensing the voltage across a current sense resistor (**R6** and **R9**) connected from VIN to the drain of the top FET (See Figures 4 and 5). The advantage of sensing current across the top FET are reduced parts count, cost and power loss, whereas using a current sense resistor improves the current sense accuracy. Keeping the differential current-sense voltage below 200mV ensures linear operation of the current sense amplifier. Therefore, the Rdson of the top FET or the current sense resistor must be small enough so that the current sense voltage does not exceed 200mV when the top FET is on. There is a leading edge blanking circuit that forces the top FET on for at least 150ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. Additionally, a minimum voltage of at least 50mV across Rsns is recommended to ensure a high SNR at the current sense amplifier.

Assuming a maximum of 200mV across Rsns, the current sense resistor (or maximum $R_{DS(ON)}$)can be calculated as follows:

$$R_{sns\ max} = \frac{200\ mV}{I_{max} + \frac{1}{2} I_{rip}} \tag{5}$$

where Imax is the maximum expected load current, including overload multiplier (ie:120%), and Irip is the inductor ripple current (see Equation 14). The above equation gives the maximum allowable value for Rsns. Switching losses will increase with Rsns, thus lowering efficiency.

The peak current limit is set by an external resistor (**R7** and **R8**) connected between the ILIMx pin and the KSx pin. An internal 10µA current sink on the ILIMx pin produces a voltage across the resistor to set the current limit threshold which is compared to the current sense voltage. A 10nF capacitor across this resistor is required to filter unwanted noise that could improperly trip the current limit comparator.

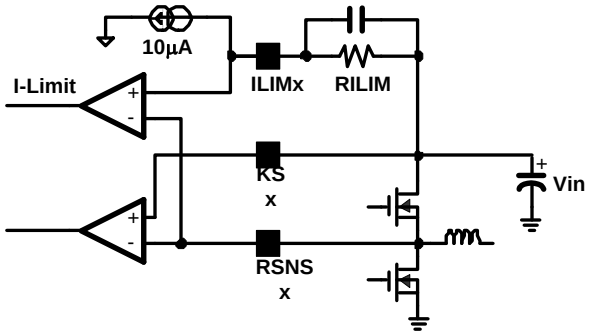

Figure 4. Current Sensing by Vds of the Top FET

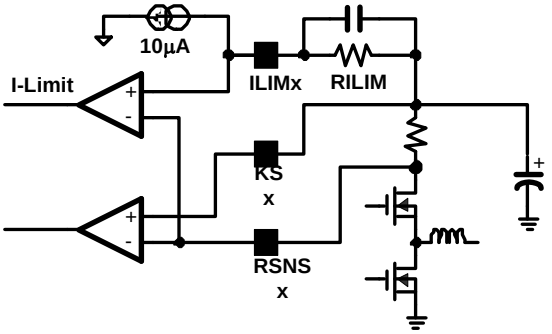

Figure 5. Current Sensing by External Sense Resistor

Current limit is activated when the inductor current is high enough to cause the voltage at the RSNSx pin to be lower than that of the ILIMx pin. This toggles the comparator, thus turning off the top FET immediately. The comparator is disabled either when the top FET is turned off or during the leading edge blanking time. The equation for current limit resistor, R_{lim}, is as follows:

$$R_{lim} = \frac{(I_{lim} + \frac{1}{2} I_{rip}) R_{sns}}{10\ \mu A} \quad (6)$$

Where Ilim is the load current at which the current limit comparator will be tripped.

When sensing current across the top FET, replace Rsns with the Rdson of the FET. This calculated Rlim value guarantees that the minimum current limit will not be less than Imax. It is recommended that a 1% tolerance resistor be used.

When sensing across the top FET, Rdson will show more variation than a current sense resistor, largely due to temperature. Rdson will increase proportional to temperature according to a specific temperature coefficient. Refer to the manufacturer's data sheet to determine the range of Rdson values over operating temperature or see the *MOSFET SELECTION* section for a calculation of maximum Rdson. This will prevent Rdson variations from prematurely setting off the current limit comparator as the operating temperature increases.

5 Output Capacitor Selection (C4, and C19)

In applications that exhibit large and fast load current swings, the slew rate of such a load current transient may be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple will often result in fewer design iterations.

5.1 Allowed Transient Voltage Excursion

The allowed output voltage excursion during a load transient (ΔVc_s) is:

$$\Delta V_{c\_s} = (\delta\% - \varepsilon\%) \cdot V_{nom} - \frac{1}{2} V_{rip}. \quad (7)$$

Where ±δ% is the output voltage regulation window and ±ε% is the output voltage initial accuracy.

Example: Vnom = 5V, δ% = 7%, ε% = 3.4%, Vrip = 40mV peak to peak.

$$\Delta V_{c\_s} = (7\% - 3.4\%) \times 5V - \frac{40\ mV}{2}$$
$$= 160\ mV. \quad (8)$$

Since the ripple voltage is included in the calculation of ΔVc_s, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply maximum load current change specification, ΔIc_s.

5.2 Maximum ESR Calculation

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (Re) is too high, the load transient requirement will not be met, no matter how large the capacitance.

The maximum allowed total combined ESR is:

$$R_{e\_max} = \frac{\Delta V_{c\_s}}{\Delta I_{c\_s}} \quad (9)$$

Example: ΔVc_s = 160mV, ΔIc_s = 3A. Then Re_max = 53.3mΩ.

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

5.3 Minimum Capacitance Calculation

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \cdot \left[\Delta V_{c\_s} - \sqrt{(\Delta V_{c\_s})^2 - (\Delta I_{c\_s} \cdot R_e)^2}\right]}{V_{nom} \cdot R_e^2} \quad (10)$$

Notice it is already assumed the total ESR, Re, is no greater than Re_max, otherwise the term under the square root will be a negative value. Also, it is assumed that L has already been selected, therefore the minimum L value should be calculated before Cmin and after Re (see Inductor Selection below). Example: Re = 20mΩ, Vnom = 5V, ΔVc_s = 160mV, ΔIc_s = 3A, L = 8µH

$$C_{min} = \frac{8\,\mu H \cdot \left[160\,mV - \sqrt{(160\,mV)^2 - (3A \times 20\,m\Omega)^2}\right]}{5 \times (20\,m\Omega)^2}$$

$$= 47\,\mu F. \quad (11)$$

Generally speaking, Cmin decreases with decreasing Re, ΔIc_s, and L, but with increasing Vnom and ΔVc_s.

6 Inductor Selection

The size of the output inductor (**L1** and **T1A**) can be determined from the desired output ripple voltage, Vrip, and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in} - V_{nom}}{f \cdot V_{in}} \cdot \frac{V_{nom} \cdot R_e}{V_{rip}} \quad (12)$$

In the above equation, Re is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to Re. In the case of ceramic capacitors, replace Re with the true impedance.

Example: Vin (max)= 30V, Vnom = 5.0V, Vrip = 40mV, Re =20mΩ, f = 300kHz

$$L_{min} = \frac{30V - 5.0V}{300\,kHz \cdot 30V} \cdot \frac{5.0V \cdot 20\,m\Omega}{40\,mV}$$

$$L_{min} = 7\,\mu H \quad (13)$$

Lmin = 7µH

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered. If an inductance value larger than Lmin is selected, make sure that the Cmin requirement is not violated.

Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

$$I_{rip} = \frac{(V_{in} - V_{nom})}{f \cdot L} \cdot D \quad (14)$$

Also important is the ripple content, which is defined by Irip /Inom. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content will cause too much loss in the inductor.

Example: Vin = 12V, Vnom = 5.0V, f = 300kHz, L = 8µH

$$I_{rip} = \frac{12V - 5.0V}{300\,kHz \cdot 8\,\mu H} \cdot \frac{5.0V}{12V} = 1.22A \quad (15)$$

Given a maximum load current of 3A, the ripple content is 1.2A / 3A = 40%.

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

7 Input Capacitor Selection

The LM2645 eval. board provides 5 input capacitor options for each channel (**C5, C6, C28, C29, C32** and **C16, C17, C30, C31, C33**). Referring to , two capacitors are used on each channel and their placement depends on the method of current sensing. C6 and C16 can be installed when higher input capacitances are necessary.

The fact that the two switching channels of the LM2645 are 180° out of phase will reduce the RMS value of the ripple current seen by the input capacitors. This will help extend input capacitor life span and result in a more efficient system. Input capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. In applications in which output voltages are less than half of the input voltage, the corresponding duty cycles will be less than 50%. This means there will be no overlap between the two channels' input current pulses. The equation for calculating the maximum total input ripple RMS current for duty cycles under 50% is:

$$I_{irrm} = \sqrt{I_1^2 D_1 (1 - D_1) + I_2^2 D_2 (1 - D_2) - 2 I_1 I_2 D_1 D_2} \tag{16}$$

where I1 is maximum load current of Channel 1, I2 is the maximum load current of Channel 2, D1 is the duty cycle of Channel 1, and D2 is the duty cycle of Channel 2.

Example: Imax_1 = 3.6A, Imax_2 = 3.6A, D1 = 0.42, and D2 = 0.275

$$I_{irrm} = \left[(3.6A)^2 \cdot 0.42 \cdot (1 - 0.42) + (3.6A)^2 \cdot 0.275 \cdot (1 - 0.275) - 2 \cdot 3.6A \cdot 3.6A \cdot 0.42 \cdot 0.275 \right]^{.5} = 2.75A. \tag{17}$$

Choose input capacitors that can handle 2.75A ripple RMS current at highest ambient temperature. In applications where output voltages are greater than half the input voltage, the corresponding duty cycles will be greater than 50%, and there will be overlapping input current pulses. Input ripple current will be highest under these circumstances. The input RMS current in this case is given by:

$$I_{irrm} = \left[\begin{array}{l} \left[I_1 (1 - D_1) + I_2 (1 - D_2) \right]^2 (D_1 + D_2 - 1) \\ + \left[I_1 (1 - D_1) - I_2 (D_2) \right]^2 (1 - D_2) + \\ \left[I_2 (1 - D_2) - I_1 (D_1) \right]^2 (1 - D_1) \end{array} \right]^{.5} \tag{18}$$

Where, again, I1 and I2 are the maximum load currents of channel 1 and 2, and D1 and D2 are the duty cycles. This equation should be used when both duty cycles are expected to be higher than 50%.

Input capacitors must meet the minimum requirements of voltage and ripple current capacity. The size of the capacitor should then be selected based on hold up time requirements. Bench testing for individual applications is still the best way to determine a reliable input capacitor value. The input capacitor should always be placed as close as possible to the current sense resistor or the drain of the top FET.

8 MOSFET Selection

Power MOSFETs are very fast switching devices. In synchronous rectifier converters, the rapid increase of drain current in the top FET coupled with parasitic inductance will generate unwanted $L\Delta i / \Delta t$ noise spikes at the source node of the FET (SWx node) and also at the V_{IN} node. The magnitude of this noise will increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance.

To reduce this switching noise, the LM2645 board provides two resistors in series with the CBOOTx pin (R24, R25). These resistors slow down the rise time of the top FET, yielding a longer drain current transition time and reduced switch node ringing. Top FET switching losses will increase with higher resistance values.

8.1 Bottom FET Selection (Q2 and Q4)

During normal operation, the bottom FET is switching on and off at almost zero voltage. Therefore, only conduction losses are present in the bottom FET. The most important parameter when selecting the bottom FET is the on resistance (Rdson). The lower the on resistance, the lower the power loss. The bottom FET power loss peaks at maximum input voltage and load current. The equation for the maximum allowed on resistance at room temperature for a given FET package, is:

$$R_{dson\_max} = \frac{1}{I_{max}^2 \cdot \left(1 - \frac{V_{nom}}{V_{in\_max}}\right)} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC \cdot (T_{j\_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (19)$$

where Tj_max is the maximum allowed junction temperature in the FET, Ta_max is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on resistance which is typically in the range of 10,000ppm/°C.

If the calculated Rdson_max is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the Imax term in the above equation, thus reducing Rdson. When using two FETs in parallel, multiply the calculated Rdson_max by 4 to obtain the Rdson_max for each FET. In the case of three FETs, multiply by 9.

$$R_{ds\_max} = \frac{1}{(3.6A)^2 \cdot \left(1 - \frac{5V}{30V}\right)} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 35.3\,m\Omega \quad (20)$$

If the selected FET has an Rds value higher than 35.3Ω, then two FETs with an Rdson less than 141mΩ (4 x 35.3mΩ) can be used in parallel. In this case, the temperature rise on each FET will not go to Tj_max because each FET is now dissipating only half of the total power.

8.2 Top FET Selection (Q1 and Q3)

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and bottom diode reverse recovery loss. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

$$R_{ds\_max} = \frac{V_{in\_min} \cdot .4}{I_{max}^2 \cdot V_{nom}} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC \cdot (T_{j\_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (21)$$

Example: Tj_max = 100°C, Ta_max = 60°C, Rqja = 60°C/W, Vin_min = 4.5V, Vnom = 5V, and Iload_max = 3.6A.

$$R_{ds\_max} = \frac{5.5V \times .4}{(3.6A)^2 \times 5V} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 13\,m\Omega \quad (22)$$

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

9 Loop Compensation

The general purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked to determine small-signal performance. Loop gain is equal to the product of control-output transfer function and the output-control transfer function (the compensation network transfer function). Generally speaking it is a good idea to have a loop gain slope that is -20dB /decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency, i.e. 60kHz in the case of 300kHz operation. The higher the bandwidth is, the faster the load transient response speed will potentially be. However, if the duty cycle saturates during a load transient, further increasing the small signal bandwidth will not help. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain will be relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot.

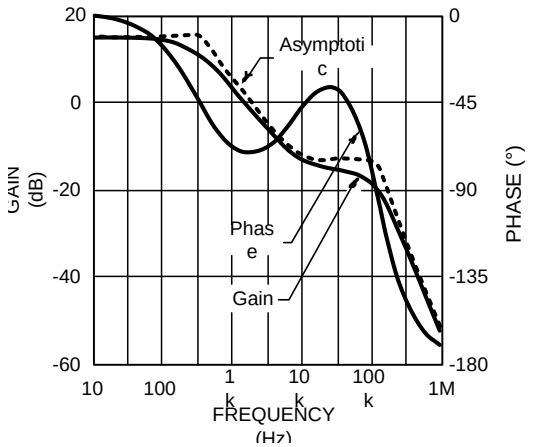

Figure 6. Control-Output Transfer Function

As shown in Figure 6, the control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency). The following can be done to create a -20dB /decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at fp, the second pole at fz, and the second zero at fn. The resulting output-control transfer function is shown in Figure 7.

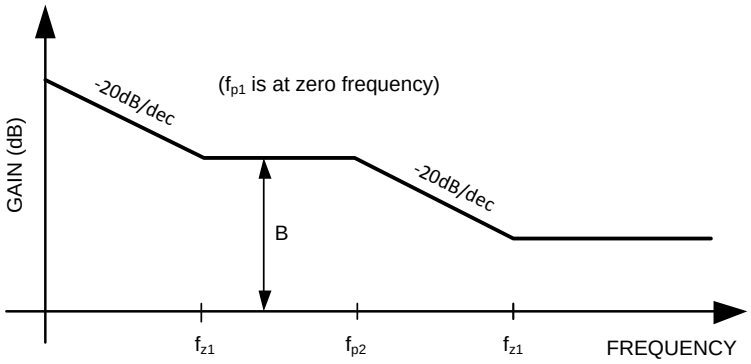

Figure 7. Output-Control Transfer Function

The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

$$f_z = \frac{1}{2\pi R_e C_o} \quad (23)$$

$$f_p = \frac{1}{2\pi R_o C_o} + \frac{.5}{2\pi L f C_o} \quad (24)$$

Since fp is determined by the output network, it will shift with loading (Ro). It is best to use a minimum Iout value of approximately 100mA when determining the maximum Ro value.

Example: Re=20mΩ, Co=100uF, Romax=5V/100mA=50Ω:

$$f_z = \frac{1}{2\pi \cdot 20\,m\Omega \cdot 100\,\mu F} = 80\,kHz \quad (25)$$

$$f_{p\,min} = \frac{1}{2\pi \cdot 50\Omega \cdot 100\,\mu F} + \frac{.5}{2\pi \cdot 300k \cdot 8\mu \cdot 100\,\mu F} = 363\,Hz \quad (26)$$

First determine the minimum frequency (fpmin) of the pole across the expected load range, then place the first compensation zero at or below that value. Once fpmin is determined, Rc1 (**R5** and **R11**) should be calculated using:

$$R_{c1} = \frac{B}{gm}\left(\frac{R_1 + R_2}{R_1}\right) \quad (27)$$

Where B is the desired gain in V/V at fp (fz1), gm is the transconductance of the error amplifier, and R1 and R2 are the feedback resistors. A gain value around 10dB (3.3v/v) is generally a good starting point.

Example: B=3.3v/v, gm=650m, R1=20KΩ, R2=60.4KΩ:

$$R_{c1} = \frac{3.3}{650\mu}\left(\frac{20k + 60.4k}{20k}\right) = 20.4\,k\Omega \cong 20\,k\Omega \quad (28)$$

Bandwidth will vary proportional to the value of Rc1. Next, Cc1 (**C10** and **C17**) can be determined with the following equation:

$$C_{c1} = \frac{1}{2\pi \cdot f_{p\,min} \cdot R_{c1}} \quad (29)$$

Example: fpmin=363Hz, Rc1=20KΩ:

$$C_{c1} = \frac{1}{2\pi \cdot 363\,Hz \cdot 20\,k\Omega} \cong 22\,nF \quad (30)$$

The compensation network (Figure 8) will also introduce a low frequency pole which will be close to 0Hz.

A second pole should also be placed at fz. This pole can be created with a single capacitor Cc2 (**C8** and **C24**) and a shorted Rc2 (see Figure 8). The minimum value for this capacitor can be calculated by:

$$C_{c2\,min} = \frac{1}{2\pi \cdot f_z \cdot R_{c1}} \quad (31)$$

Cc2 may not be necessary, however it does create a more stable control loop. This is especially important with high load currents and in current sharing mode.

Example: fz=80kHz, Rc1= 20KΩ:

$$C_{c2\,min} = \frac{1}{2\pi \cdot 80\,kHz \cdot 20\,k\Omega} \cong 100\,pF \quad (32)$$

A second zero can also be added with a resistor in series with Cc2 (**R10** and **R27**). If used, this zero should be placed at fn, where the control to output gain rolls off at -40dB/dec. Generally, fn will be well below the 0dB level and thus will have little effect on stability. Rc2 can be calculated with the following equation:

$$R_{c2} = \frac{1}{2\pi \cdot f_n \cdot C_{c2}} \quad (33)$$

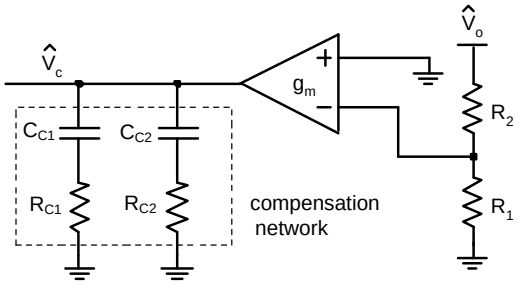

Figure 8. Compensation Network

10 PCB Layout

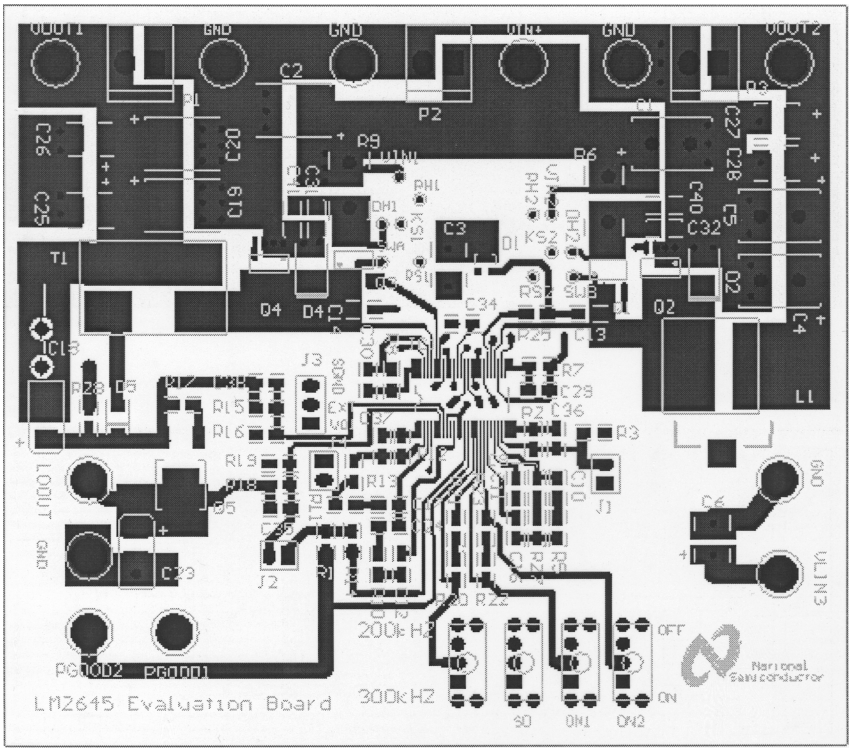

Figure 9. Top Layer

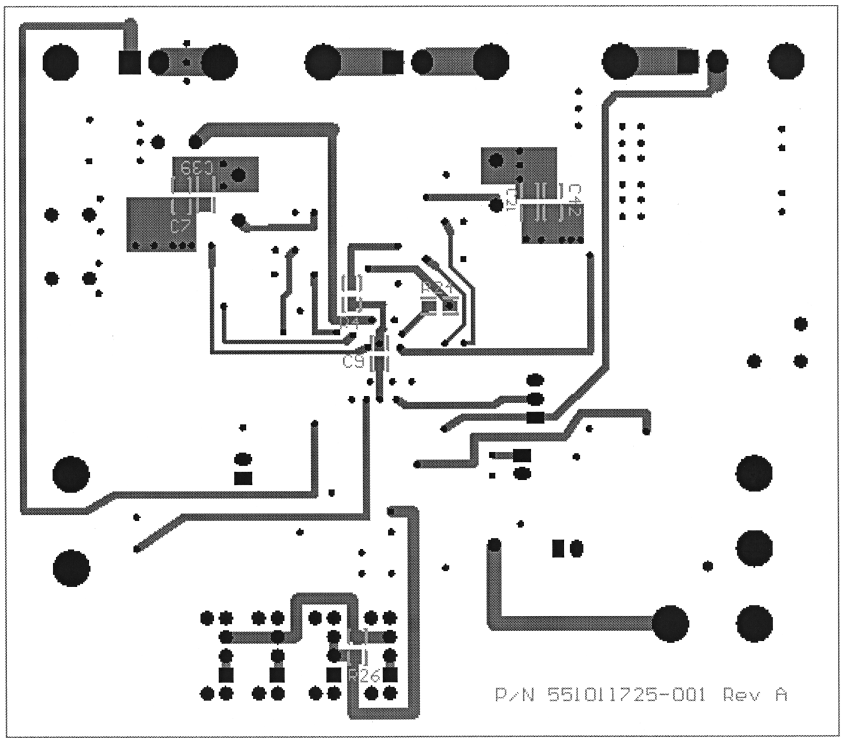

Figure 10. Bottom Layer

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265