Application Report
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Clocking Design Guidelines: Unused Pins

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ABSTRACT

Although every effort is made to provide detailed information in product data sheets to inform the design engineer of the expected performance and assist in the proper application of the device, it is unlikely that every question will be anticipated. An example of this situation is the topic of unused pins. If after reviewing the capabilities of a part, it been determined that a certain feature of a device is not needed, then it is likely there will be remaining unused pins. The design engineer will want to know what the recommendation is for these unused pins. Should they be left open, tied to ground, or pulled high? This paper reviews why these are important questions and uses actual customer questions handled by the TI applications staff as examples.

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1 Summary

This paper is intended as an aid for those engineers who have chosen to use Texas Instruments clocking products in their design, but subsequently discover that the existing data sheet or available documentation does not provide clear guidance for the product operating conditions in the case of unused pins. What is the recommendation when there are unused pins? Should unused pins simply be left open and floating? Or, should they be tied to ground or possibly biased to some voltage level? And why should this matter?

2 Unused Pin Considerations

Let's assume that after reviewing the capabilities of a part and comparing to the requirements of the end application, it been determined that a certain feature of a device will not be needed. Given this situation, it is possible that the result may be some pins not being required. Should the design engineer be concerned about unused pins? One might ask, "If it is not being used, then why should it matter?"

The general answer to this question is that it is simply good engineering practice to understand the functionality of the device under consideration and assure that it is applied properly. Part of the process for maximizing first-time success is to account for any unused pins that remain after the application of the product. But, there can be other reasons why one would want to take note if there are unused pins in final design.

One consideration is whether there is any relationship between unused pins and the inherent operation of the device itself. In some cases, the decision on how to handle unused pins can have an effect on the resulting performance of the device. An example of this would be the scenario of having unused output pins for a device that is based on an LVPECL clocking architecture. In this case, terminating an open output pin increases overall power dissipation. This can be seen by reviewing the CDCLVP1212 data sheet (SCAS886D). This device is a low additive jitter LVPECL buffer that can create 12 LVPECL output pairs. The supply current specifications provided in the data sheet are shown in Table 1.

Table 1. CDCLVP1212 Supply Current

Parameter		Test Conditions	CDCLVP1212			Unit
			MIN	TYP	MAX	
I_{EE}	Supply internal current	Outputs unterminated			88	mA
I_{CC}	Output and internal supply current	All outputs terminated, 50 Ω to V_{CC} – 2			468	mA

As can be seen, the supply current is specified for the case of all outputs terminated, as well as the case of all outputs unterminated. If the intended application of this product is to utilize the full 12 output capability, then the power dissipation is represented by both the internal and external current under an all output load termination condition (468 mA × 3.3 V = 1500 mW).

Note that under the operating condition where all outputs are un-terminated, the supply current is given as a much lower value of 88 mA. The maximum power dissipation will be a combination of the inherent internal dissipation of the part + the external load dissipation. The overall external load dissipation will be a function of the number of terminated outputs. As shown in Figure 1, an LVPECL output stage is an open-emitter transistor. The power dissipated in this stage is a function of the current established when the external termination resistors are connected. (1) So, if there are unused LVPECL outputs in a given application and those unused outputs are terminated, they will be contributing to the overall power dissipation. A rough approximation is about 20 mW per LVPECL output pair.

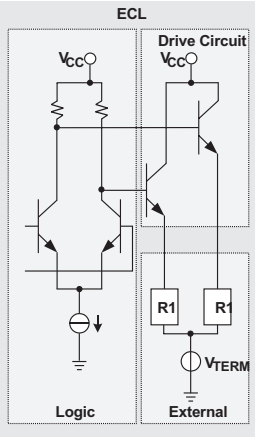


Figure 1. LVPECL Simplified Drive Circuit Diagram

If you are using an LVPECL clocking buffer and not utilizing the full fanout capability, be aware that the overall power dissipation can be reduced by not terminating the unused outputs.

A similar recommendation applies for LVDS outputs, but the reduction is not as significant. The reason being that LVDS is a lower power architecture and power dissipation contribution of the load is much lower. This can be seen in Figure 2, where the simplified diagram illustrates that the LVDS drive is a 3.5-mA current source. [2] So, when terminated in a 100-Ω termination, the resulting power dissipation represented by the load is $P = I^2R = (0.0035)^2 \times 100 = 1.2$ mW.

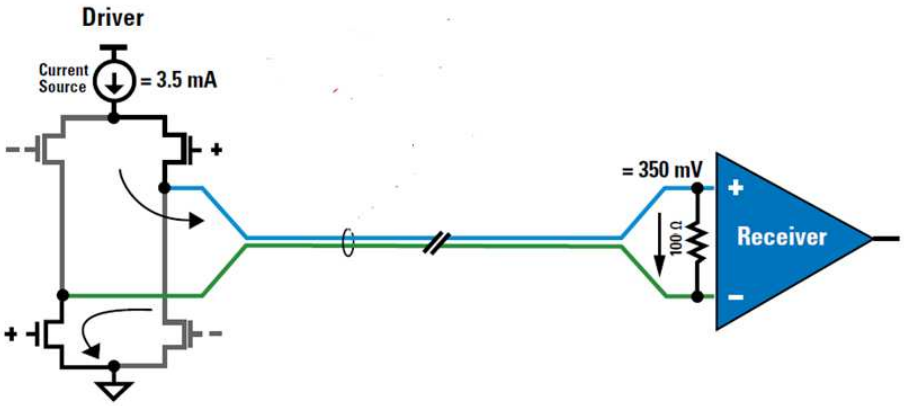


Figure 2. LVDS Simplified Drive Circuit Diagram

Device power dissipation is an example of a “general” unused pin design consideration that the engineer should keep in mind, but sometimes there will be questions regarding unused pin scenarios for a particular device. The following information provides responses to common customer questions for specific products.

3 Unused Pin Examples: Customer Questions and Recommendations

3.1 CDCE62005: 5/10 Output Clock Generator/Jitter Cleaner with Integrated Dual VCO

Question #1: "What do I do with the SEC_REF+ and SEC_REF– pins, if I'm not using this input? Should both of these unused inputs be grounded (see Figure 3)?"

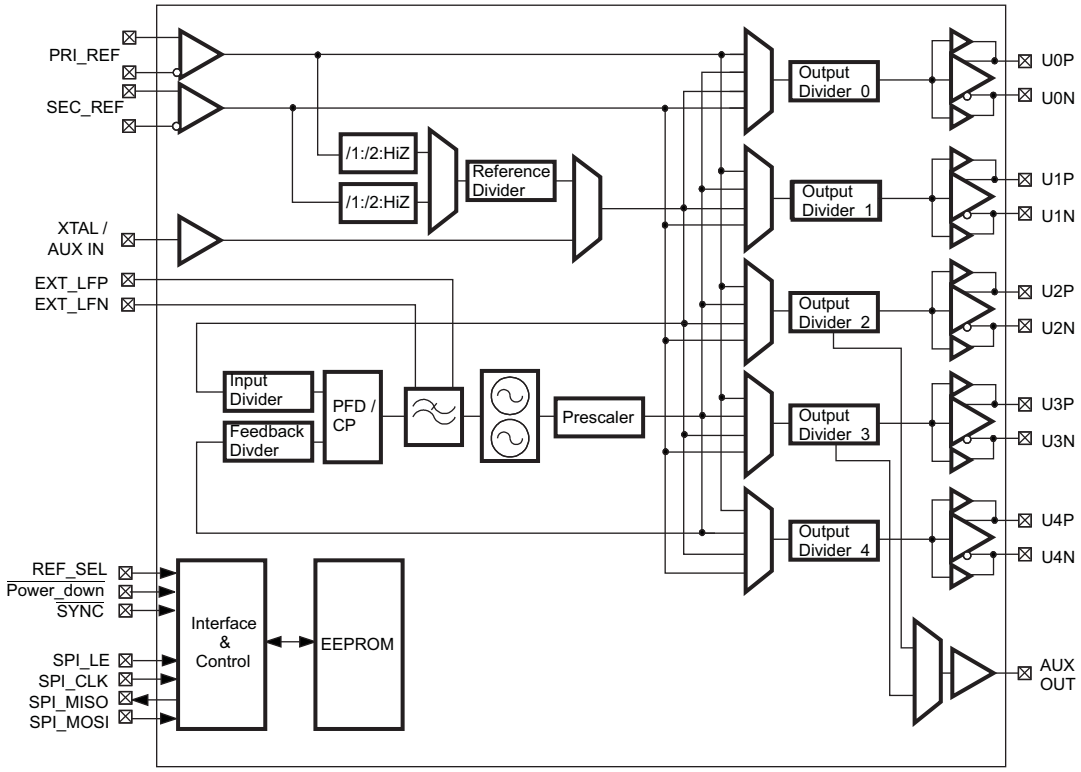


Figure 3. CDCE62005 Functional Block Diagram

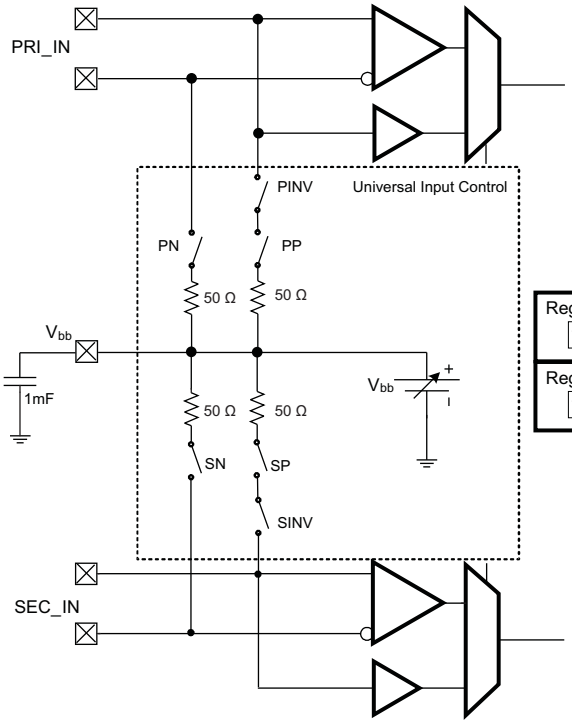
Response: The decision for how to handle unused PRI_REF/SEC_REF inputs depends on the input buffer selection. These unused input pins should be connected depending on the buffer type selected, as described as follows:

- If input buffer selection is LVCMOS (internal termination is turned off), the unused inputs should be connected to ground through 1-kΩ resistors.
- If input buffer selection is differential (LVDS/LVPECL) , then connect one input of the differential pair to V_{DD} and other input to ground through 1-kΩ pullup and pulldown resistors.

Question #2: "Is there a preference to select internal termination vs external termination? For example, in the case of the SEC REF +/– inputs, if PRI REF +/– is CMOS, it is suggested to tie the unused SEC REF +/– to gnd via a 1-kΩ external resistor. But, there is also the option to set internal termination resistors for these pins via internal register settings. What are the considerations for whether to use external or internal termination?"

Response: When you choose PRI_REF as LVCMOS input, the SEC_REF will also be selected as LVCMOS input. The reason is that the same register bit selects the buffer type, so both input buffers are selected as the same type. So, in the case of the LVCMOS buffer selection, the recommendation is to ground both input pins to ground through 1-kΩ resistors.

Regarding the internal input termination resistors, these are an option as part of the universal buffer input stage, although they are not intended for terminating unused pins. Rather, they are intended for providing receiver input termination for LVPECL (50-Ω termination) or LVDS (100-Ω termination) drivers. These internal termination values can be configured for the appropriate termination based on the PN, PP, and PINV switch setting selections made in register 5 (see Figure 4). The basic consideration on whether to use external or internal termination will be performance. External termination is usually more accurate since it will exhibit tighter tolerance and has less temperature variation vs integrated silicon-based internal resistors.



Settings			Nominal
5.1	5.0	5.6	
INBUFSELY	INBUFSELX	ACDCSEL	Vbb
1	0	0	1.9V
1	0	1	1.2V
1	1	0	1.2V
1	1	1	1.2V

Register 6

12

Register 5

10	9	8	7	6	1	0

Settings				SWITCH Status		
5.0	5.1	5.8, 6.12	5.9,5.10			
INBUFSELX	INBUFSELY	TERMSEL	INVBB	P	N	INV
0	0	X	X	OFF	OFF	OFF
X	X	1	X	OFF	OFF	OFF
X	1	0	0	ON	ON	ON
X	1	0	1	ON	ON	OFF

Figure 4. CDCE62005 Universal Input Buffer

Question #3: “What do I do with the unused AUX_IN?”

Response: If the AUX_IN pin is not used, it is recommended to connect this pin to ground through a 1-kΩ resistor. In addition, the VCC_AUX power supply pin, intended for powering the internal 3.3-V crystal oscillator circuitry, can be left open/not connected.

3.2 CDCLVP1212: Low Jitter, 2-Input Selectable 1:12 Universal-to-LVPECL Buffer

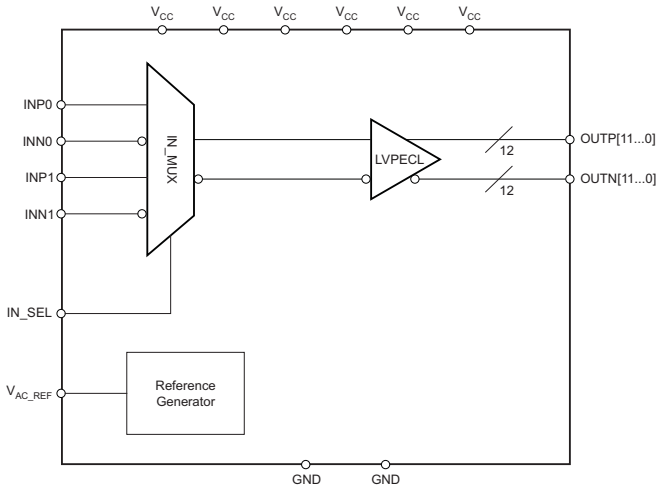


Figure 5. CDCLVP1212 Simplified Diagram

Question #4: "What should I do with the VAC_REF, pin 7, if unused? Do I still put a 0.1-µF capacitor to ground as it recommends in the pin description table on page 5 of the data sheet (see Figure 5)?"

Table 2. CDCLVP1212 V_{AC_REF} Pin Description

Terminal Name	Terminal Number	Type	Pullup/ Pulldown	Description
V_{AC_REF}	7	Output	—	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1-µF capacitor to GND on this pin. The output current is limited to 2 mA.

Response: If the internal biasing/ V_{AC_REF} function is not used (assuming external biasing and termination is used), then connection of that capacitor to the V_{AC_REF} pin is not required.

3.3 CDCLVD1204: Low Jitter, 2-Input Selectable 1:4 Universal-to-LVDS Buffer

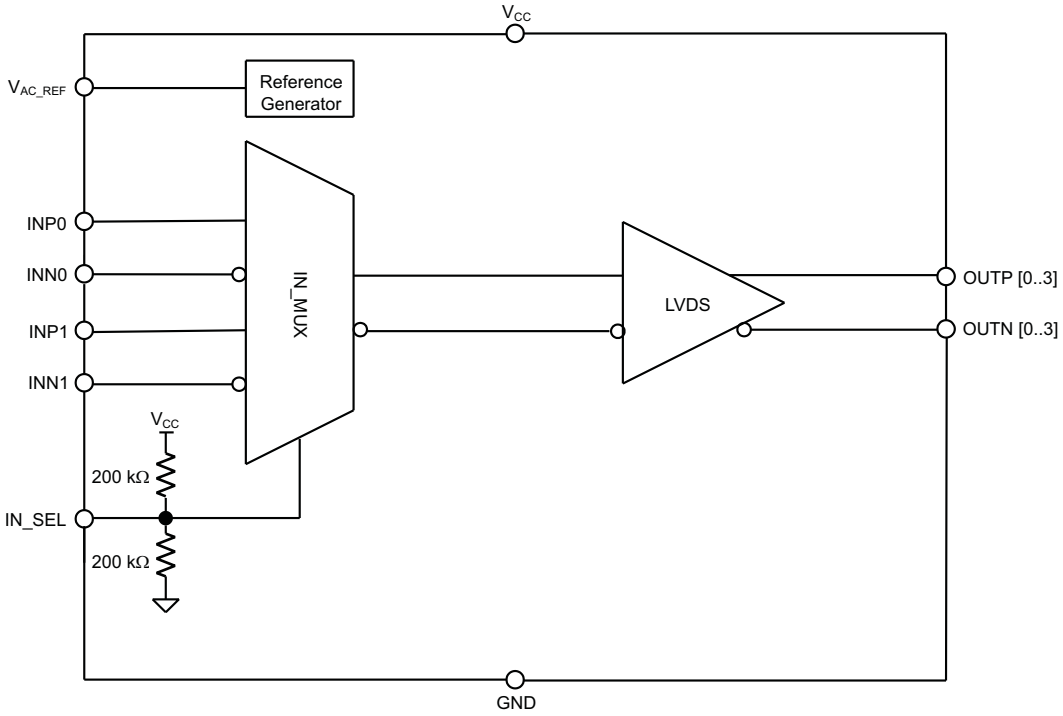


Figure 6. CDCLVD1204 Simplified Diagram

Question #5: "What are the recommendations for unused inputs and outputs (see Figure 6)?"

Response: Unused outputs can be left open, although it is recommended to not connect any traces to unused output pins. But, for unused inputs, it is recommended to connect both unused input pins, INPx, INNx, to ground thru using 1-kΩ resistors. Open outputs can conserve power, while terminating the inputs will help minimize the receiver stage from picking up noise.

3.4 CDCLVP110: 1:10 LVPECL/HSTL to LVPECL Clock Driver

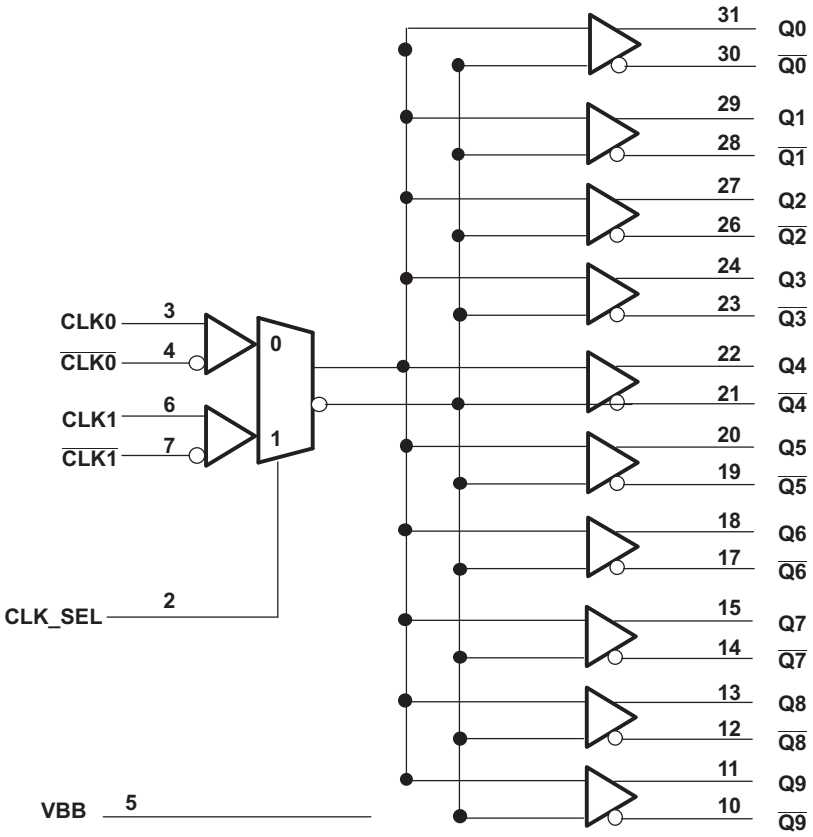


Figure 7. CDCLVP110 Simplified Diagram

Question #6: "We are using the CDCLVP110 for differential signaling, but we do not know what to do with the VBB pin then. Do we tie it high, or low, or leave it open (see Figure 7)?"

Response: Yes, you can leave VBB floating if you do not use that. You can use this VBB biasing voltage if you use ac-coupled differential input.

Question #7: "I am only using six of the 10 outputs of the CDCLVP110. How do I calculate power dissipation savings when 4 outputs are unused?"

Response: From CDCLVP110 data sheet (SCAS683D):

IEE - Max internal supply current = 82 mA

ICC - Max output + internal supply current (with all outputs terminated in 50 Ω) = 370 mA

Therefore, Max current due to load (20 terminations) = ICC – IEE = 370 mA – 82 mA = 288 mA.

So, output current due to load/channel = 288/20 = 14.4 mA.

Power dissipation per load = $I^2R = (.0144)^2 \times 50\ \Omega$ = 10 mW/load termination(or 20 mW per differential output pair).

Therefore, expected power dissipation savings associated with 4 unused outputs is 80 mW.

3.5 CDCV304: General Purpose and PCI-X 1:4 Clock Buffer

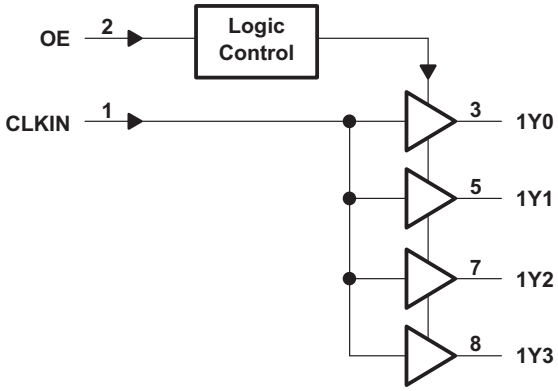


Figure 8. CDCV304 Simplified Diagram

Question #7: "Do the unused outputs need to be terminated? If so, what is the recommended termination (see Figure 8)?"

Response: TI recommends leaving the unused outputs floating without connecting any traces to the output pin.

4 Conclusion

Do not ignore unused pins as you finalize your design. If the available product documentation does not specifically provide recommendations regarding the status of unused pins, then the manufacturer's local or factory applications staff should be contacted for further guidance.

5 References

1. *Power Consumption of LVPECL and LVDS* (SLYT127)
2. *LVDS Handbook* (www.ti.com/LVDS)
3. *CDCE62005 Data Sheet* (SCAS862F)
4. *CDCLVP1212 Data Sheet* (SCAS886D)
5. *CDCLVD1204 Data Sheet*(SCAS898A)
6. *CDCLVP110 Data Sheet*(SCAS683D)
7. *PCB Layout Guidelines for the CDCLVP110* (SCAA057)
8. *CDCV304 Data Sheet*(SCAS643H)

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